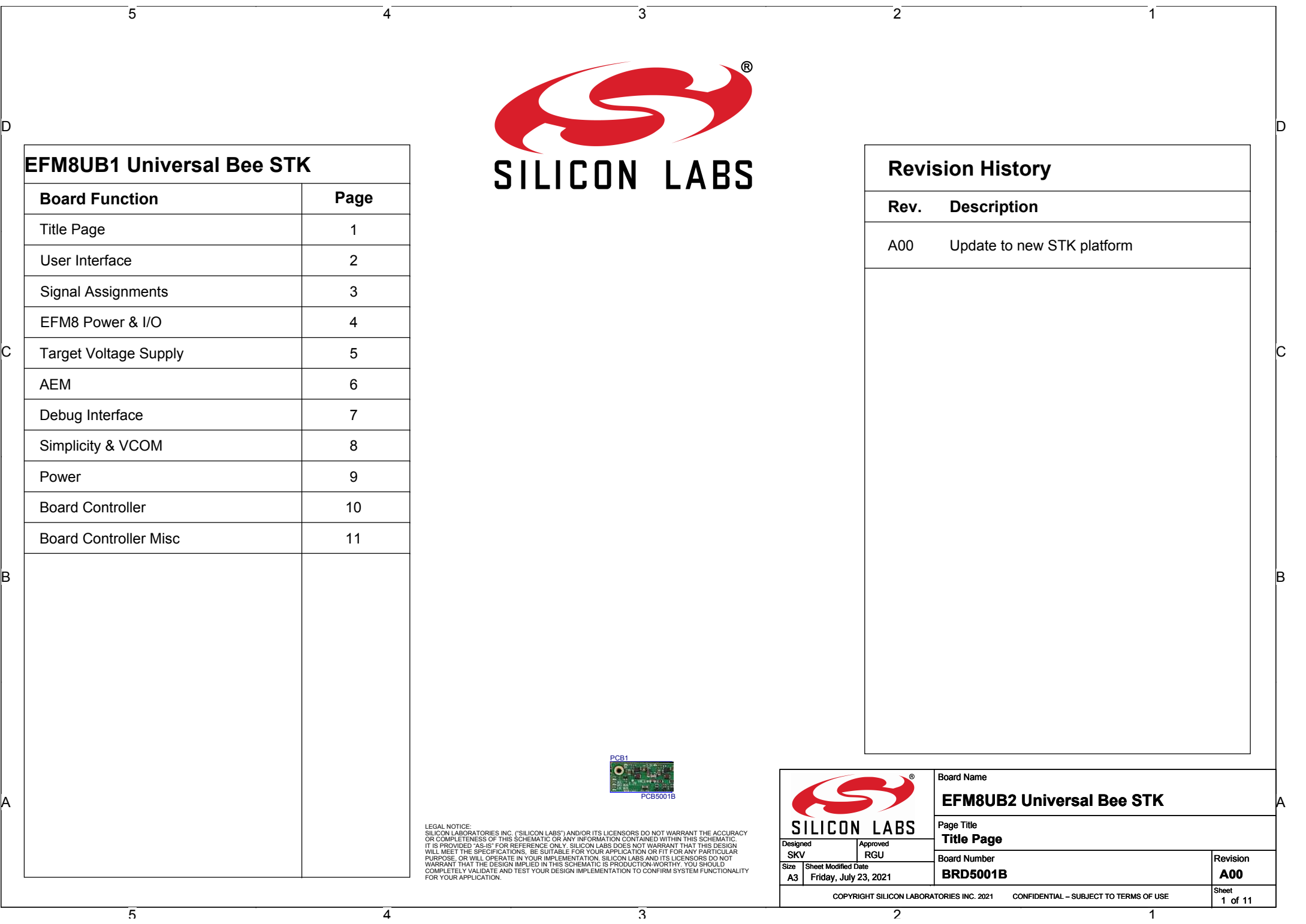
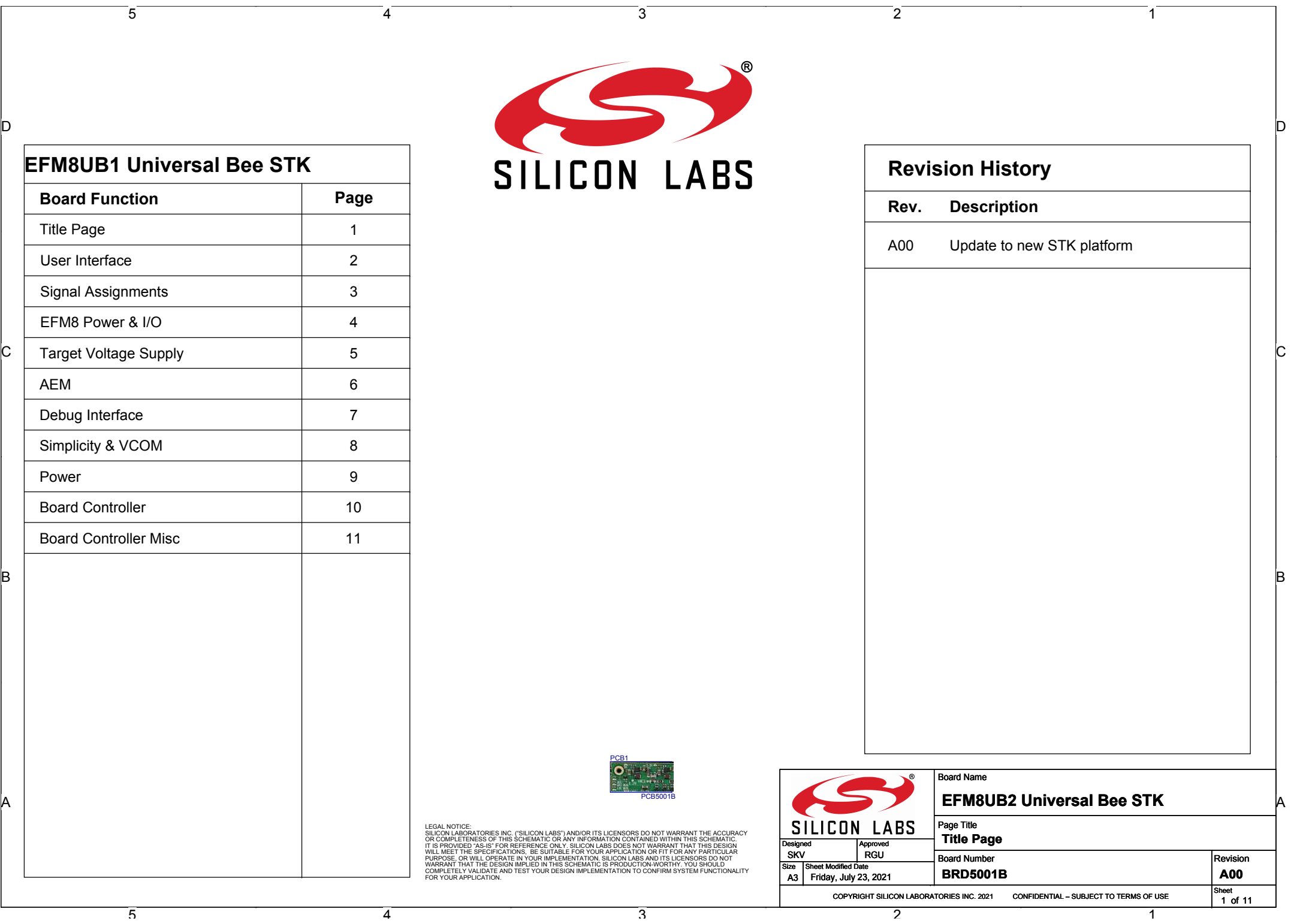


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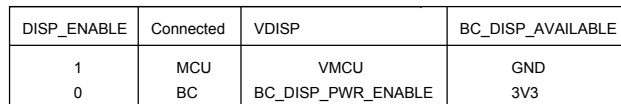
5



C



A



4



2



C



Breakout Connections

Diagram illustrating the breakout connections for two MCU boards, J101 and J102, showing pin mappings and connections to a debugger (D) and power supply (3V3).

J101 Pinout:

Pin	Label	Connection
1	VMCU	MCU_P4[7..0]
2	VMCU	MCU_P3[7..0]
3	GND	
4	NC	
5	NC	
6	NC	
7	NC	
8	NC	
9	NC	
10	NC	
11	NC	
12	NC	
13	NC	
14	NC	
15	NC	
16	NC	
17	RST	MCU_P4[7..0]
18	C2CK	MCU_P4[7..0]
19	C2D	MCU_P4[7..0]
20	P4.7	MCU_P4[7..0]
21	P4.6	MCU_P4[7..0]
22	P4.5	MCU_P4[7..0]
23	P4.4	MCU_P4[7..0]
24	GND	
25	3V3	
26	3V3	
27	3V3	
28	3V3	
29	3V3	
30	3V3	
31	3V3	
32	3V3	

J102 Pinout:

Pin	Label	Connection
1	5V	MCU_P0[7..0]
2	5V	MCU_P0[7..0]
3	GND	
4	P0.0	MCU_P0[7..0]
5	P0.1	MCU_P0[7..0]
6	P0.2	MCU_P0[7..0]
7	P0.3	MCU_P0[7..0]
8	P0.4	MCU_P0[7..0]
9	P0.5	MCU_P0[7..0]
10	P0.6	MCU_P0[7..0]
11	P0.7	MCU_P0[7..0]
12	P1.0	MCU_P1[7..0]
13	P1.1	MCU_P1[7..0]
14	P1.2	MCU_P1[7..0]
15	P1.3	MCU_P1[7..0]
16	P1.4	MCU_P1[7..0]
17	P1.5	MCU_P1[7..0]
18	P1.6	MCU_P1[7..0]
19	P1.7	MCU_P1[7..0]
20	P1.8	MCU_P1[7..0]
21	P1.9	MCU_P1[7..0]
22	P1.10	MCU_P1[7..0]
23	P1.11	MCU_P1[7..0]
24	P1.12	MCU_P1[7..0]
25	P1.13	MCU_P1[7..0]
26	P1.14	MCU_P1[7..0]
27	P1.15	MCU_P1[7..0]
28	P1.16	MCU_P1[7..0]
29	P1.17	MCU_P1[7..0]
30	P1.18	MCU_P1[7..0]
31	P1.19	MCU_P1[7..0]
32	P1.20	MCU_P1[7..0]

P0 Connections

The diagram illustrates the P0 Connections between an MCU and various peripheral signals. The connections are as follows:

- MCU_P0[7..0] is connected to a bus that branches to:
 - MCU_P0.7: EXP_HEADER6 → EXP_HEADER[16..3]
 - MCU_P0.6: SPI0_SCK → DISP_SCLK
 - MCU_P0.5: UART0_RX → VCOM_RX
 - MCU_P0.4: UART0_TX → VCOM_TX
 - MCU_P0.3 → UIF_BUTTON1
 - MCU_P0.2 → UIF_BUTTON0
 - MCU_P0.1 → DISP_CS
 - MCU_P0.0: R300 → VCOM_ENABLE
- MCU_P0.6 is also connected to EXP_HEADER8 → EXP_HEADER[16..3].
- MCU_P0.0 is connected to R300, which has an OR connection to NM.

C P1 Connections

The diagram illustrates the P1 Connections for the MCU. The connections are as follows:

- MCU_P1[7..0] is connected to a bus that branches to MCU_P1.7, MCU_P1.6, MCU_P1.5, MCU_P1.4, MCU_P1.3, MCU_P1.2, MCU_P1.1, and MCU_P1.0.
- MCU_P1.7 (PCA0_CEX1) is connected to UIF_LEDB.
- MCU_P1.6 (PCA0_CEX0) is connected to UIF_LEDG.
- MCU_P1.5 is connected to a bus that branches to MCU_P1.4, MCU_P1.3, MCU_P1.2, MCU_P1.1, and MCU_P1.0.
- MCU_P1.4 is connected to R301 (OR) and then to DISP_ENABLE.
- MCU_P1.3 (I2C0_SCL) is connected to EXP_HEADER15.
- MCU_P1.2 (I2C0_SDA) is connected to EXP_HEADER16.
- MCU_P1.1 (SPI0_CS) is connected to EXP_HEADER10.
- MCU_P1.0 (SPI0_MOSI) is connected to EXP_HEADER4.
- EXP_HEADER15 and EXP_HEADER16 are connected to EXP_HEADER[16..3].
- EXP_HEADER10 and EXP_HEADER4 are connected to EXP_HEADER[16..3].
- EXP_HEADER4 is also connected to DISP_SI.

B

P2 Connections

Diagram illustrating the P2 Connections. The MCU_P2[7..0] bus is connected to the following components:

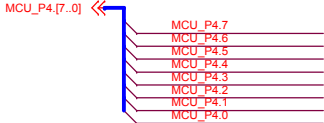
- MCU_P2.7: EXP_HEADER13 → EXP_HEADER[16..3]
- MCU_P2.6: EXP_HEADER11 → EXP_HEADER[16..3]
- MCU_P2.5: (unlabeled)
- MCU_P2.4: (unlabeled) → UIF_JOYSTICK
- MCU_P2.3: (unlabeled)
- MCU_P2.2: UART1_RX → EXP_HEADER14 → EXP_HEADER[16..3]
- MCU_P2.1: UART1_TX → EXP_HEADER12 → EXP_HEADER[16..3]
- MCU_P2.0: PCA0_CEX2 → UIF_LED

P3 Connections

Diagram illustrating the P3 Connections. The MCU_P3[7..0] bus is connected to the following components:

- MCU_P3.7: (unlabeled)
- MCU_P3.6: (unlabeled)
- MCU_P3.5: (unlabeled)
- MCU_P3.4: (unlabeled)
- MCU_P3.3: EXP_HEADER9 → EXP_HEADER[16..3]
- MCU_P3.2: EXP_HEADER7 → EXP_HEADER[16..3]
- MCU_P3.1: EXP_HEADERS → EXP_HEADER[16..3]
- MCU_P3.0: EXP_HEADERS → EXP_HEADER[16..3]

P4 Connections



MCU_P4[7..0] <<

- MCU_P4.7
- MCU_P4.6
- MCU_P4.5
- MCU_P4.4
- MCU_P4.3
- MCU_P4.2
- MCU_P4.1
- MCU_P4.0

DEBUG Connections

A



MCU_C2D >> DEBUG_TMS_SWDIO_C2D

MCU_C2CK_RESET >>

R302
1K

UIF_BTNRESET <<

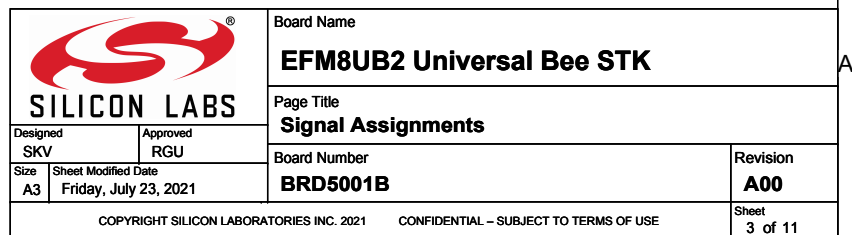
DEBUG_#RESET_C2CKPS >>

DEBUG_TCK_SWCLK_C2CK >>

DEBUG Connections

The diagram illustrates the debug connections for the MCU_C2D and MCU_C2CK_RESET signals. The MCU_C2D signal is connected to the DEBUG_TMS_SWDIO_C2D pin. The MCU_C2CK_RESET signal is connected to the DEBUG_TCK_SWCLK_C2CK pin. A 1K resistor (R302) is connected between the MCU_C2CK_RESET signal and the UIF_BTNRESET pin. The DEBUG_#RESET_C2CKPS pin is also connected to the UIF_BTNRESET pin.

```
graph LR; MCU_C2D[MCU_C2D] --> DEBUG_TMS_SWDIO_C2D[DEBUG_TMS_SWDIO_C2D]; MCU_C2CK_RESET[MCU_C2CK_RESET] --> R302[R302 1K]; R302 --> UIF_BTNRESET[UIF_BTNRESET]; DEBUG_#RESET_C2CKPS[DEBUG_#RESET_C2CKPS] --> UIF_BTNRESET; UIF_BTNRESET --> DEBUG_TCK_SWCLK_C2CK[DEBUG_TCK_SWCLK_C2CK];
```



D



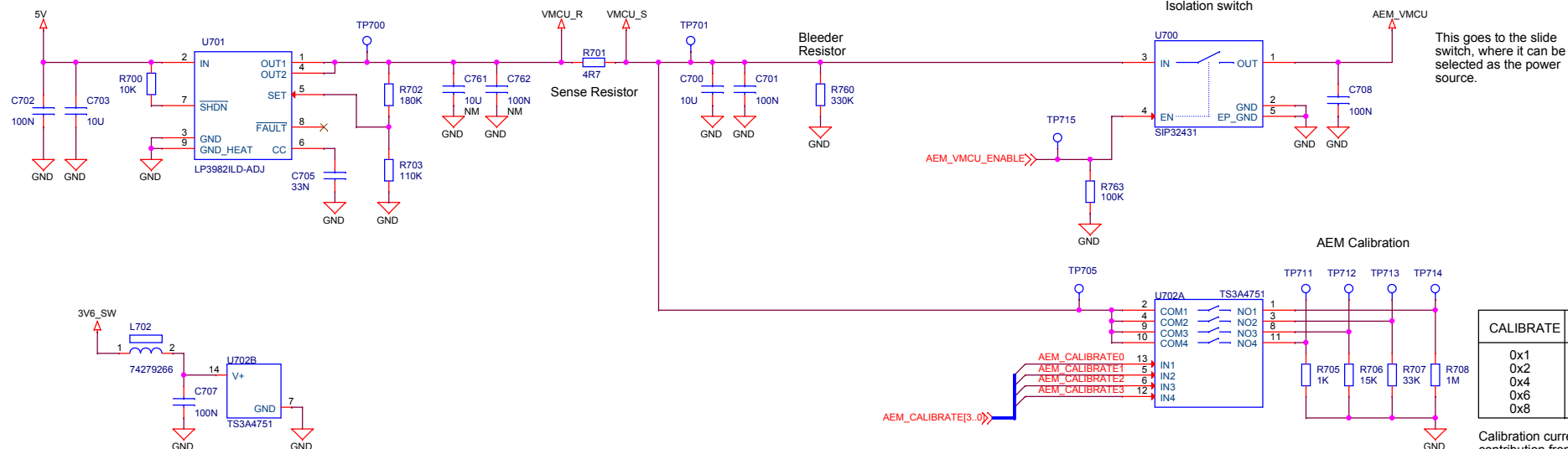
B

A

A



MCU Power Regulator



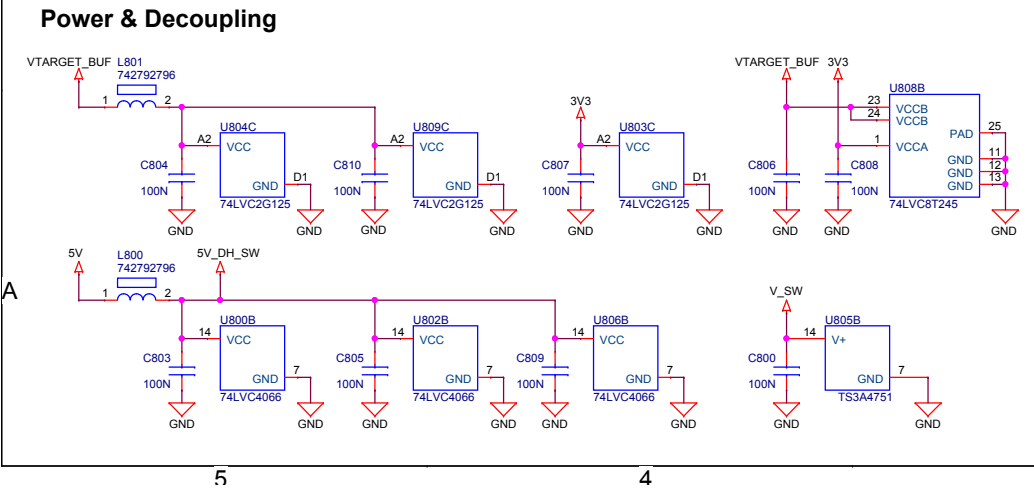
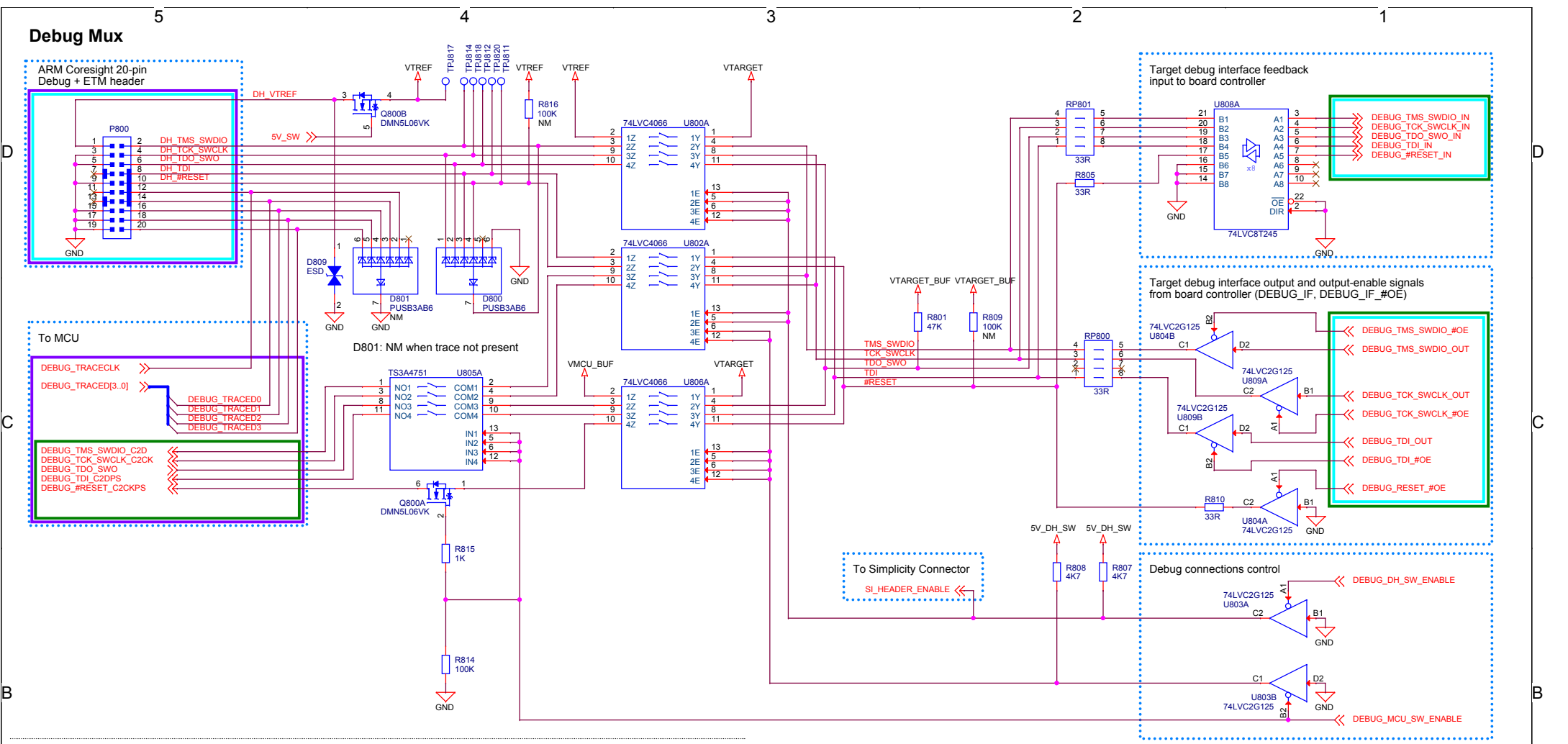
CALIBRATE	Calibration Current
0x1	13.30 uA
0x2	110 uA
0x4	230 uA
0x6	320 uA
0x8	3.30 mA

Calibration currents include contribution from sense and bleeder resistors.

 SILICON LABS		Board Name	
		EFM8UB2 Universal Bee STK	
Designed SKV		Page Title	
Approved RGU		Target Voltage Supply	
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A





Mode	DEBUG_DH_SW_ENABLE	DEBUG_MCU_SW_ENABLE	DEBUG_IF_#OE	VTREF	VTARGET
Debug Out	1	0	0/1	External voltage	External voltage
MCU Debug	0	1	0/1	Disconnected	VMCU
Debug In	1	1	1	VMCU	VMCU
Debug Off	0	0	1	-	-

Color coded frames indicates which groups of signal nodes that are active in a given debug mode



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Designed SKV Approved RGU

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Board Name

EFM8UB2 Universal Bee STK

Page Title

Debug Interface

Board Number

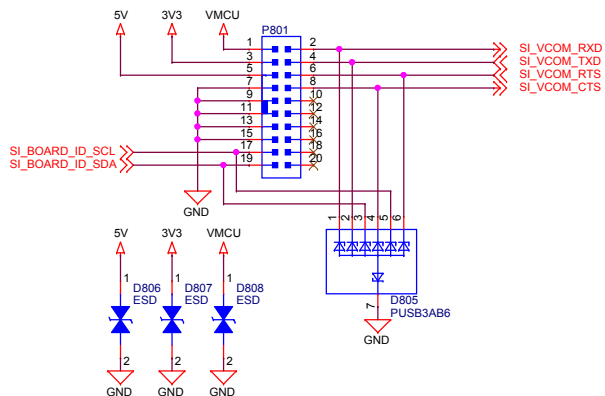
BRD5001B

Revision

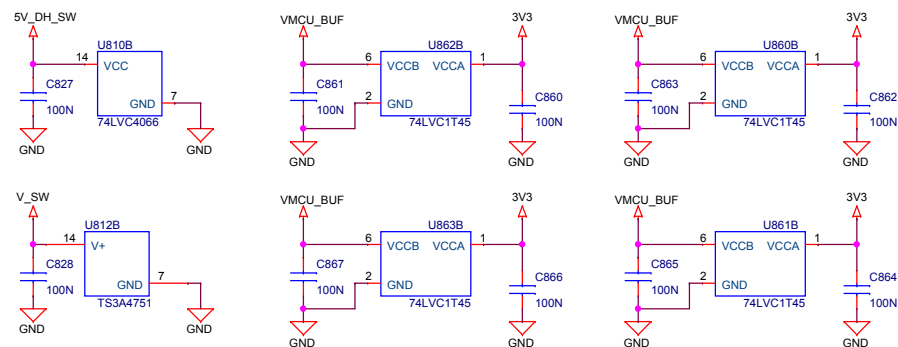
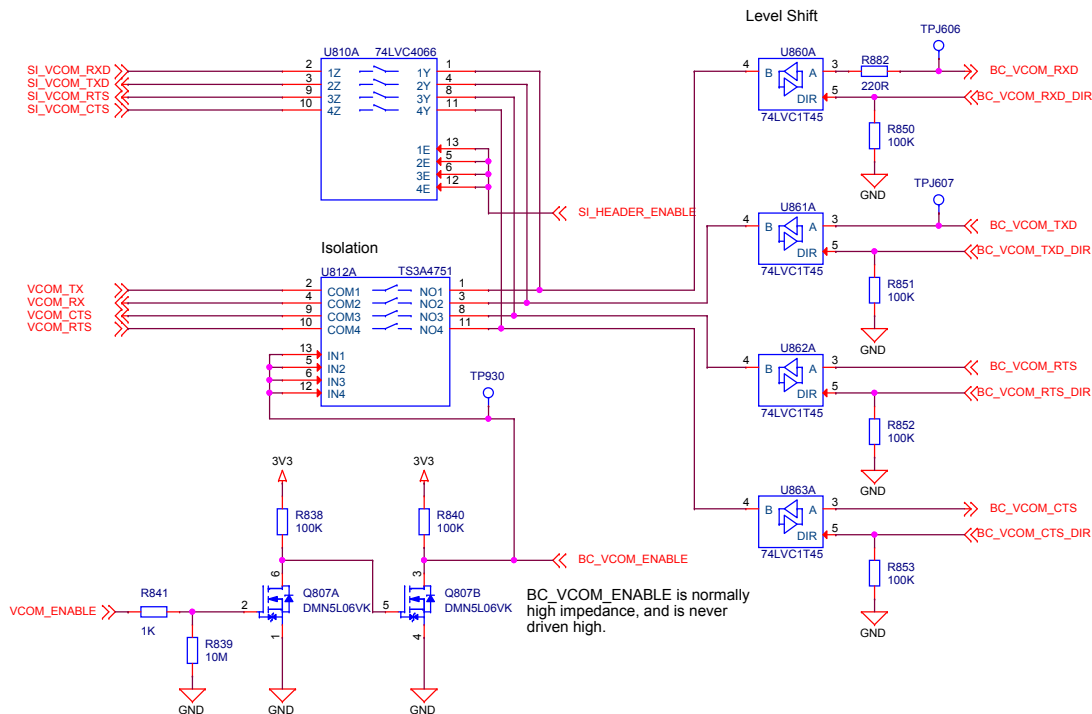
A00

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Simplicity Connector



VCOM Interface



		Board Name	
		EFM8UB2 Universal Bee STK	
Designed SKV		Page Title	
Size A3		Simplicity & VCOM	
Sheet Modified Date Friday, July 23, 2021		Board Number	Revision
		BRD5001B	A00
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J-Link USB Port

The schematic shows the internal wiring of the J-Link USB port. It features a P601 connector labeled WR_COM_USB_MINI_B with pins 1 through 9. Pins 8 and 9 are connected to GND. Pin 7 is connected to TPJ614. Pin 6 is connected to a 5V supply through an L600 inductor (742792662). Pin 5 is connected to TPJ613. Pin 4 is connected to the USB_DP signal line. Pin 3 is connected to the USB_DM signal line. Pin 2 is connected to TPJ611. Pin 1 is connected to TPJ612. The USB_DP and USB_DM signals are shown as red arrows pointing right. A DMM symbol is present near the top left.

Place these TPs close to USB header

TPJ614

TPJ613

L600
742792662

5V

USB DP

USB DM

D600 DT1446-04

TPJ611 TPJ612

GND

[illegible]

VMCU Voltage Mirror

The schematic diagram illustrates the VMCU Voltage Mirror circuit, which is divided into three main sections labeled 1, 2, and 3.

Section 1: This section shows a buffer stage. A 5V input is connected to the VDD of an MCP6001T op-amp (U606B) through a 33R resistor (R681). The op-amp's output is connected to a 10uF capacitor (C660) and then to a 5V_BUF output.

Section 2: This section shows an isolation stage. A 5V_SW input is connected to the input of a BC846BWT1G transistor (Q601B) through a 1M resistor (R628). The transistor's output is connected to a 1K resistor (R672) and then to the non-inverting input of an MCP6001T op-amp (U606A). The op-amp's output is connected to a 100nF capacitor (C621) and then to a 5V_BUF output.

Section 3: This section shows a voltage mirror stage. The 5V_BUF output is connected to the VDD of an MCP6001T op-amp (U606A) through a 3R3 resistor (R675). The op-amp's output is connected to a 4K7 resistor (R674) and then to a 5V_BUF output.

The circuit also includes a 5V input, a 5V_SW input, and a 5V_BUF output.

3V3 Regulator

The diagram shows a 3V3 Regulator circuit. The input is 5V, which passes through capacitors C600 (100N) and C611 (10U) to the IN pin (pin 2) of the LP3982ILD-ADJ IC (U600). A 10K resistor (R600) is connected between the IN pin and the SHDN pin (pin 7). The SHDN pin is also connected to GND. The IC is configured as an adjustable regulator with the following connections:

- OUT1 (pin 1) and OUT2 (pin 4) are connected together and to the 3V3 output.
- SET (pin 5) is connected to GND through a 180K resistor (R601).
- FAULT (pin 8) is connected to GND through a 110K resistor (R602).
- CC (pin 6) is connected to GND through a 33N capacitor (C602).
- GND (pin 3) and GND_HEAT (pin 9) are connected to GND.

The output is 3V3, with a 10U capacitor (C607) connected to GND. A temperature node TPJ600 is also indicated. Below the circuit, there are three measurement points labeled M1, M2, and M3, each represented by a blue circle with a red arrow pointing to GND.

Power Supply for Analog Switches

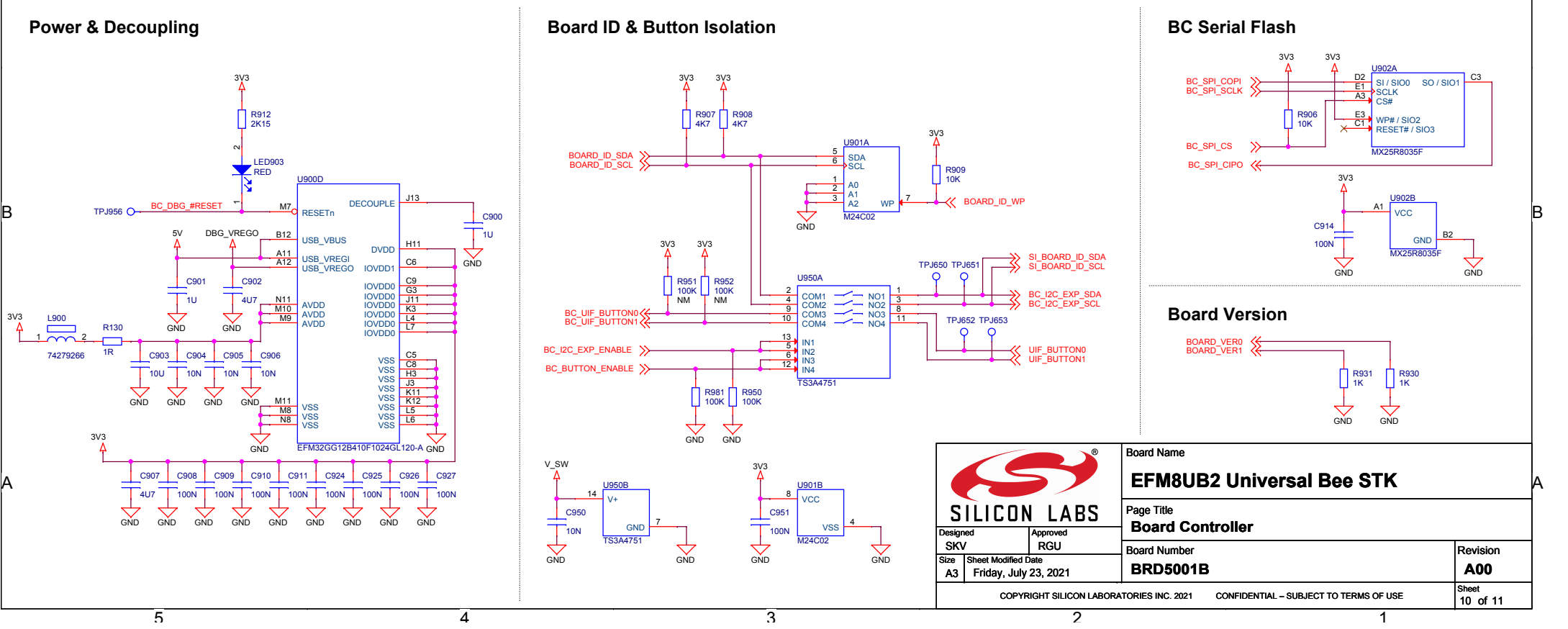
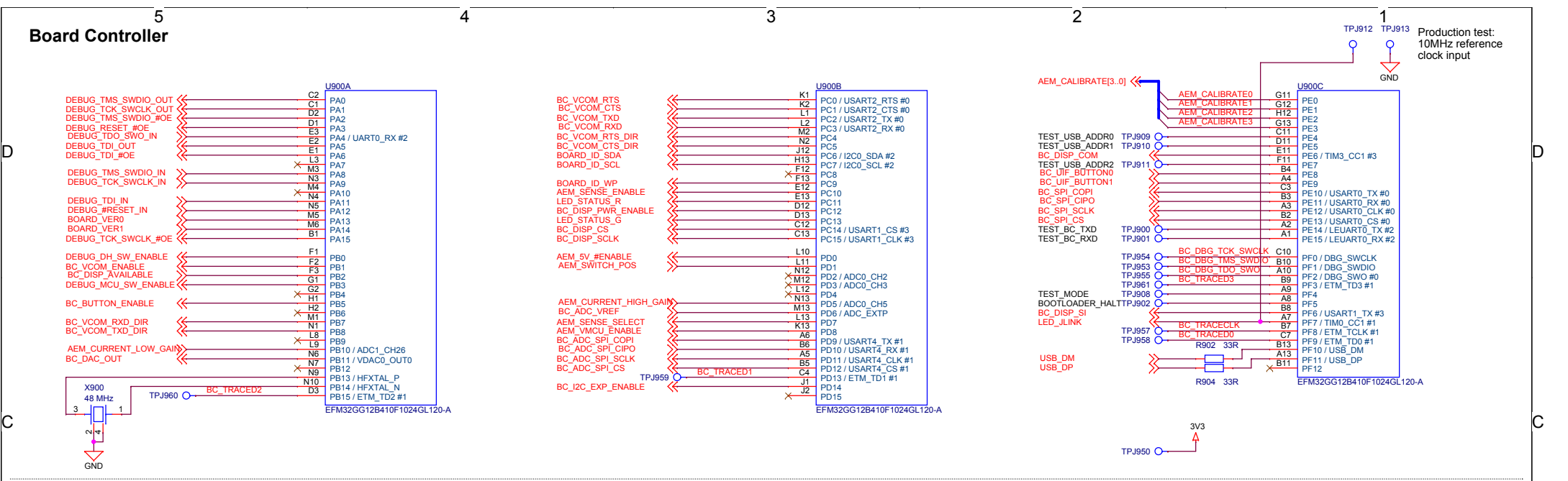
Analog switches used for isolation are powered by 3V6_SW when the USB cable is connected, otherwise by VMCU.

J-Link USB Cable	PMOS State	NMOS State	V_SW	VMCU_SENSE
Connected	Off	On	3.6V	VMCU
Disconnected	On	Off	VMCU	Isolated

TLV70536 Voltage Detector Circuit

Power Supply for Analog Switches

 SILICON LABS		Board Name	
		EFM8UB2 Universal Bee STK	
Designed SKV		Page Title	
		Power	
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		Sheet 9 of 11	





SILICON LABS

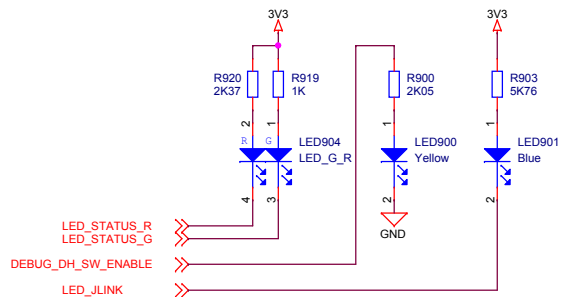
Designed SKV Approved RGU

Size A3 Sheet Modified Date Friday, July 23, 2021

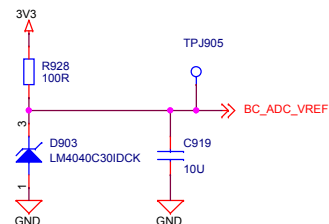
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Board Name	
EFM8UB2 Universal Bee STK	
Page Title	
Board Controller	
Board Number	Revision
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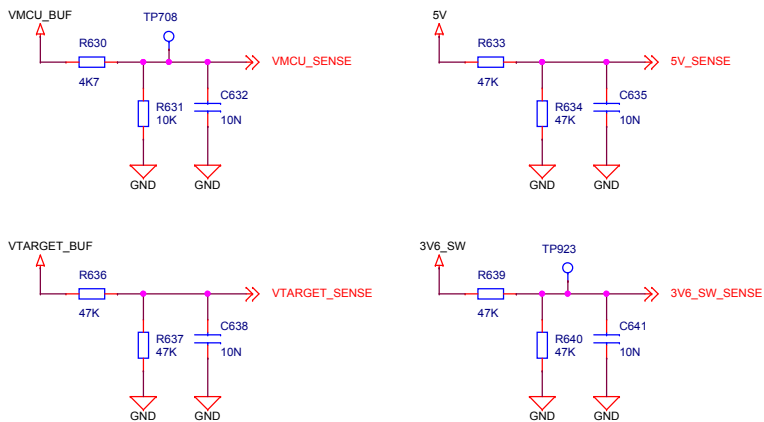
Indicator LEDs



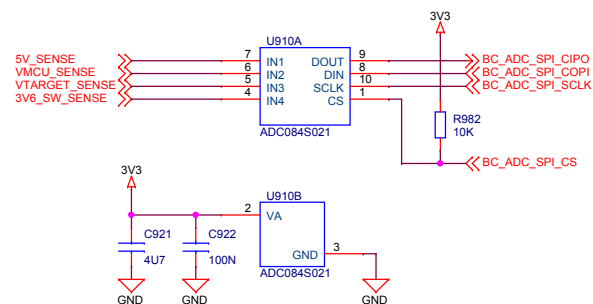
BC ADC Reference



BC Voltage Sense



BC Voltage Sense ADC



		Board Name	
		EFM8UB2 Universal Bee STK	
Designed SKV		Page Title	
Size A3		Board Controller Misc	
Sheet Modified Date Friday, July 23, 2021		Board Number	Revision
		BRD5001B	A00
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