



EFM8SB2 Sleepy Bee STK	
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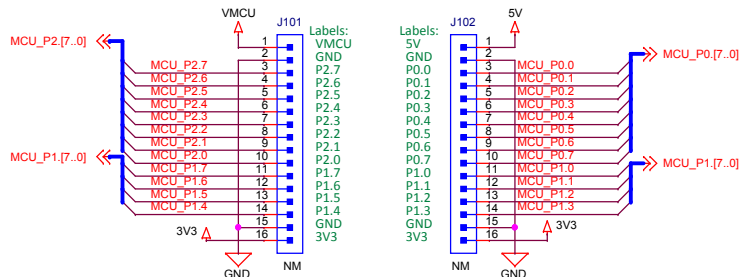
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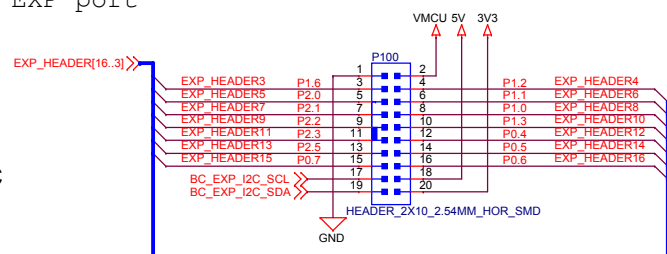
Revision History	
Rev.	Description
A00	Initial release for production.
A01	Removed ST1 and J103 from the BOM.
A02	Updated PCB revision.
A03	Updated EFM8 to Rev B. Un-mounted D801.

/ STK			
		Schematic Title	
SILICON LABS		EFM8SB2 Sleepy Bee STK	
Designed: MRW		Page Title	
Approved: JNO		Title Page	
Size: A3	BOM Doc No:	Document number	Revision
		BRD5100A	A03
Design Created Date: Wednesday, December 03, 2008		Sheet Created Date: Thursday, May 15, 2014	Sheet Modified Date: Tuesday, December 19, 2017
		Sheet 1 of 11	

Breakout Connections



EXP port



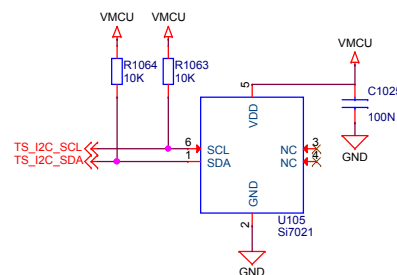
EXP-Header Functionality

** Indicates potential STK hardware conflicts

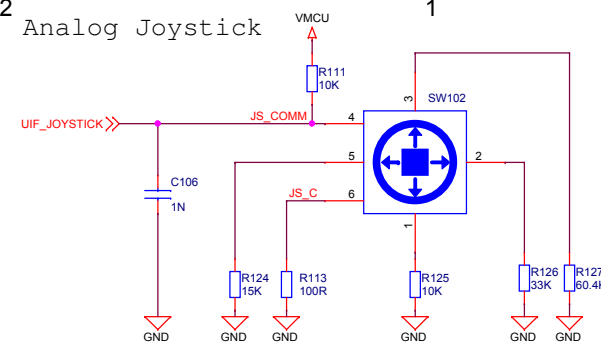
1	GND			
3	P1.6		CMP_P7/ADC0.14	** STK LED0
5	P2.0		CMP_P8/ADC0.16	** STK LED1
7	P2.1		CMP_P9/ADC0.17	** STK LED2
9	P2.2		CMP_P10/ADC0.18	
11	P2.3		CMP_P11/ADC0.19	
13	P2.5		CMP_P12/ADC0.21	
15	P0.7		CMP_P13/ADC0.7	
17			Reserved for EXP Board Identification	
19			Reserved for EXP Board Identification	

2	VMCU			
4	P1.2	SPI0_MOSI	CMP_P5/ADC0.10	
6	P1.1	SPI0_MISO	CMP_P4/ADC0.9	
8	P1.0	SPI0_SCK	CMP_P3/ADC0.8	
10	P1.3	SPI0_NSS	CMP_P2/ADC0.11	
12	P0.4	UART0_TX	CMP_P1/ADC0.4	
14	P0.5	UART0_RX	CMP_P0/ADC0.5	
16	P0.6	I2C0_SDA	CMP_P0/ADC0.6	
18	5V			
20	3V3			

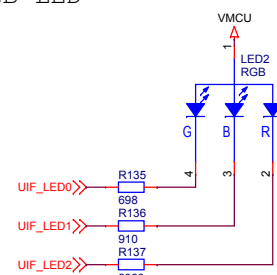
Temperature & Relative Humidity Sensor



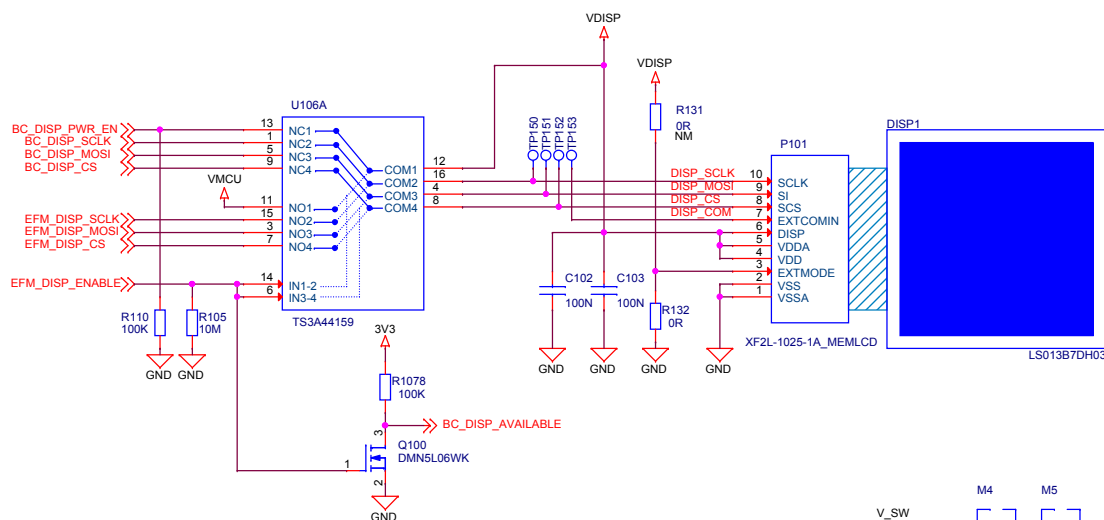
Analog Joystick

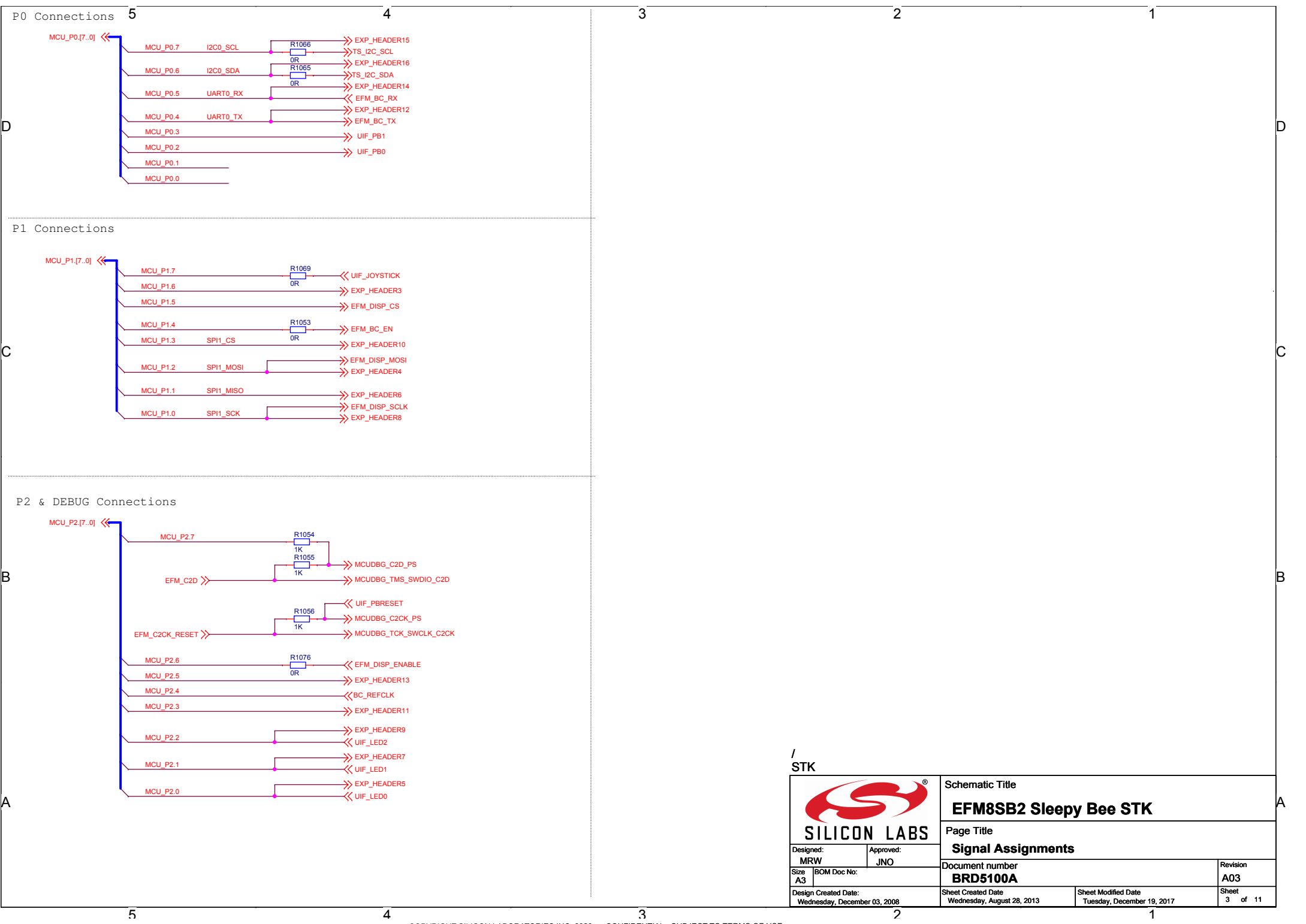


RGB LED



Memory LCD-TFT Display & Multiplexer







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Designed:
MRW

Size
A3

Design Created Date:
Wednesday, December 03, 2008

Approved:
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Schematic Title
EFM8SB2 Sleepy Bee STK

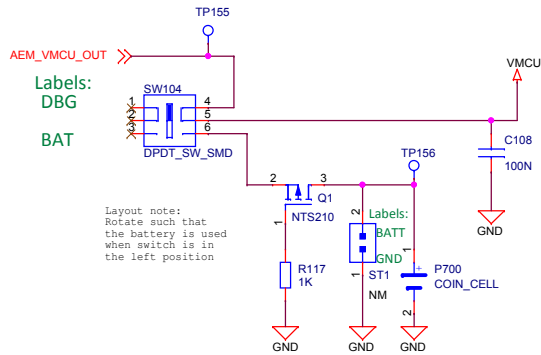
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Signal Assignments

Document number BRD5100A	Revision A03
Sheet Created Date Wednesday, August 28, 2013	Sheet Modified Date Tuesday, December 19, 2017
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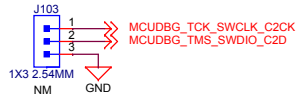
STK

Power Switch

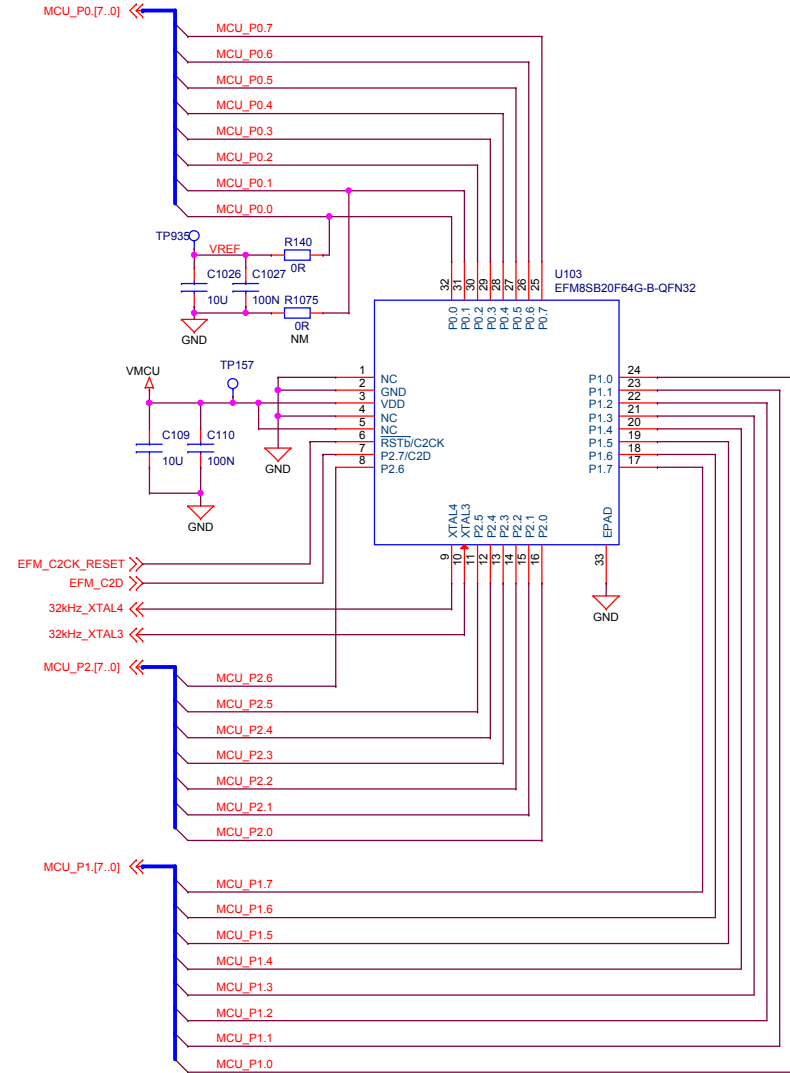
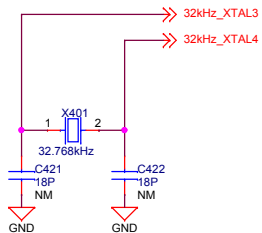
SWITCH POS	MODE DESCRIPTION
DBG	AEM Enabled, VMCU sourced from external 3.3V LDO powered by BC USB 5V supply
BAT	AEM Disabled, VMCU sourced from external coin-cell battery or external power supply



C2 Debug Header

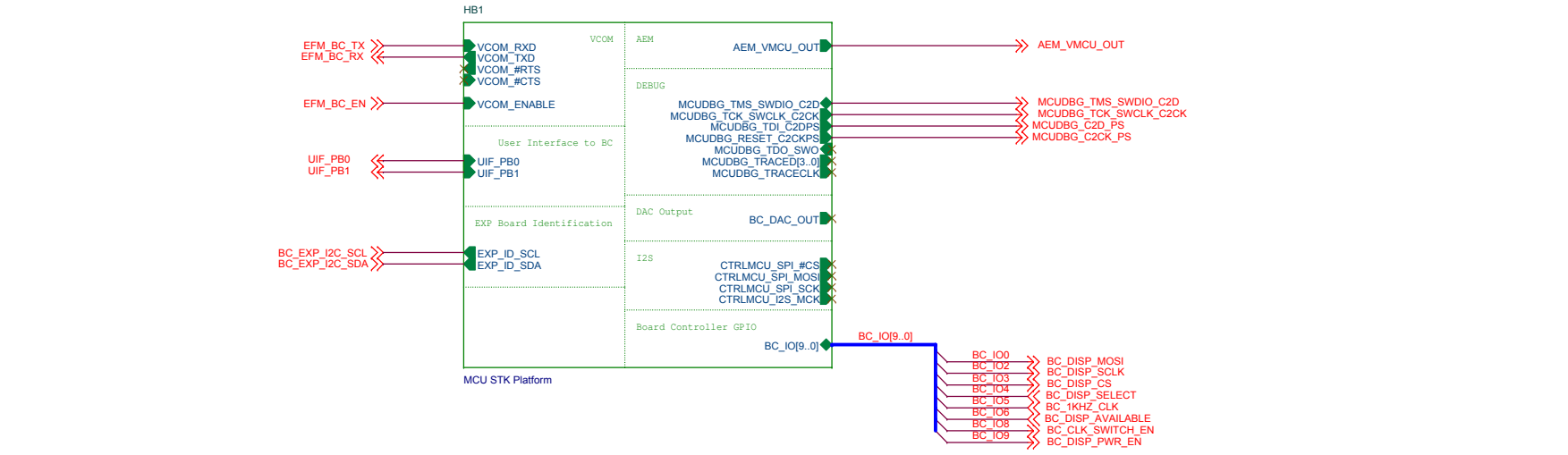


Low Frequency Clock

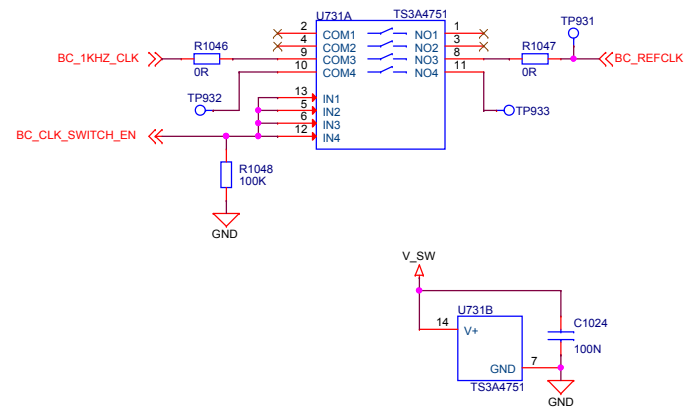


/
STK

		Schematic Title	
		EFM8SB2 Sleepy Bee STK	
Designed: MRW Size: A3		Page Title	
		EFM8 I/O & Power	
BOM Doc No:		Document number	Revision
Design Created Date:		BRD5100A	A03
Wednesday, December 03, 2008		Sheet Created Date	Sheet Modified Date
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Analog Switch





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Designed: **MRW**

Size: **A3**

Design Created Date: **Wednesday, December 03, 2008**

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Sheet Created Date: **Thursday, May 15, 2014**

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Schematic Title

EFM8SB2 Sleepy Bee STK

Page Title

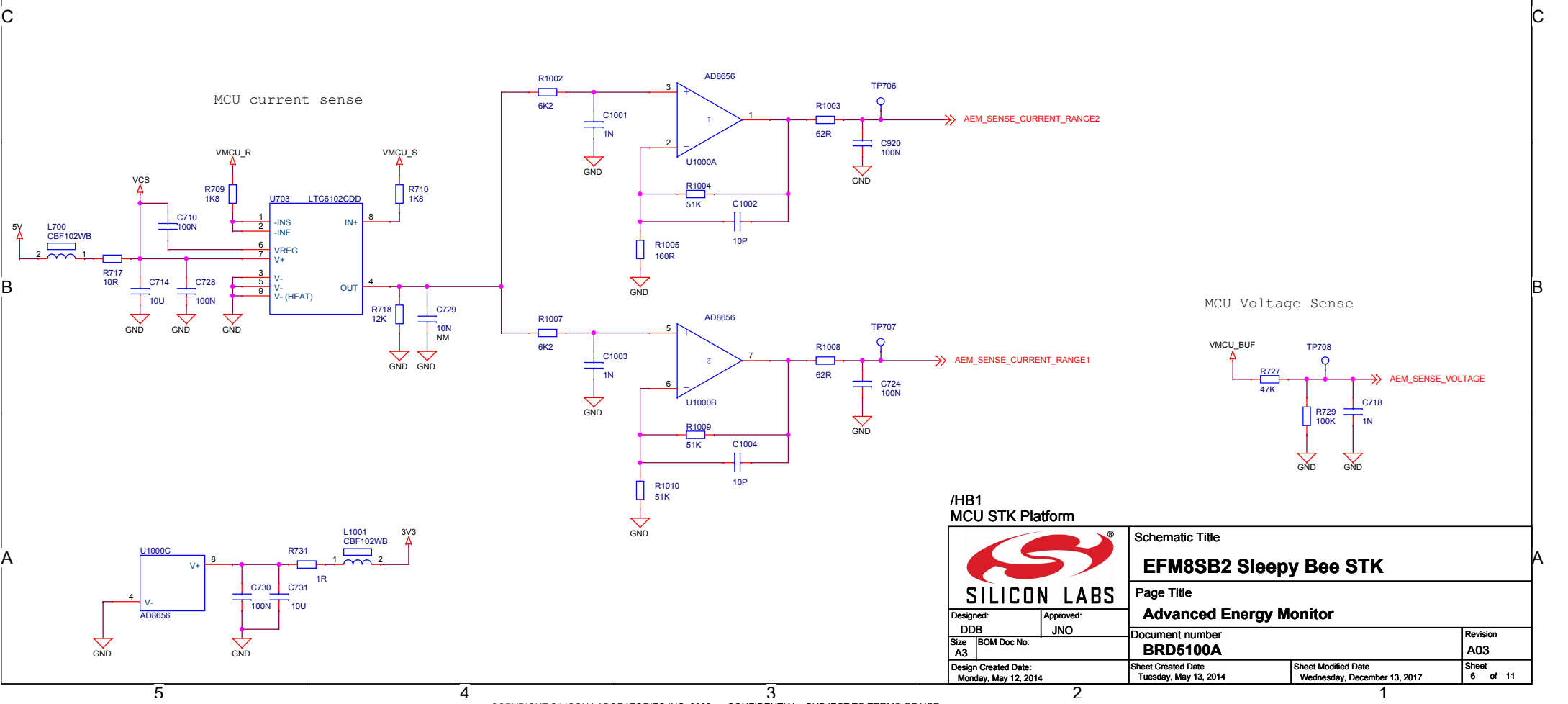
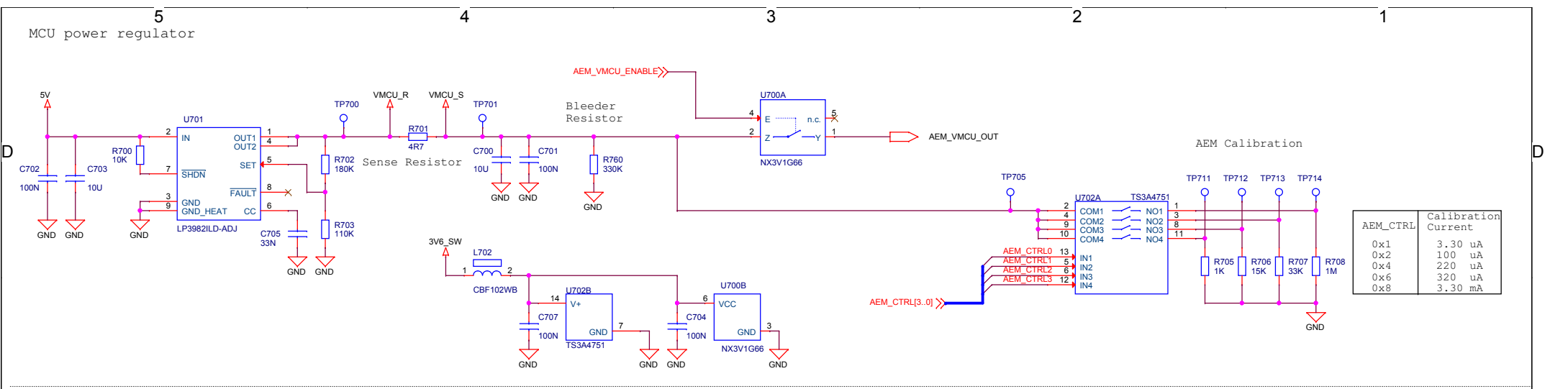
STK Common Platform

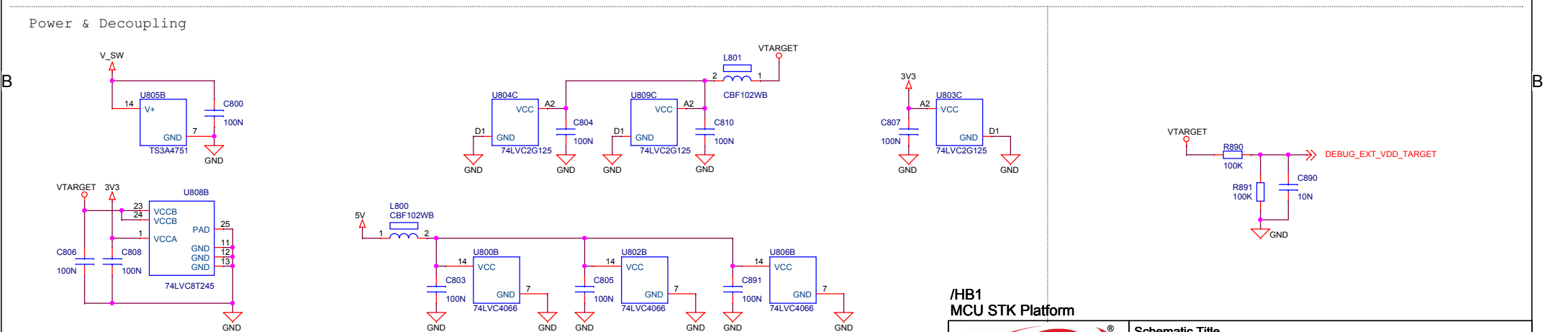
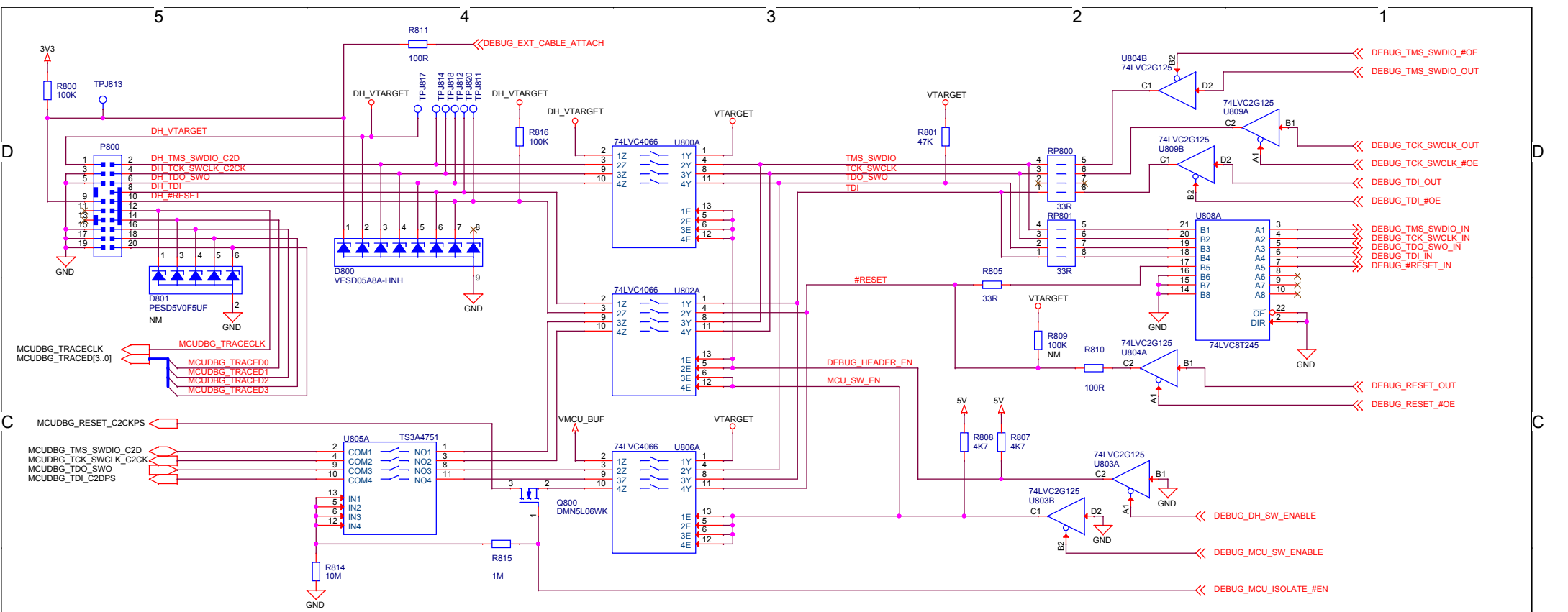
Document number

BRD5100A

Revision

A03





Mode	DEBUG_MCU_SW_ENABLE	DEBUG_DH_SW_ENABLE	DEBUG_BUF_#OE	ISOLATE_#EN	DH_VTARGET	VTARGET
Debug Out	0	1	0	0	External voltage	External voltage
MCU Debug	1	0	0	1	Disconnected	VMCU
Debug In	1	1	1	1	VMCU	VMCU
Debug Off	1	1	1	0	-	-



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Designed: DDB
Size: A3
BOM Doc No: JNO
Design Created Date: Monday, May 12, 2014

Schematic Title
EFM8SB2 Sleepy Bee STK

Page Title
Debug Interface

Document number
BRD5100A

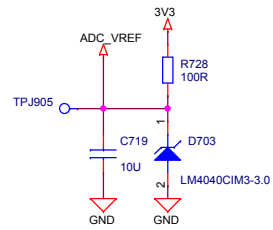
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Sheet Modified Date
Wednesday, December 13, 2017

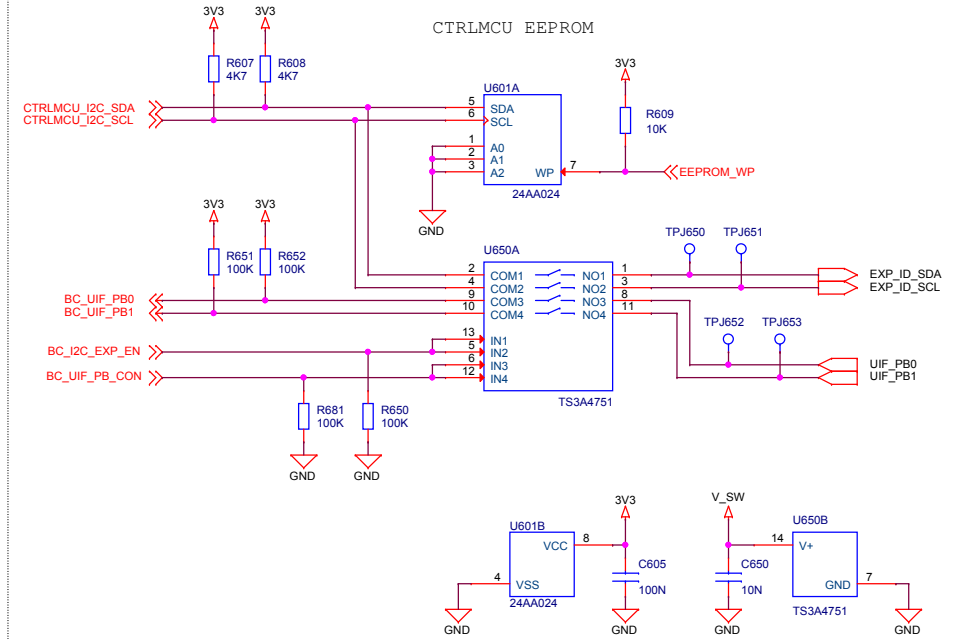
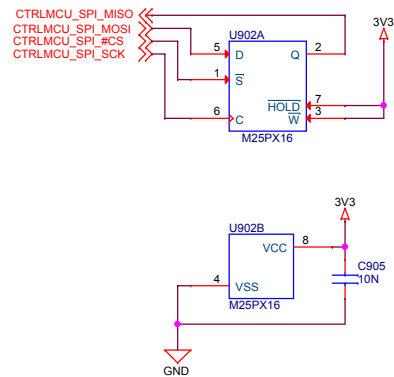
Revision
A03

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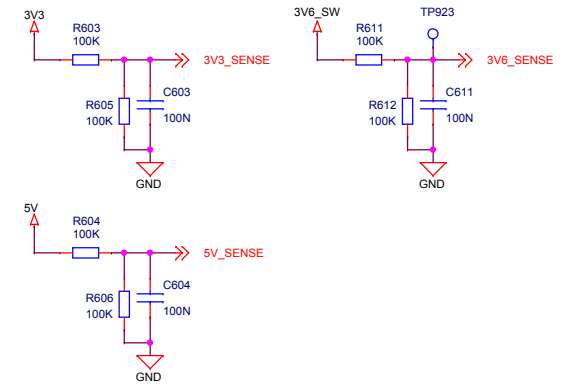
ADC reference voltage



CTRLMCU SERIAL FLASH



POWER SENSE



/HB1/CMCU1
Control MCU

		Schematic Title	
		EFM8SB2 Sleepy Bee STK	
Designed: ANB		Page Title	
Approved: JNO		Control MCU Misc.	
Size A3	BOM Doc No:	Document number BRD5100A	Revision A03
Design Created Date: Monday, May 12, 2014		Sheet Created Date Wednesday, February 11, 2015	Sheet Modified Date Tuesday, December 19, 2017
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