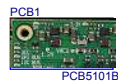




EFM8SB1 Sleepy Bee STK

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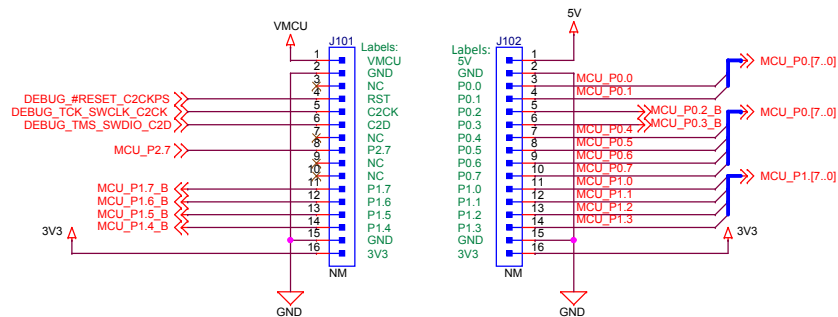
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Revision History

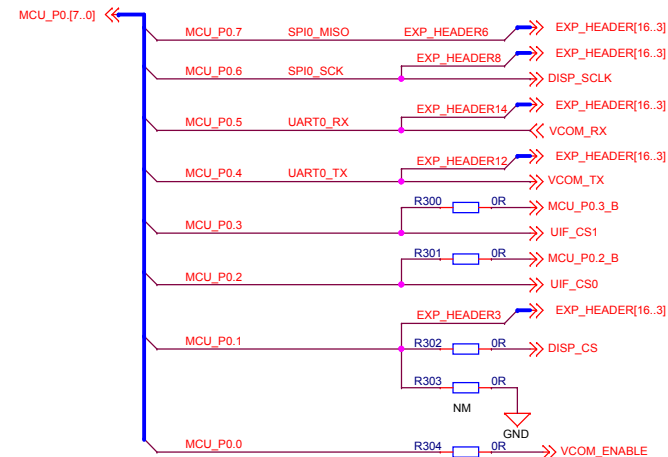
Rev.	Description
A01	Update to new STK platform
A02	User Push buttons connection updated

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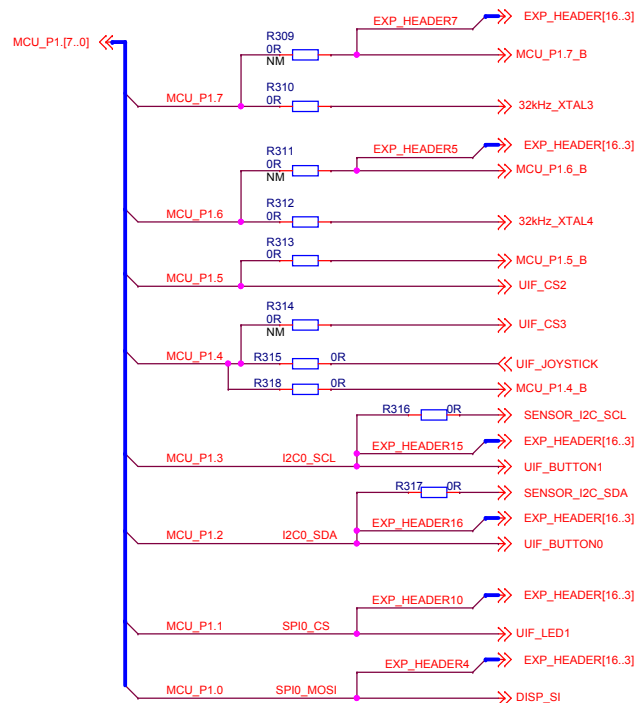
Breakout Connections



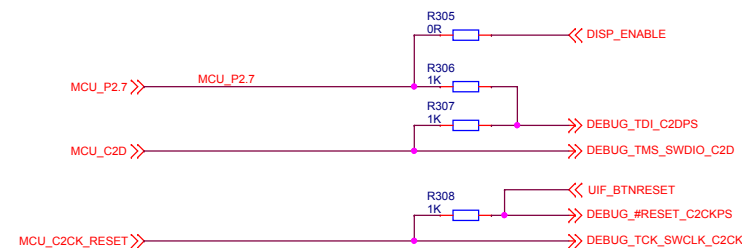
P0 Connections



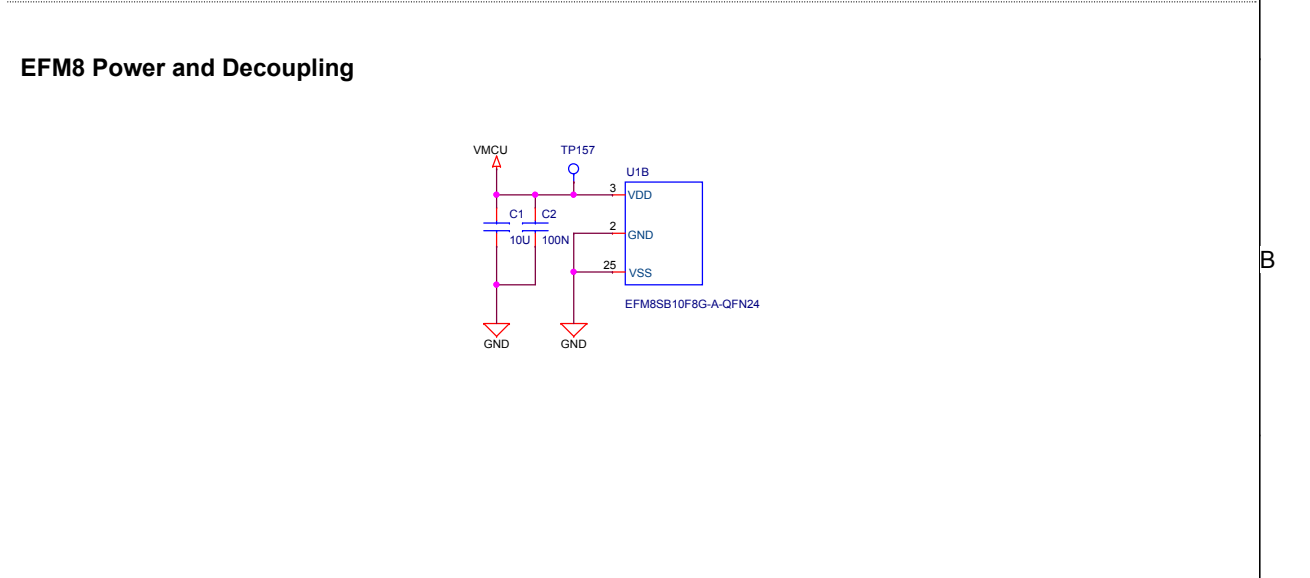
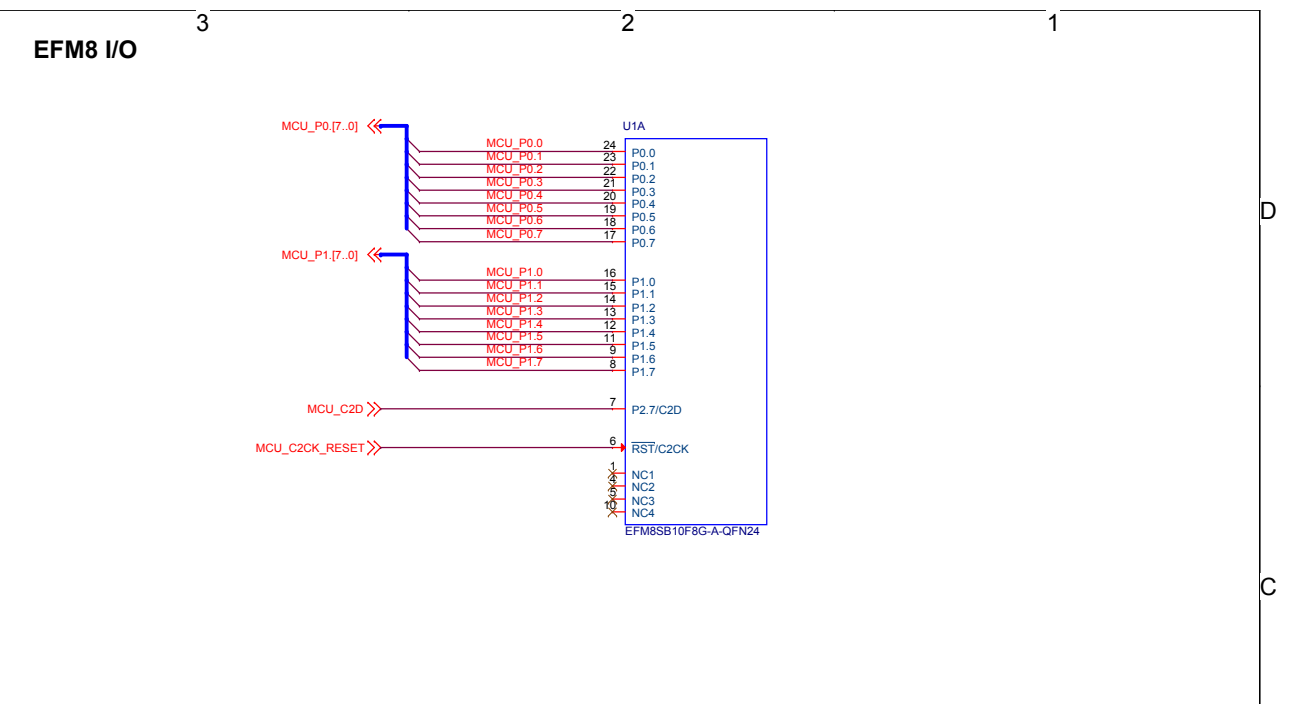
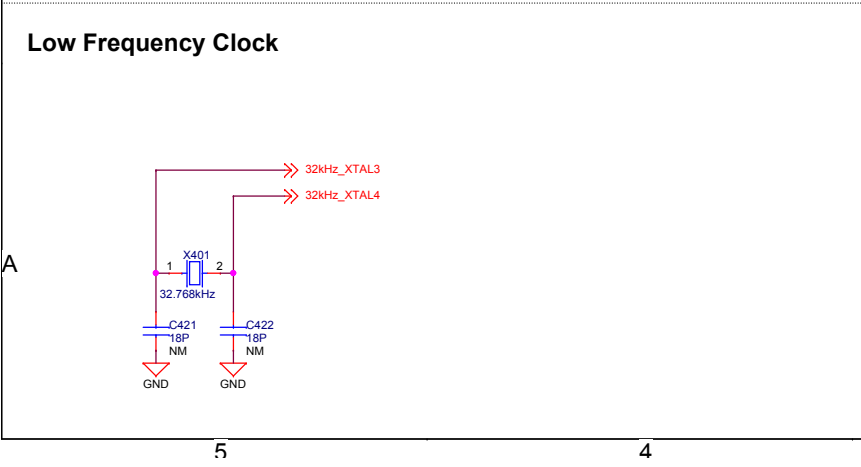
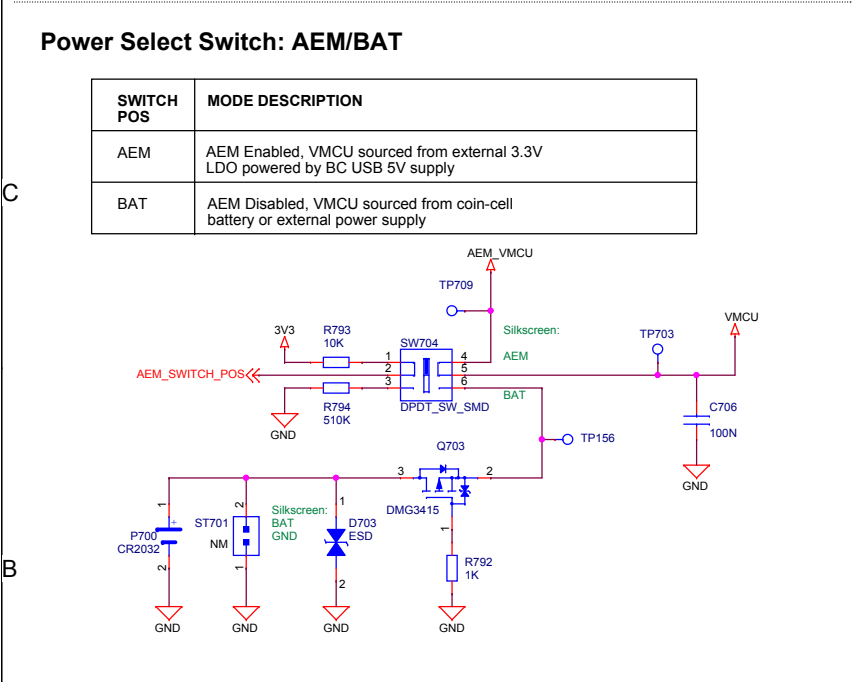
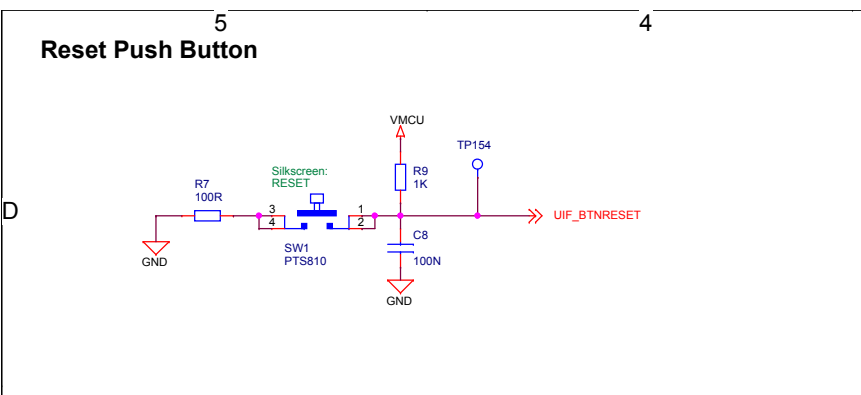
P1 Connections



P2 & Debug Connections

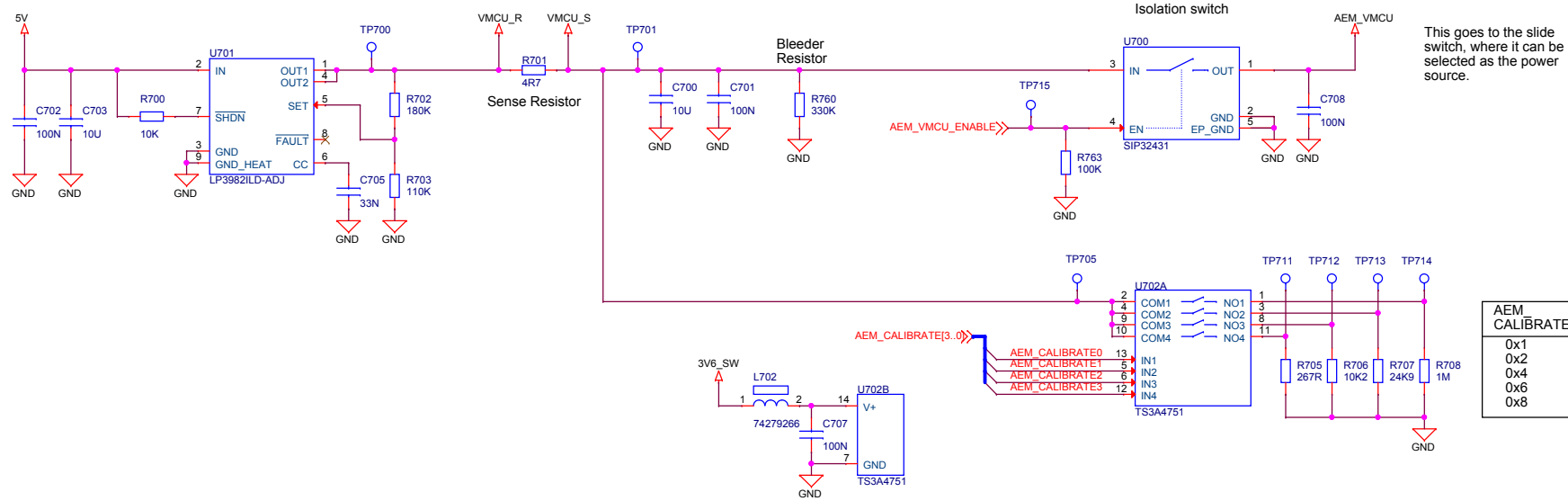


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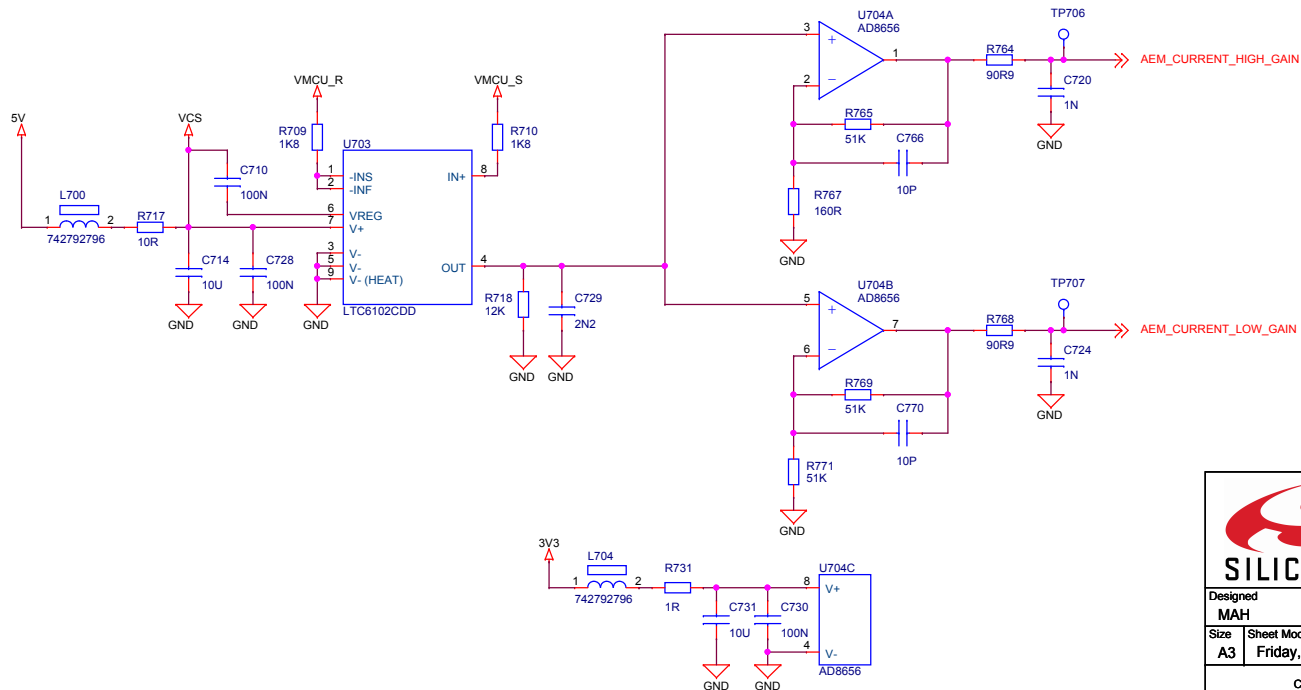


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MCU Power Regulator

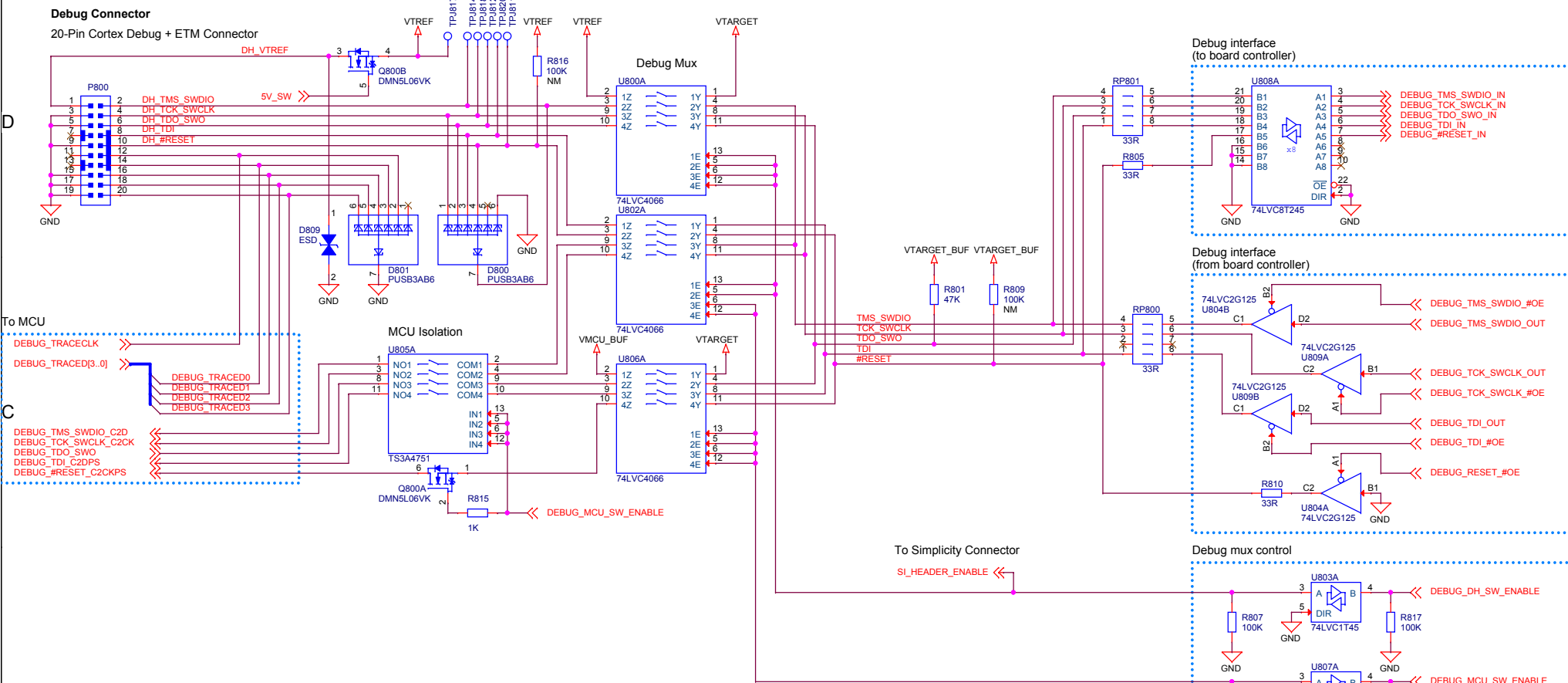


Advanced Energy Monitoring

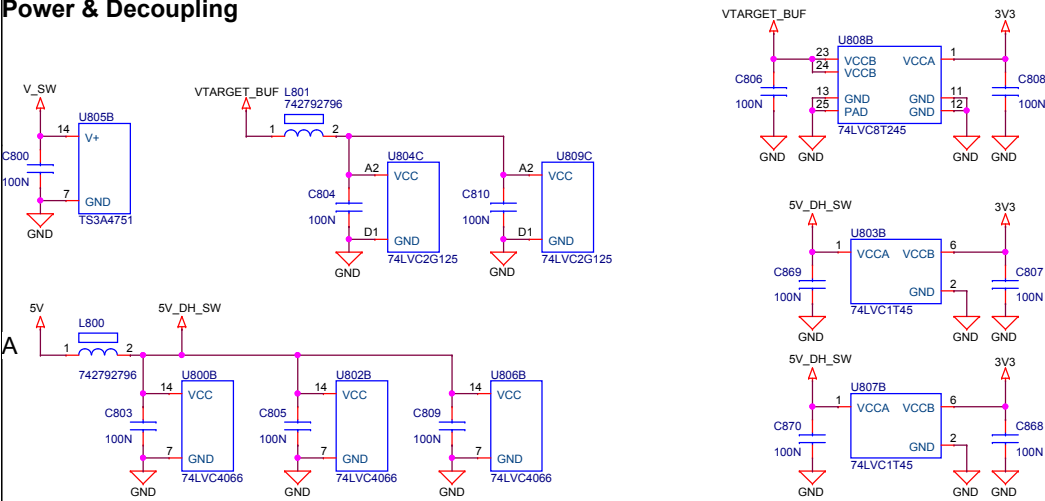


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Debug Mux



Power & Decoupling



Debug Mode	DH_SW_ENABLE	MCU_SW_ENABLE	Debug Mode	VTARGET Source	VTREF Source
MCU	0	1	MCU	VMCU	None
Debug Out	1	0	Debug Out	VTREF (EXT)	External
Debug In	1	1	Debug In	VMCU	VMCU_BUF
Debug Off	0	0	Debug Off	None	None



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Debug Interface

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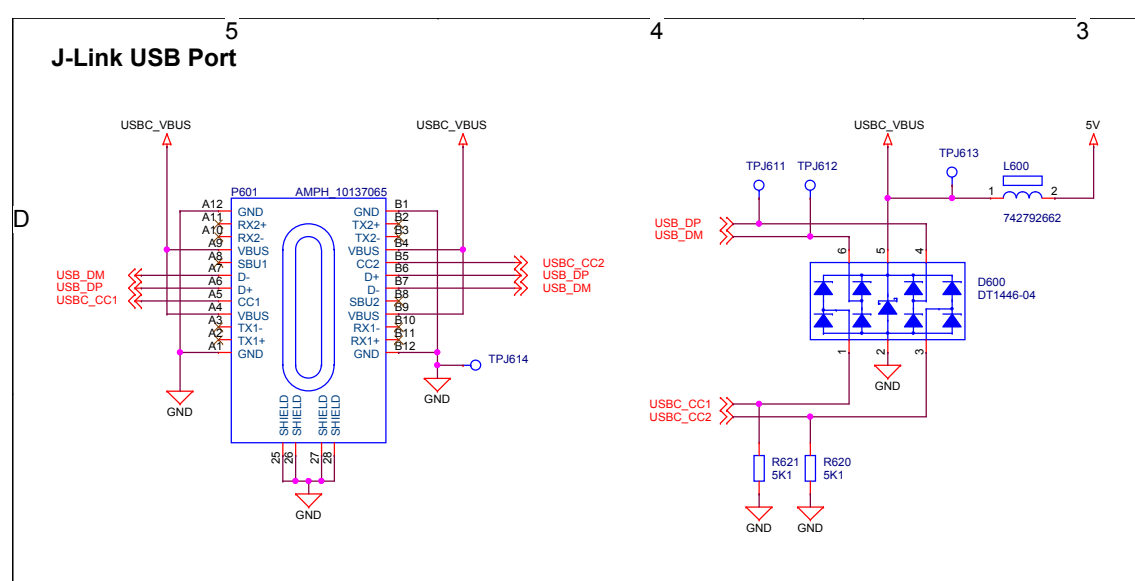
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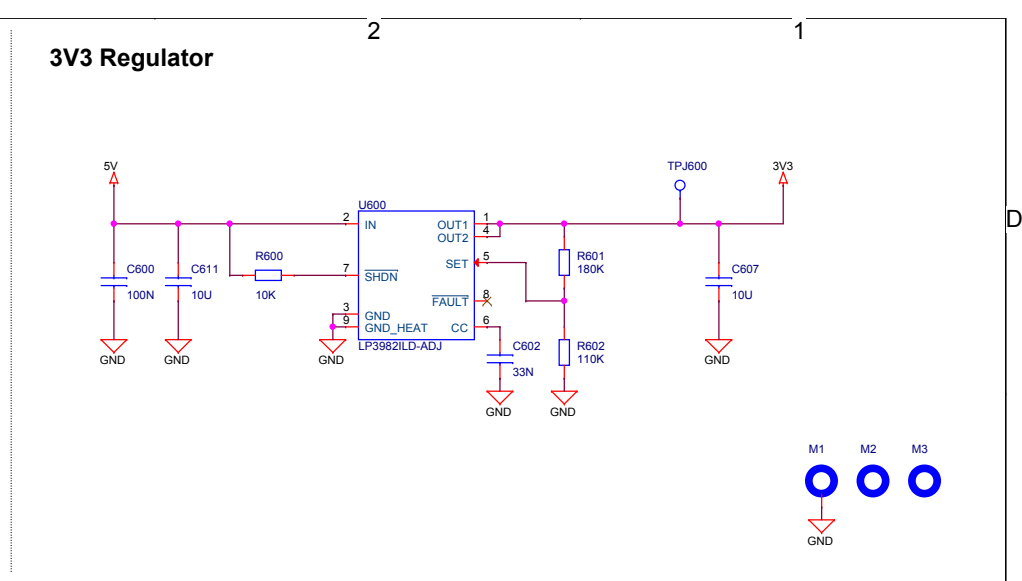
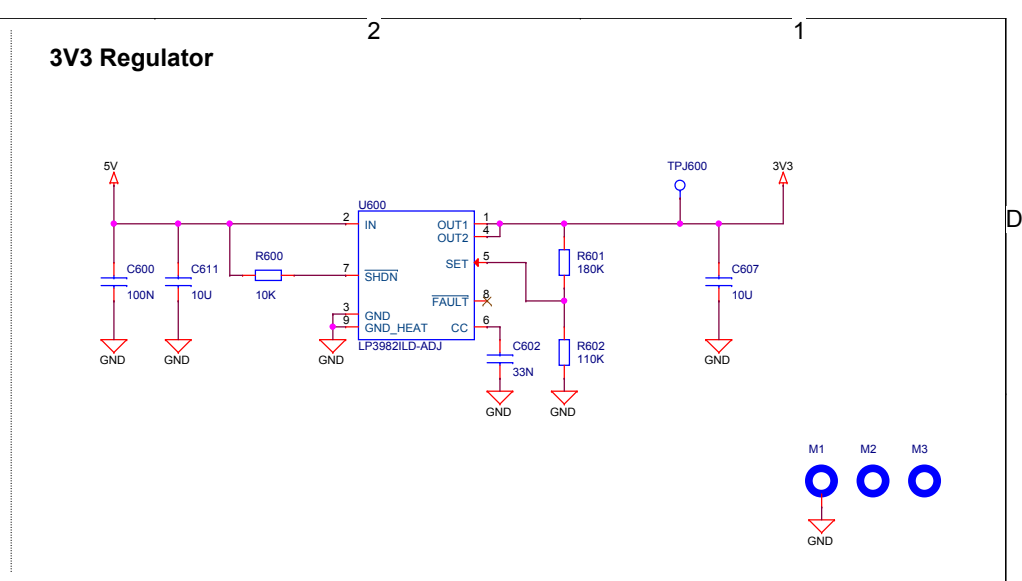
J-Link USB Port

The schematic diagram illustrates the J-Link USB Port. It shows the connection between the USB connector (D600 DT1446-04) and the J-Link hardware (P601, AMPH 10137065). The USB connector is labeled with pins 1 through 12. The J-Link hardware is labeled with pins A1 through A12, B1 through B12, and SHIELD. The connections are color-coded: red for USB_VBUS, blue for USB_DP, green for USB_DM, and black for GND. The USB connector is labeled with pins 1 through 12. The J-Link hardware is labeled with pins A1 through A12, B1 through B12, and SHIELD. The USB connector is labeled with pins 1 through 12. The J-Link hardware is labeled with pins A1 through A12, B1 through B12, and SHIELD.



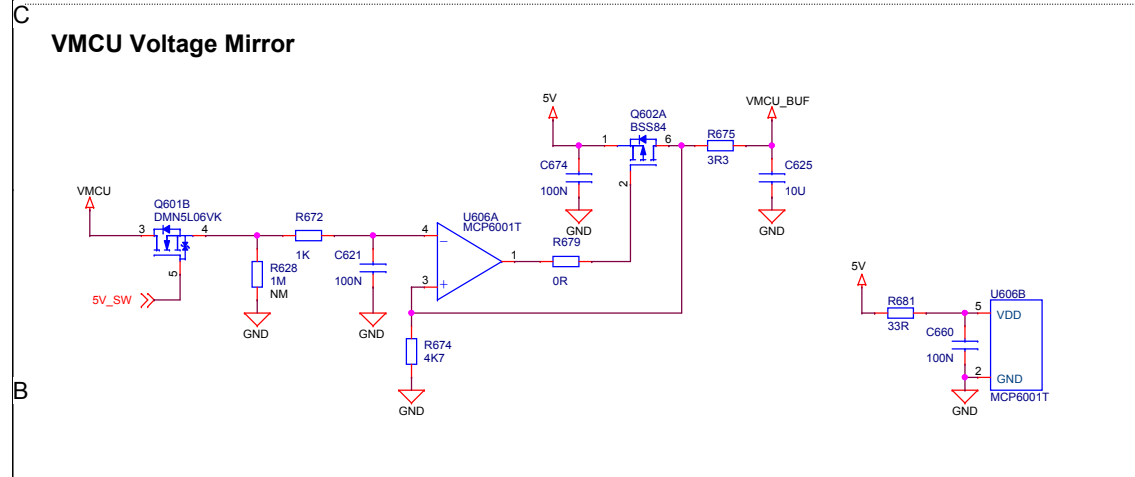
3V3 Regulator

The schematic diagram illustrates a 3V3 Regulator circuit. The input is 5V, which is decoupled by capacitors C600 (100N) and C611 (10U). The input voltage is then regulated by the U600 LP3982ILDR-ADJ regulator. The regulator's IN pin (pin 2) is connected to the 5V input through a 10K resistor (R600). The SHDN pin (pin 7) is connected to GND. The GND_HEAT pin (pin 3) is also connected to GND. The OUT1 pin (pin 1) provides the 3V3 output. The SET pin (pin 5) is connected to the 3V3 output through a 180K resistor (R601). The FAULT pin (pin 8) is connected to GND. The CC pin (pin 6) is connected to GND through a 33nF capacitor (C602). The 3V3 output is decoupled by capacitor C607 (10U). A temperature sensor (TPJ600) is connected to the 3V3 output. Three motor pins (M1, M2, M3) are shown at the bottom, connected to GND.

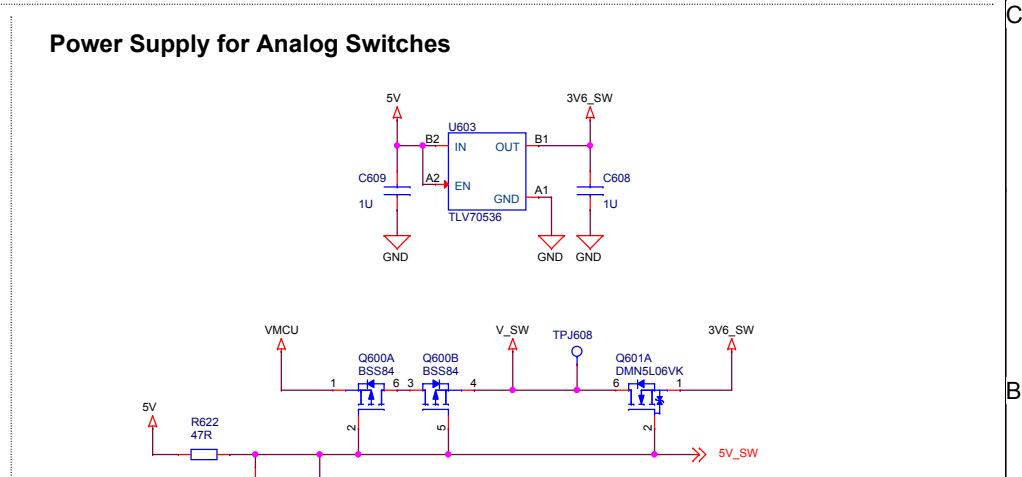


VMCU Voltage Mirror

The schematic diagram illustrates the VMCU Voltage Mirror circuit. It features two operational amplifiers, U606A MCP6001T and U606B MCP6001T, and two MOSFETs, Q601B DMN5L06VK and Q602A BSS84. The circuit is powered by a 5V supply and includes various passive components like resistors (R672, R674, R675, R681) and capacitors (C621, C625, C660, C674). The output of the first stage is connected to the gate of the MOSFET Q601B, which then drives the VMCU signal. The second stage, a buffer, drives the VMCU_BUF signal. The circuit is designed to mirror the VMCU voltage to the VMCU_BUF signal.



Power Supply for Analog Switches



The diagram shows the power supply section of the EFM8SB1 Sleepy Bee STK. It includes a 3V6 voltage regulator, a 10K resistor (R623), and a 1N diode (C610). The 3V6 is connected to the V_SW pin of the EFM8SB1. The 1N diode is connected to the VMCU pin of the EFM8SB1. The 10K resistor is connected to GND. The 3V6 is connected to GND. The 1N diode is connected to GND. The EFM8SB1 is connected to a USB cable.

J-Link USB Cable	Q600 State	Q601A State	V_SW	VMCU_SENSE
Connected	OFF	ON	3.6V	VMCU
Disconnected	ON	OFF	VMCU	Isolated

Isolation switches are powered by 3V6_SW when the USB cable is connected, otherwise by VMCU.



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EFM8SB1 Sleepy Bee STK

Page Title

Power

Board Number

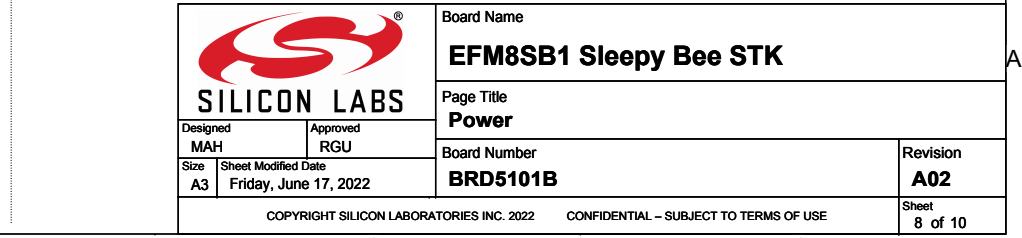
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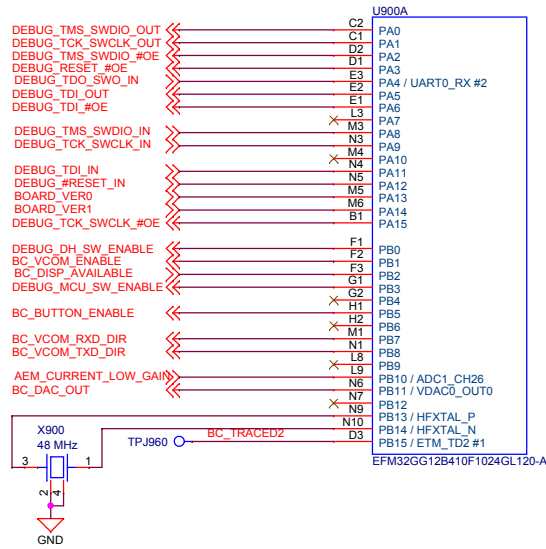
Board Controller

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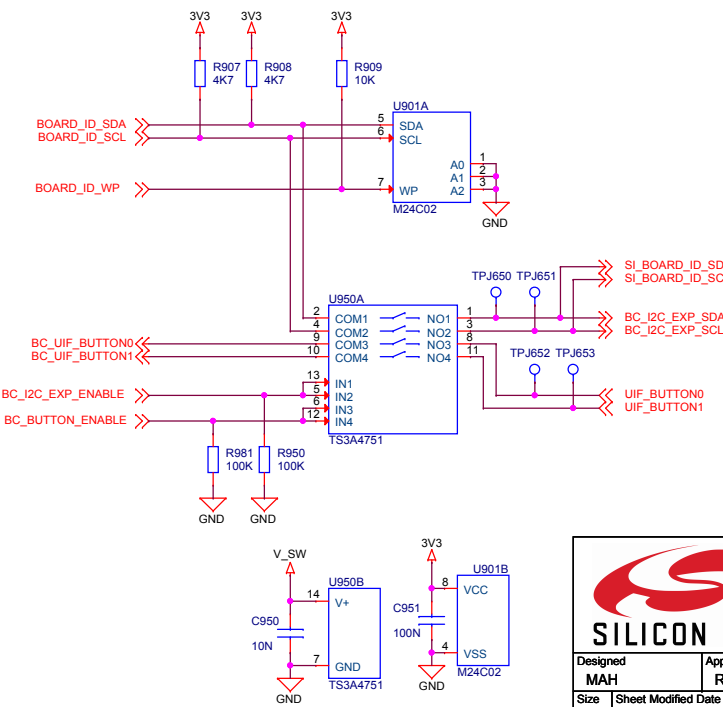
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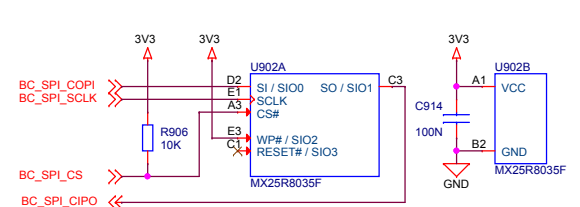
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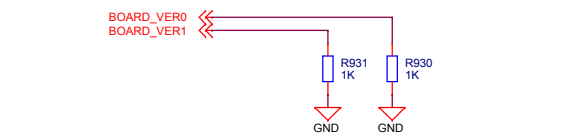
Board ID & Button Isolation



BC Serial Flash

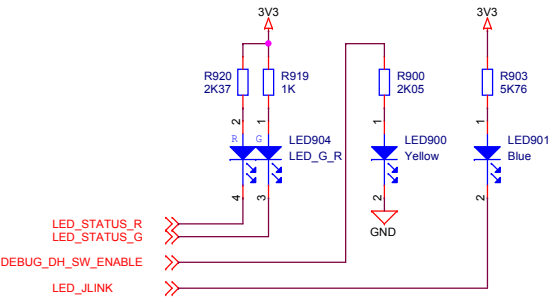


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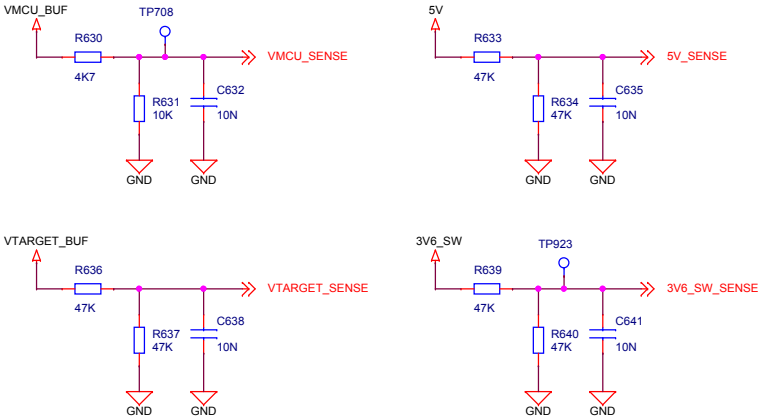


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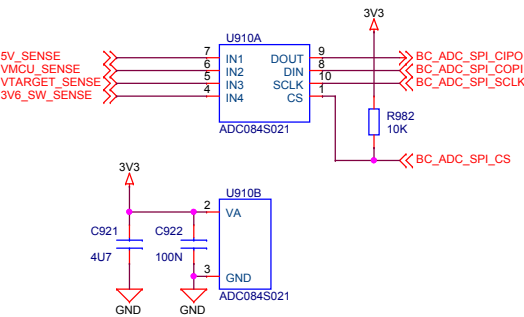
Indicator LEDs



BC Voltage Sense



BC Voltage Sense ADC



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