



EFM8BB1 Busy Bee STK

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Revision History

Rev.	Description
A00	Initial version released for production.
A01	Minor updates to design. Updated sine wave generator and new PCB.
A02	Updated PCB revision.

STK

 SILICON LABS		Schematic Title EFM8BB1 Busy Bee Starter Kit	
Designed: MRW		Page Title Title Page	
Size A3	BOM Doc No:	Document number BRD5200A	Revision A02
Design Created Date: Wednesday, December 03, 2008		Sheet Created Date Thursday, May 15, 2014	Sheet Modified Date Monday, March 23, 2015
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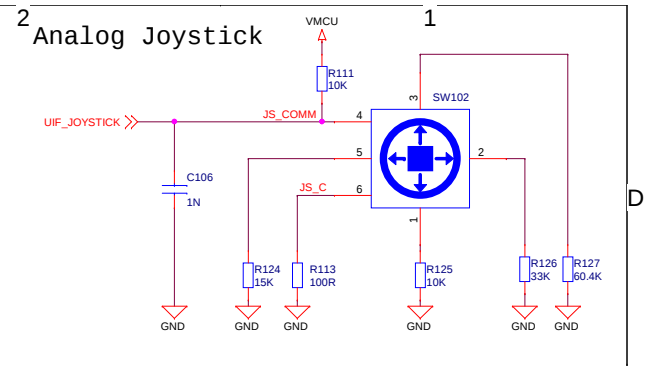
PCB5200

The image contains three circuit diagrams labeled 1, 2, and 3.

Diagram 1: Breakout Connections shows two pin headers, J101 and J102. J101 is connected to VMCU and GND. J102 is connected to 5V, GND, and 3V3. The diagrams show the mapping of MCU pins to the breakout board pins.

Diagram 2: RGB LED shows the connection of the RGB LED pins (G, B, R) to the breakout board pins. The LED is connected to VMCU and GND. The diagram also shows the connection of the LED pins to the breakout board pins.

Diagram 3: Analog Joystick shows the connection of the joystick pins (JS_C, JS_COMM, JS_C) to the breakout board pins. The joystick is connected to VMCU and GND. The diagram also shows the connection of the joystick pins to the breakout board pins.



EXP port

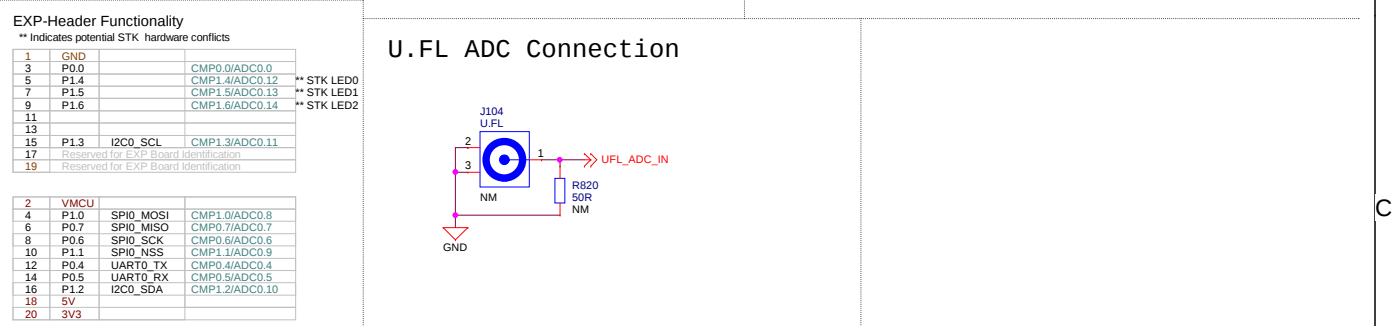
EXP-Header Functionality

** Indicates potential STK hardware conflicts

Pin	Function	STK Pin
1	GND	
3	P0.0	
5	P1.4	CMP0.0/ADC0.2 ** STK LED0
7	P1.5	CMP1.4/ADC0.12 ** STK LED1
9	P1.6	CMP1.5/ADC0.13 ** STK LED2
11		
13		
15	P1.3 I2C0_SCL	CMP1.6/ADC0.14
17	Reserved for EXP Board Identification	
19	Reserved for EXP Board Identification	

Pin	Function	STK Pin
2	VMCU	
4	P1.0	CMP0.0/ADC0.0
6	P0.7	SPI0_MISO CMP0.7/ADC0.7
8	P0.6	SPI0_SCK CMP0.6/ADC0.6
10	P1.1	SPI0_NSS CMP1.1/ADC0.9
12	P0.4	UART0_TX CMP0.4/ADC0.4
14	P0.5	UART0_RX CMP0.5/ADC0.5
16	P1.2	I2C0_SDA CMP1.2/ADC0.10
18	5V	
20	3V3	

U.FL ADC Connection



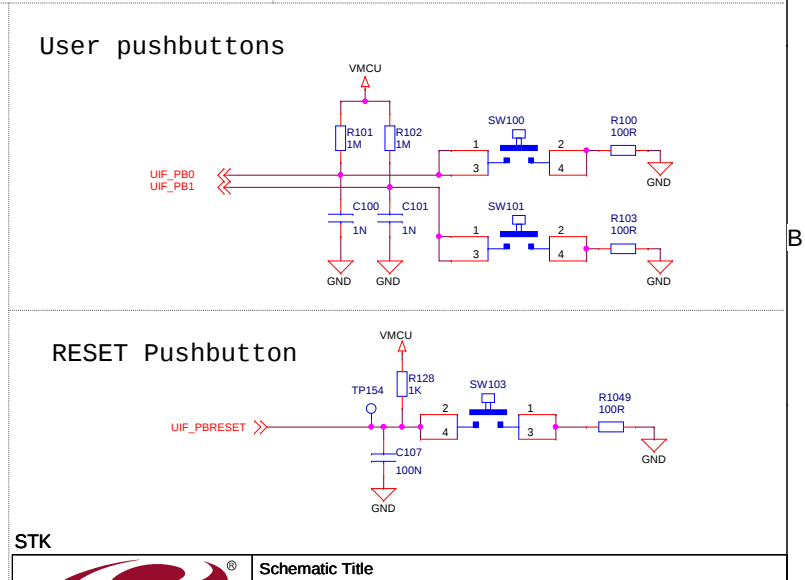
Memory LCD-TFT Display & Multiplexer

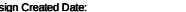
User pushbuttons

RESET Pushbutton

STK

Schematic Title



A The EFM8 always controls ownership of the display using the EFM_DISP_ENABLE signal. <table border="1" data-bbox="185 1476 575 1490"> <thead> <tr> <th data-bbox="185 1476 349 1481">EFM_DISP_ENABLE</th><th data-bbox="349 1476 495 1481">DISP_CTRL</th><th data-bbox="495 1476 575 1481">VDISP</th></tr> </thead> <tbody> <tr> <td data-bbox="185 1481 349 1484">0</td><td data-bbox="349 1481 495 1484">BC</td><td data-bbox="495 1481 575 1484">BC_DISP_PWR_EN</td></tr> <tr> <td data-bbox="185 1484 349 1490">1</td><td data-bbox="349 1484 495 1490">EFM</td><td data-bbox="495 1484 575 1490">VMCU</td></tr> </tbody> </table>	EFM_DISP_ENABLE	DISP_CTRL	VDISP	0	BC	BC_DISP_PWR_EN	1	EFM	VMCU	 <table border="1" data-bbox="1632 1473 2161 1490"> <thead> <tr> <th colspan="2" data-bbox="1632 1473 2161 1476">EFM8BB1 Busy Bee Starter Kit</th></tr> </thead> <tbody> <tr> <td colspan="2" data-bbox="1632 1476 2161 1481">Page Title</td></tr> <tr> <td colspan="2" data-bbox="1632 1481 2161 1484">User Interfaces</td></tr> <tr> <td data-bbox="1632 1484 2063 1490">Document number BRD5200A</td><td data-bbox="2063 1484 2161 1490">Revision A02</td></tr> <tr> <td data-bbox="1632 1490 1839 1493">Sheet Created Date Wednesday, December 03, 2008</td><td data-bbox="1839 1490 2161 1493"> Sheet Modified Date Thursday, February 12, 2015 Sheet 2 of 10 </td></tr> </tbody> </table>	EFM8BB1 Busy Bee Starter Kit		Page Title		User Interfaces		Document number BRD5200A	Revision A02	Sheet Created Date Wednesday, December 03, 2008	Sheet Modified Date Thursday, February 12, 2015 Sheet 2 of 10
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0	BC	BC_DISP_PWR_EN																		
1	EFM	VMCU																		
EFM8BB1 Busy Bee Starter Kit																				
Page Title																				
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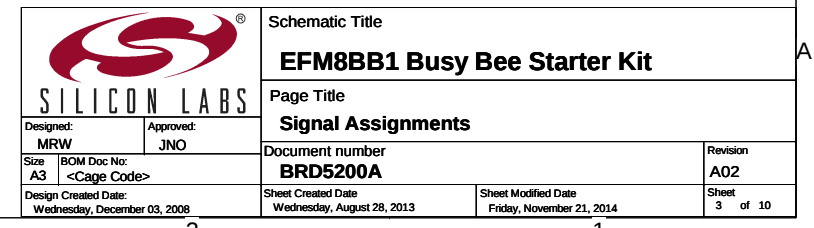
D



B



7



D

C

A



EFM8BB1 Busy Bee Starter Kit

EFM8 I/O

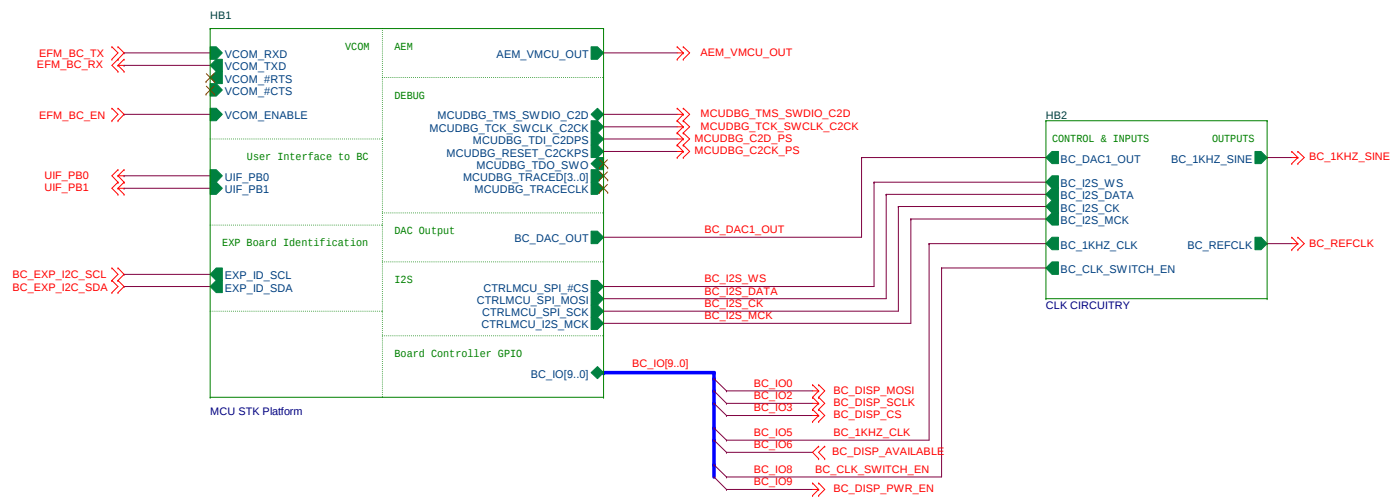
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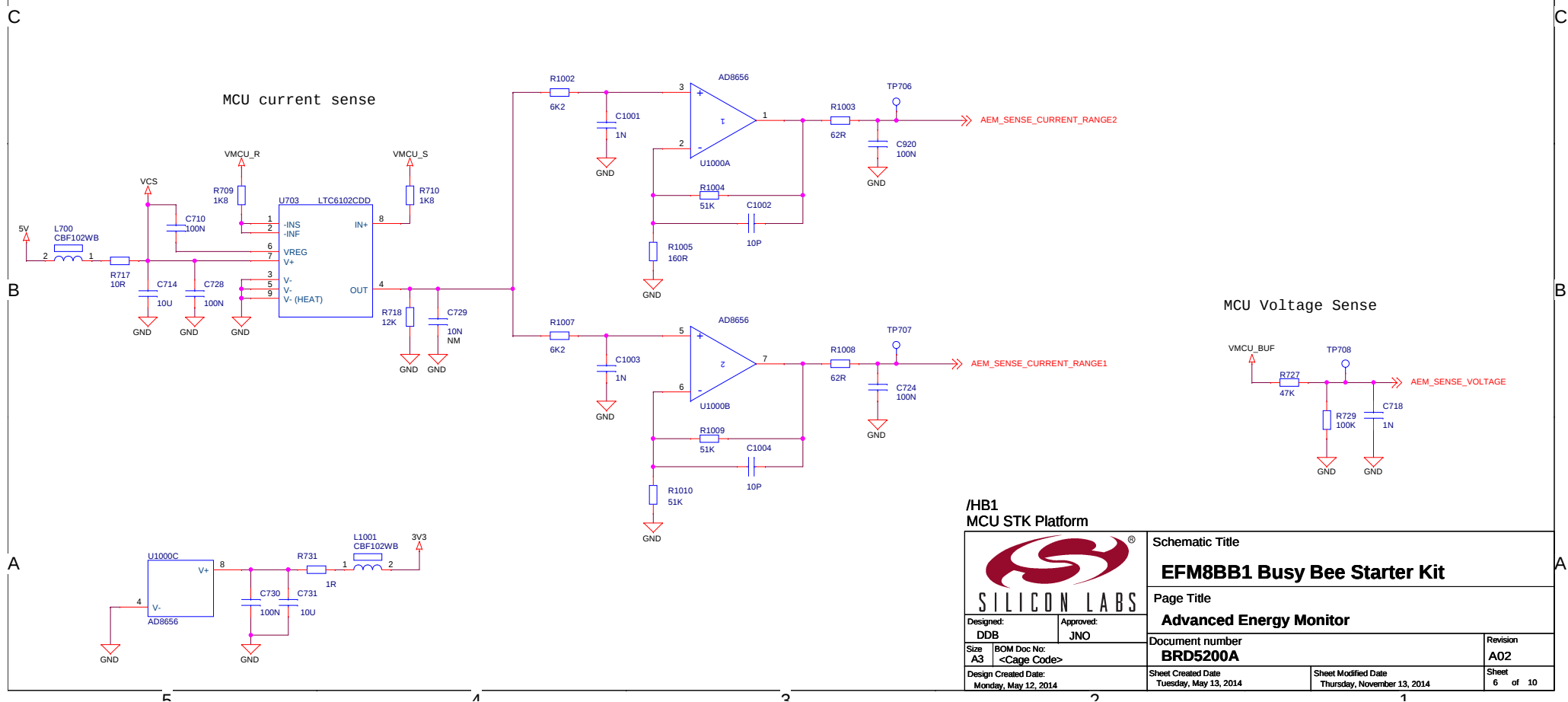
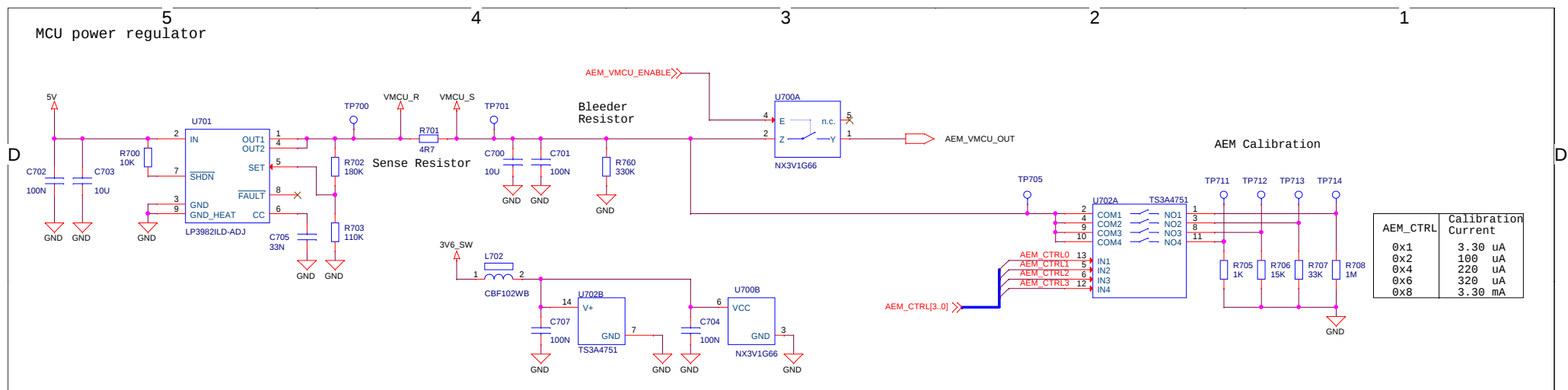
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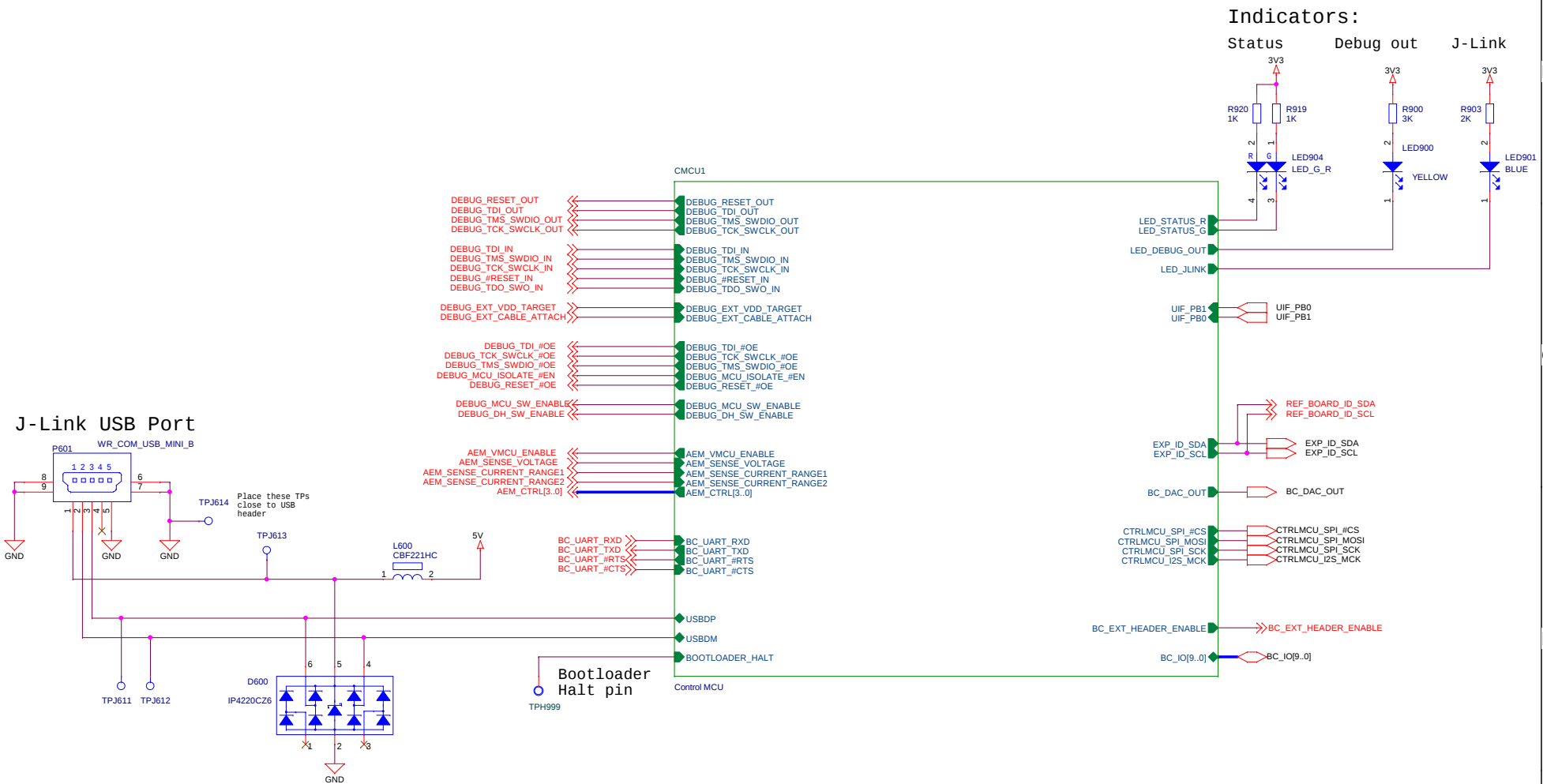


 SILICON LABS		Schematic Title	
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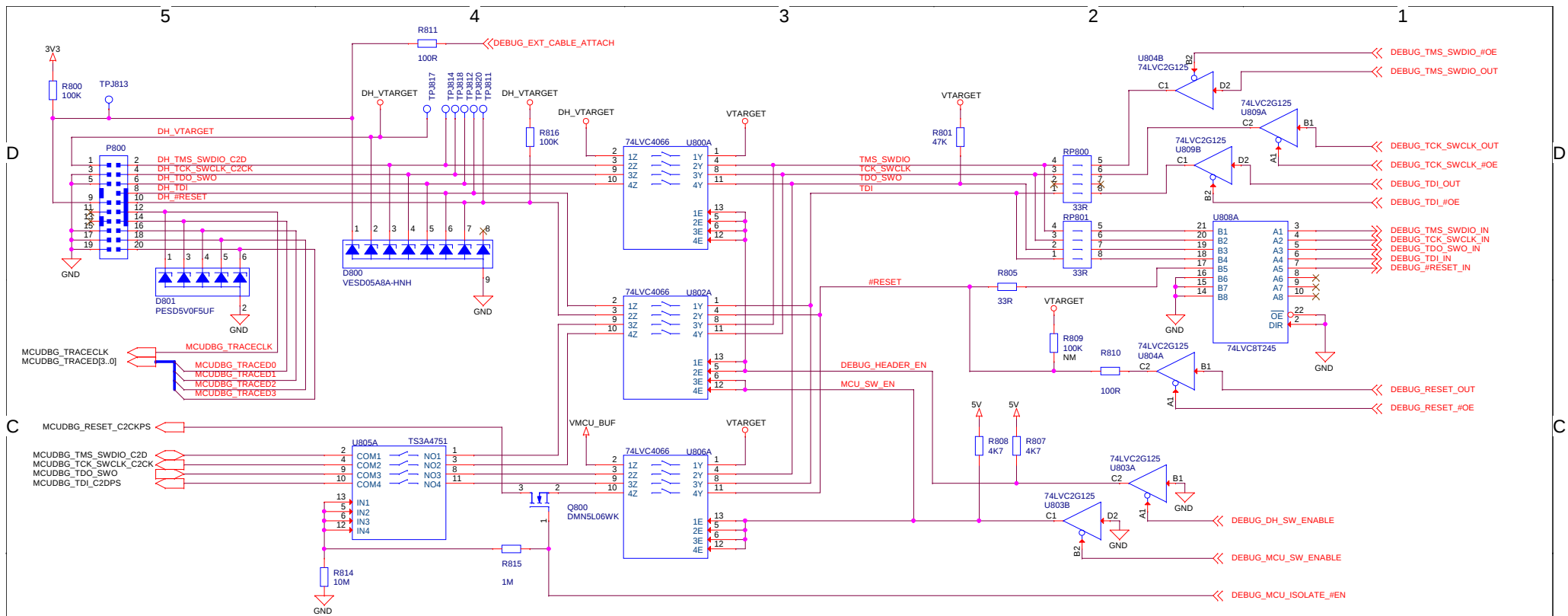


/HB1
MCU STK Platform

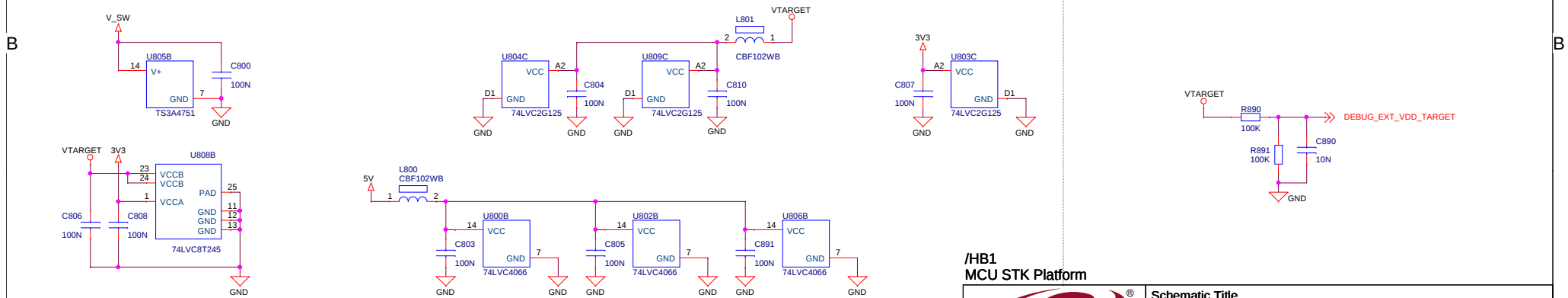
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/HB1 MCU STK Platform		Schematic Title	
		EFM8BB1 Busy Bee Starter Kit	
Page Title		Board Controller	
Designed: ANB	Approved: JNO	Document number BRD5200A	Revision A02
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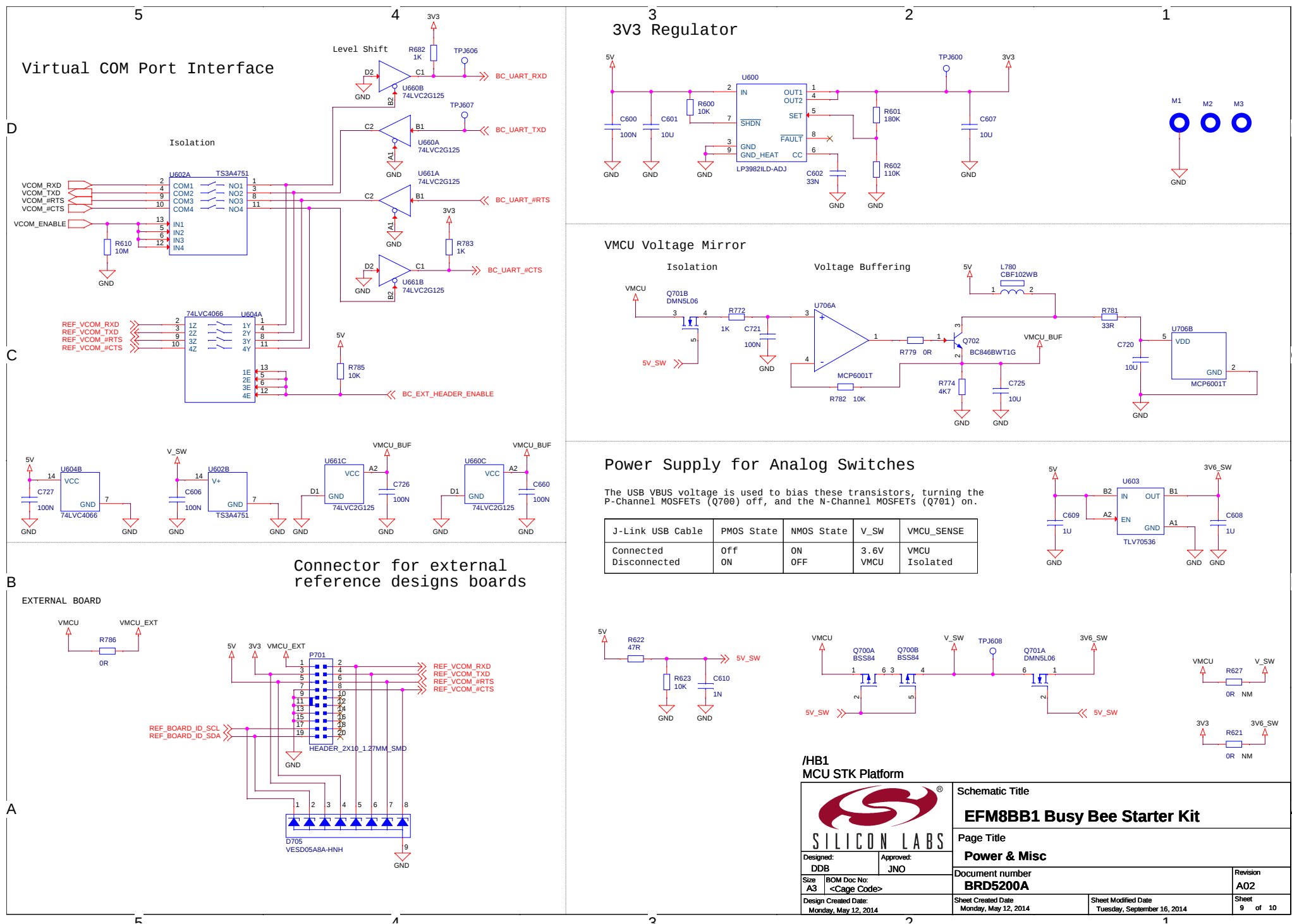
Power & Decoupling

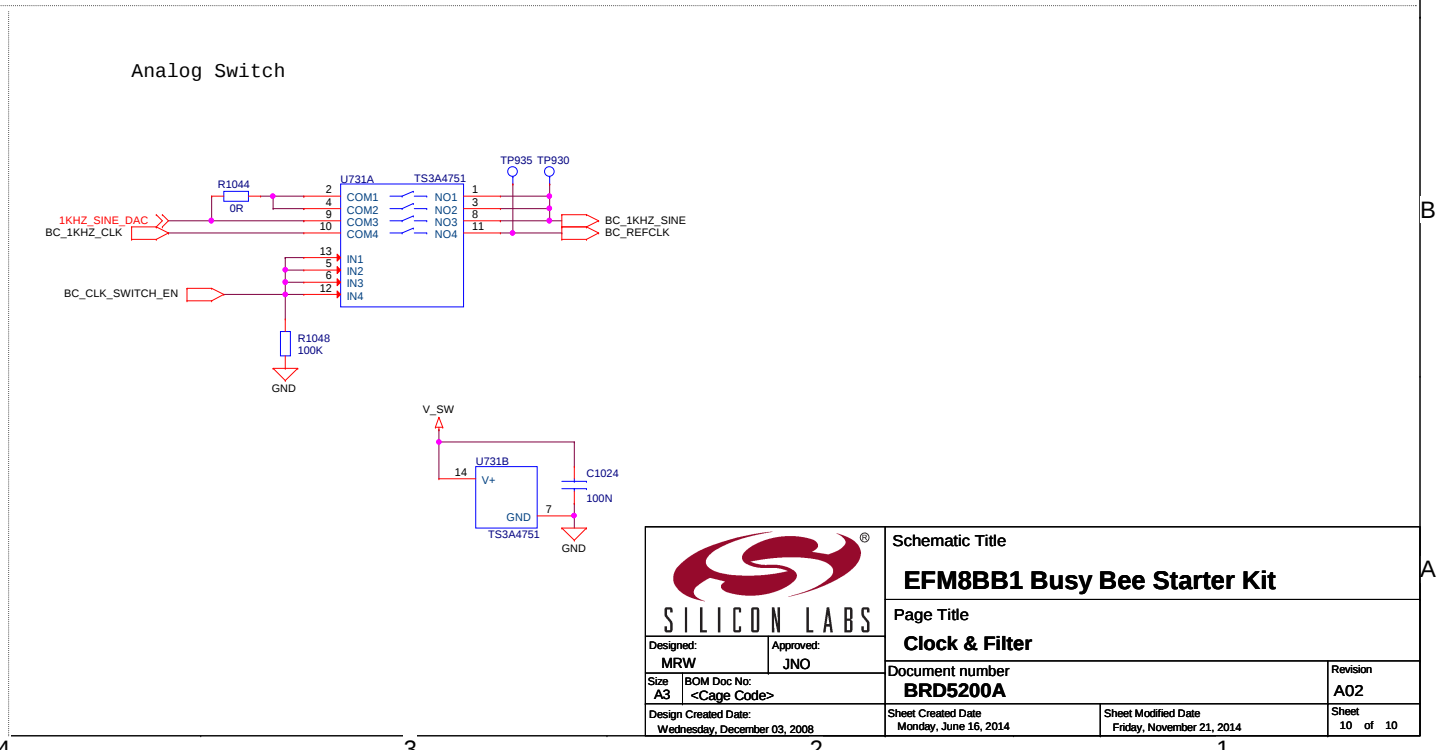
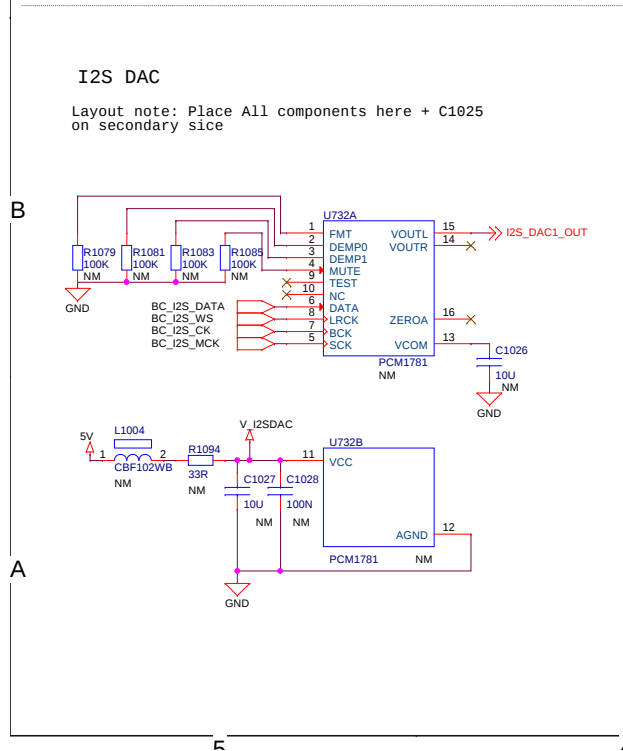
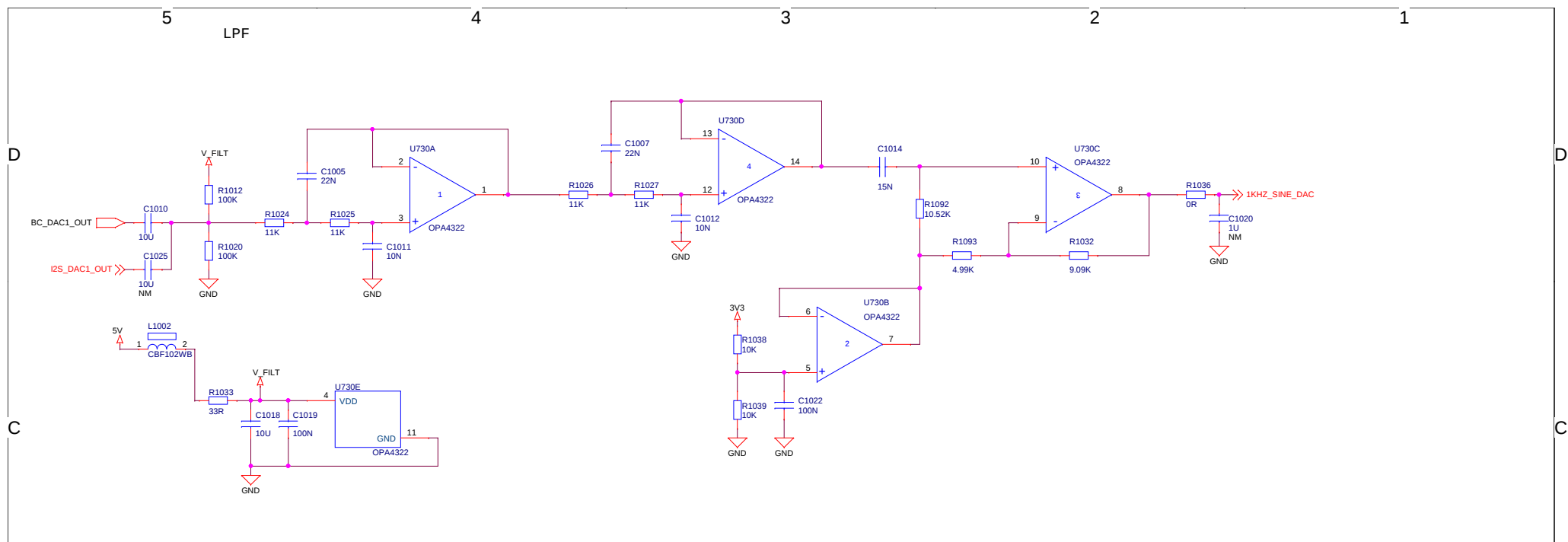


Mode	DEBUG_MCU_SW_ENABLE	DEBUG_DH_SW_ENABLE	DEBUG_BUF_#OE	ISOLATE_#EN	DH_VTARGET	VTARGET
Debug Out	0	1	0	0	External voltage	External voltage
MCU Debug	1	0	0	1	Disconnected	VMCU
Debug In	1	1	1	1	VMCU	VMCU
Debug Off	1	1	1	0	-	-

/HB1
MCU STK Platform

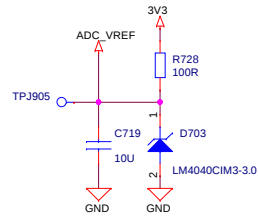
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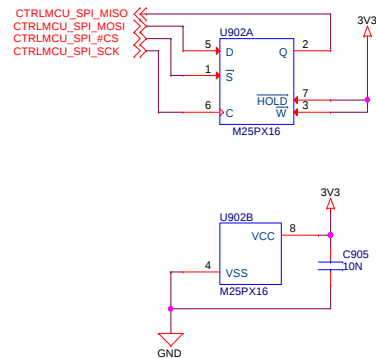


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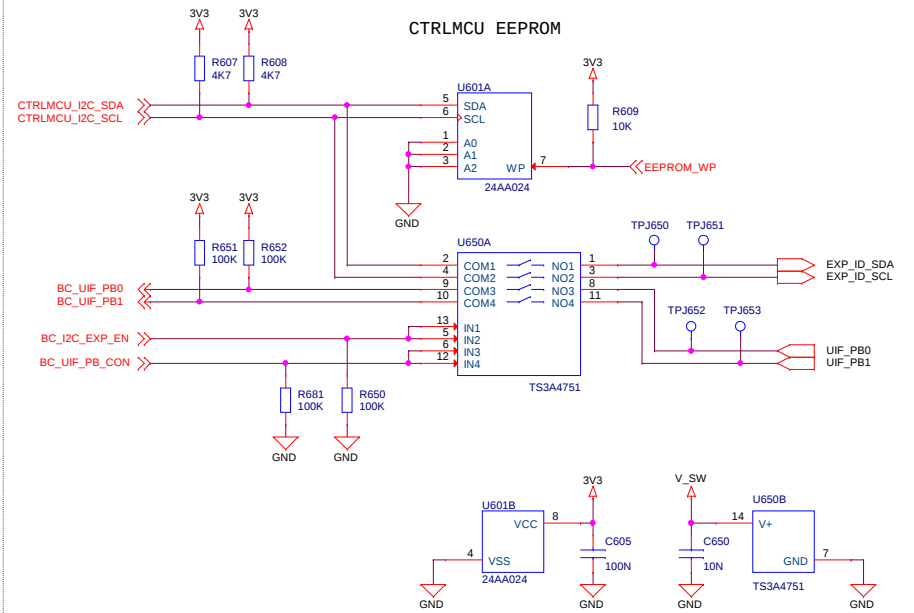
ADC reference voltage



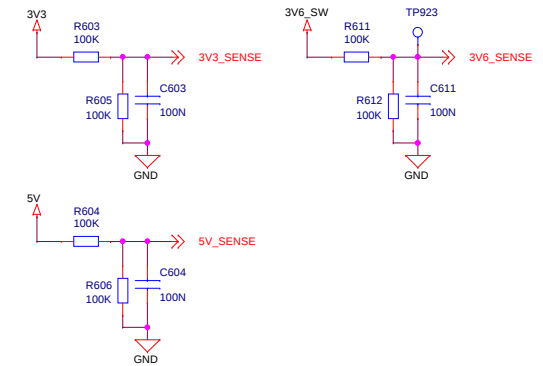
CTRLMCU SERIAL FLASH



CTRLMCU EEPROM



POWER SENSE



/HB1/CMCU1
Control MCU

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Designed: ANB		Page Title	
Approved: JNO		Control MCU Misc	
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