EFM8BB1 Busy Bee STK

Revision History

Rev.	Description
A00	Initial version released for production.
A01	Minor updates to design. Updated sine wave generator and new PCB.
A02	Updated PCB revision.
A03	Updated EFM8 to Rev B. Un-mounted D801.

PCB1

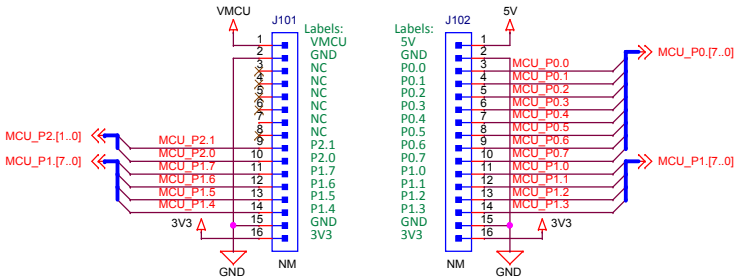
PCB5200

/
STK

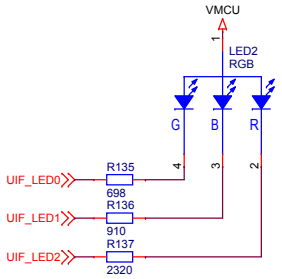
SILICON LABS

Designed: MRW	Approved: JNO	Schematic Title: EFM8BB1 Busy Bee STK	
Size: A3	BOM Doc No:	Page Title: Title Page	
Design Created Date: Wednesday, December 03, 2008		Document number: BRD5200A	Revision: A03
		Sheet Created Date: Thursday, May 15, 2014	Sheet Modified Date: Tuesday, December 19, 2017
			Sheet: 1 of 12

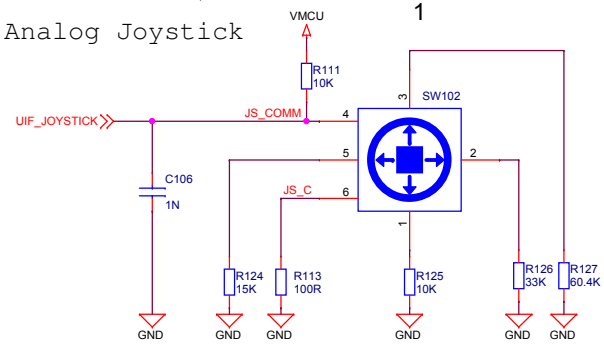
Breakout Connections



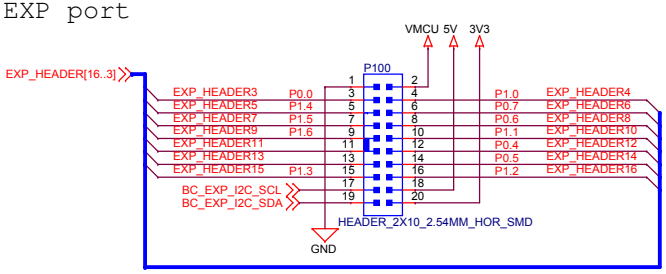
RGB LED



Analog Joystick



EXP port



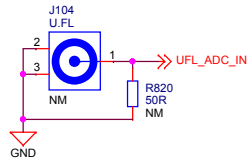
EXP-Header Functionality

** Indicates potential STK hardware conflicts

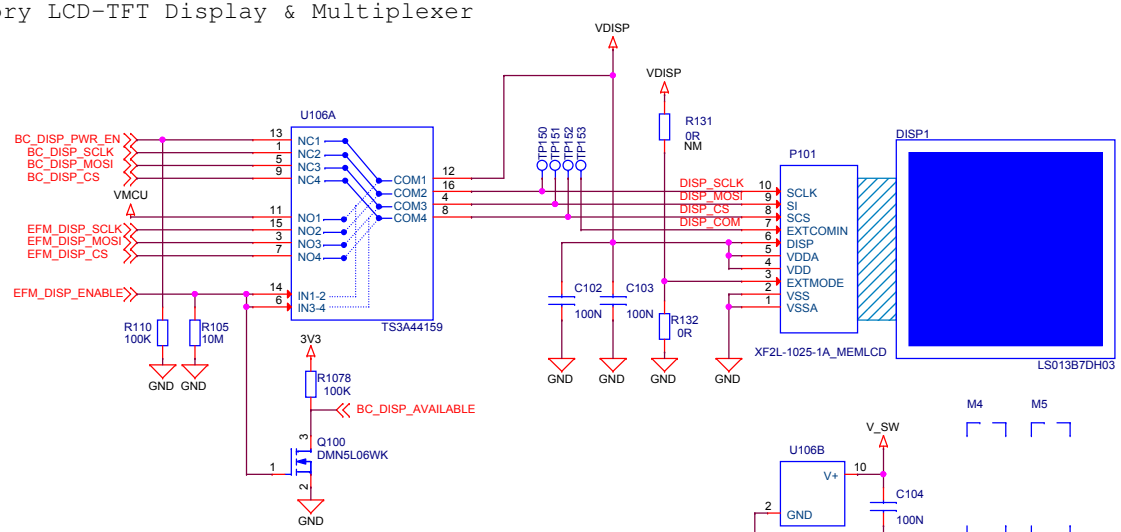
1	GND			
3	P0.0		CMP0.0/ADC0.0	
5	P1.4		CMP1.4/ADC0.12	** STK LED0
7	P1.5		CMP1.5/ADC0.13	** STK LED1
9	P1.6		CMP1.6/ADC0.14	** STK LED2
11				
13				
15	P1.3	I2C0_SCL	CMP1.3/ADC0.11	
17	Reserved for EXP Board Identification			
19	Reserved for EXP Board Identification			

2	VMCU		
4	P1.0	SPI0_MOSI	CMP1.0/ADC0.8
6	P0.7	SPI0_MISO	CMP0.7/ADC0.7
8	P0.6	SPI0_SCK	CMP0.6/ADC0.6
10	P1.1	SPI0_NSS	CMP1.1/ADC0.9
12	P0.4	UART0_TX	CMP0.4/ADC0.4
14	P0.5	UART0_RX	CMP0.5/ADC0.5
16	P1.2	I2C0_SDA	CMP1.2/ADC0.10
18	5V		
20	3V3		

U.FL ADC Connection



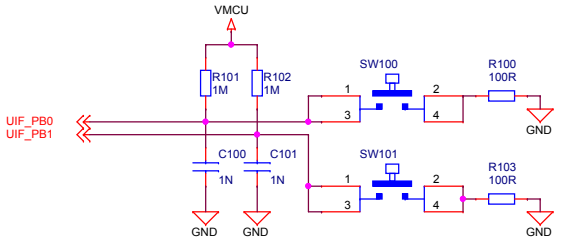
Memory LCD-TFT Display & Multiplexer



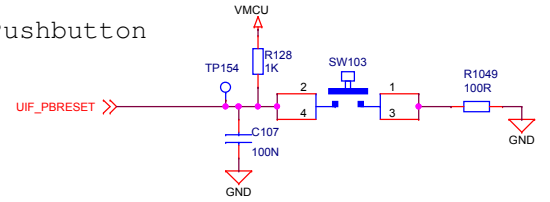
The EFM8 always controls ownership of the display using the EFM_DISP_ENABLE signal.

EFM_DISP_ENABLE	DISP_CTRL	VDISP
0	BC	BC_DISP_PWR_EN
1	EFM	VMCU

User pushbuttons



RESET Pushbutton



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STK

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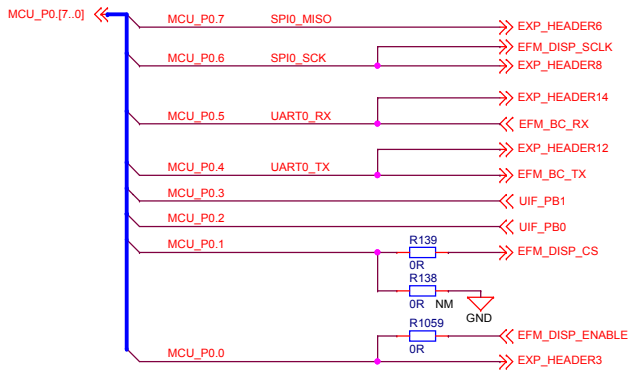
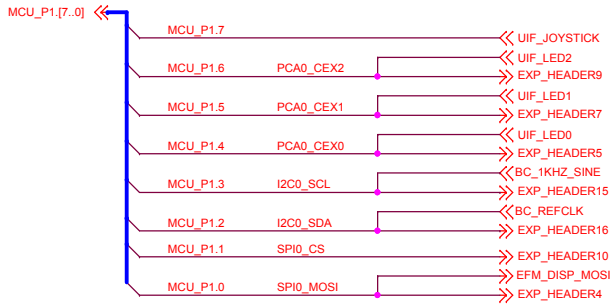
Schematic Title	EFM8BB1 Busy Bee STK
Page Title	User Interfaces
Designed: MRW / Approved: JNO	
Size: A3 / BOM Doc No:	
Document number	BRD5200A
Revision	A03
Design Created Date: Wednesday, December 03, 2008	
Sheet Created Date: Wednesday, August 28, 2013	
Sheet Modified Date: Tuesday, December 19, 2017	
Sheet	2 of 12

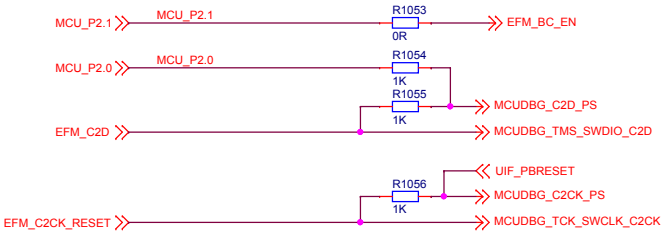
P0 Connections



P1 Connections



P2 & DEBUG Connections



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STK

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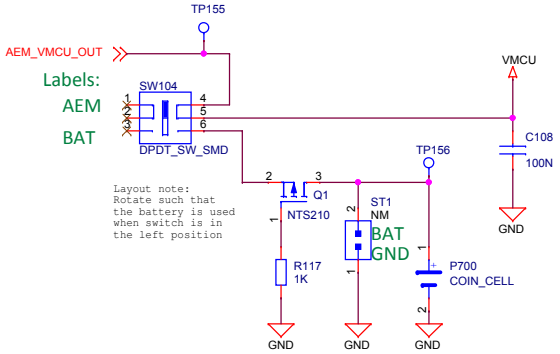
Schematic Title
EFM8BB1 Busy Bee STK

Page Title
Signal Assignments

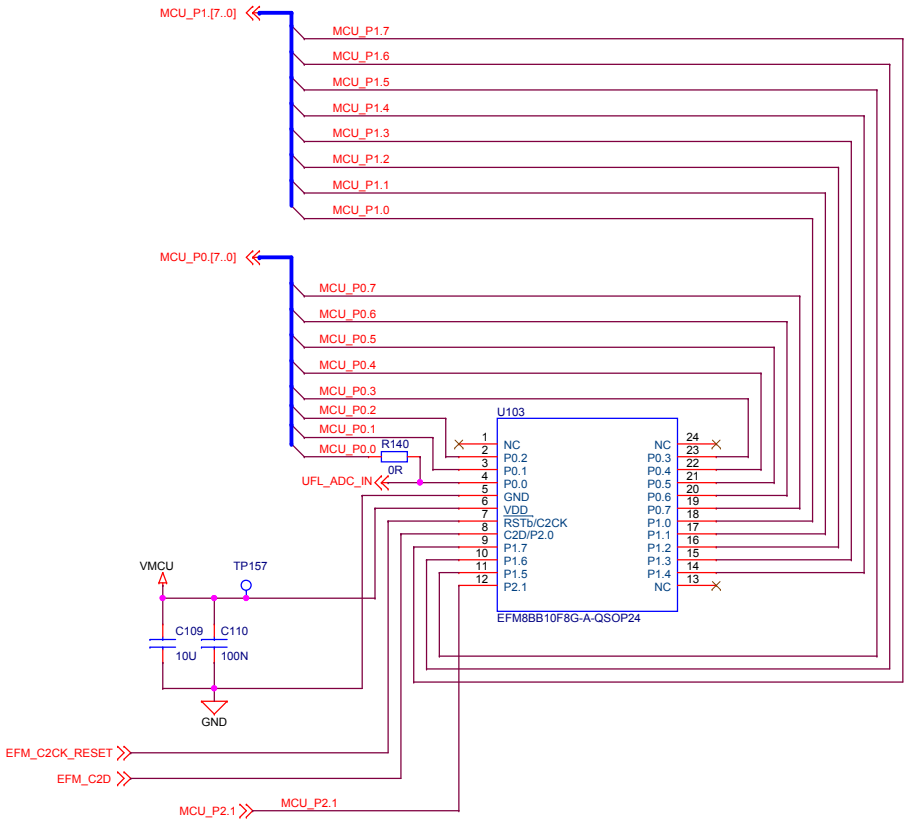
Designed: MRW	Approved: JNO	Document number BRD5200A	Revision A03
Size A3	BOM Doc No:		
Design Created Date: Wednesday, December 03, 2008		Sheet Created Date Wednesday, August 28, 2013	Sheet Modified Date Tuesday, December 19, 2017
			Sheet 3 of 12

Power Switch

SWITCH POS	MODE DESCRIPTION
AEM	AEM Enabled, VMCU sourced from external 3.3V LDO powered by BC USB 5V supply
BAT	AEM Disabled, VMCU sourced from external coin-cell battery or external power supply



C2 Debug Header



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STK

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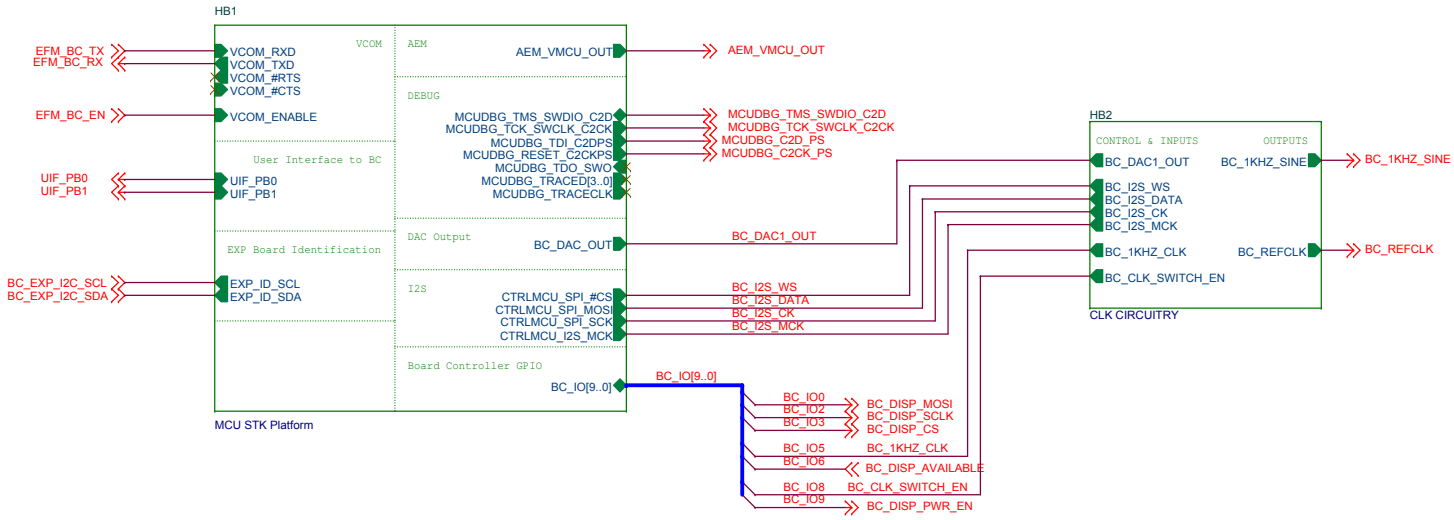
Designed: MRW	Approved: JNO
Size A3	BOM Doc No:
Design Created Date: Wednesday, December 03, 2008	

Schematic Title
EFM8BB1 Busy Bee STK

Page Title
EFM8 I/O & Power

Document number	Revision
BRD5200A	A03

Sheet Created Date	Sheet Modified Date	Sheet
Wednesday, August 28, 2013	Tuesday, December 19, 2017	4 of 12



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STK

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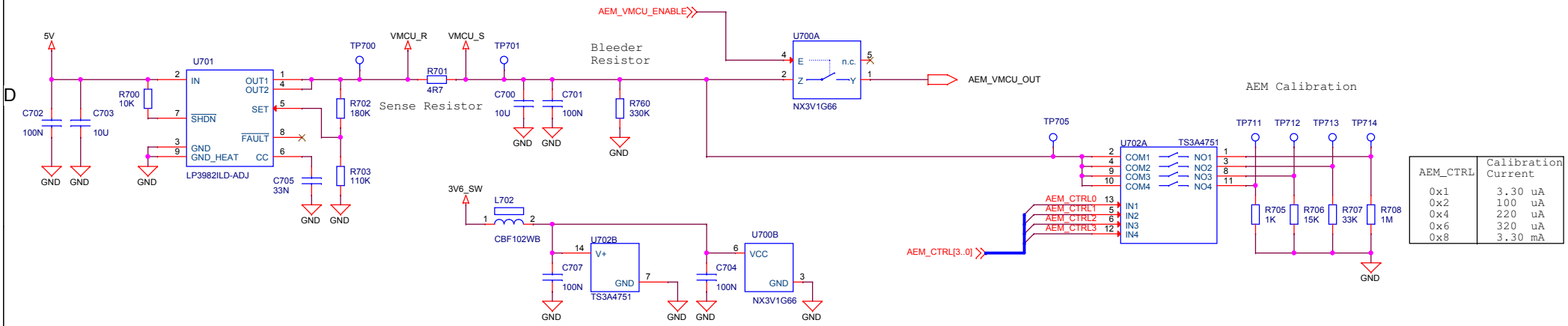
Designed: MRW	Approved: JNO
Size A3	BOM Doc No:
Design Created Date: Wednesday, December 03, 2008	

Schematic Title
EFM8BB1 Busy Bee STK

Page Title
STK Common Platform

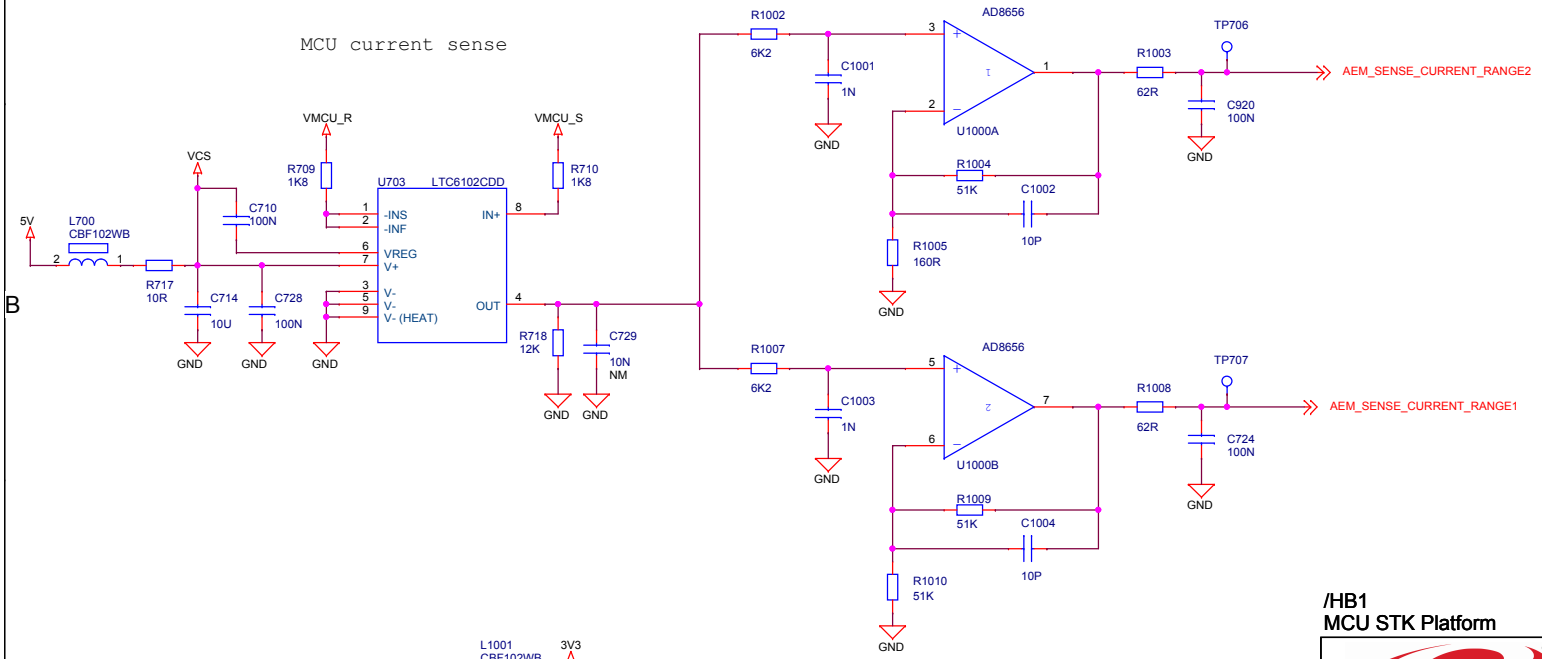
Document number **BRD5200A**		Revision A03
Sheet Created Date Thursday, May 15, 2014	Sheet Modified Date Tuesday, December 19, 2017	Sheet 5 of 12

MCU power regulator

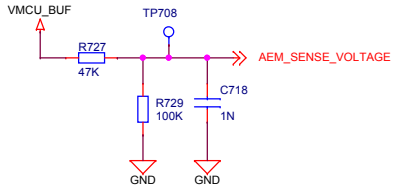


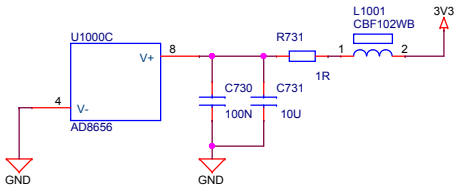
AEM_CTRL	Calibration Current
0x1	3.30 uA
0x2	100 uA
0x4	220 uA
0x6	320 uA
0x8	3.30 mA

MCU current sense



MCU Voltage Sense





/HB1
MCU STK Platform

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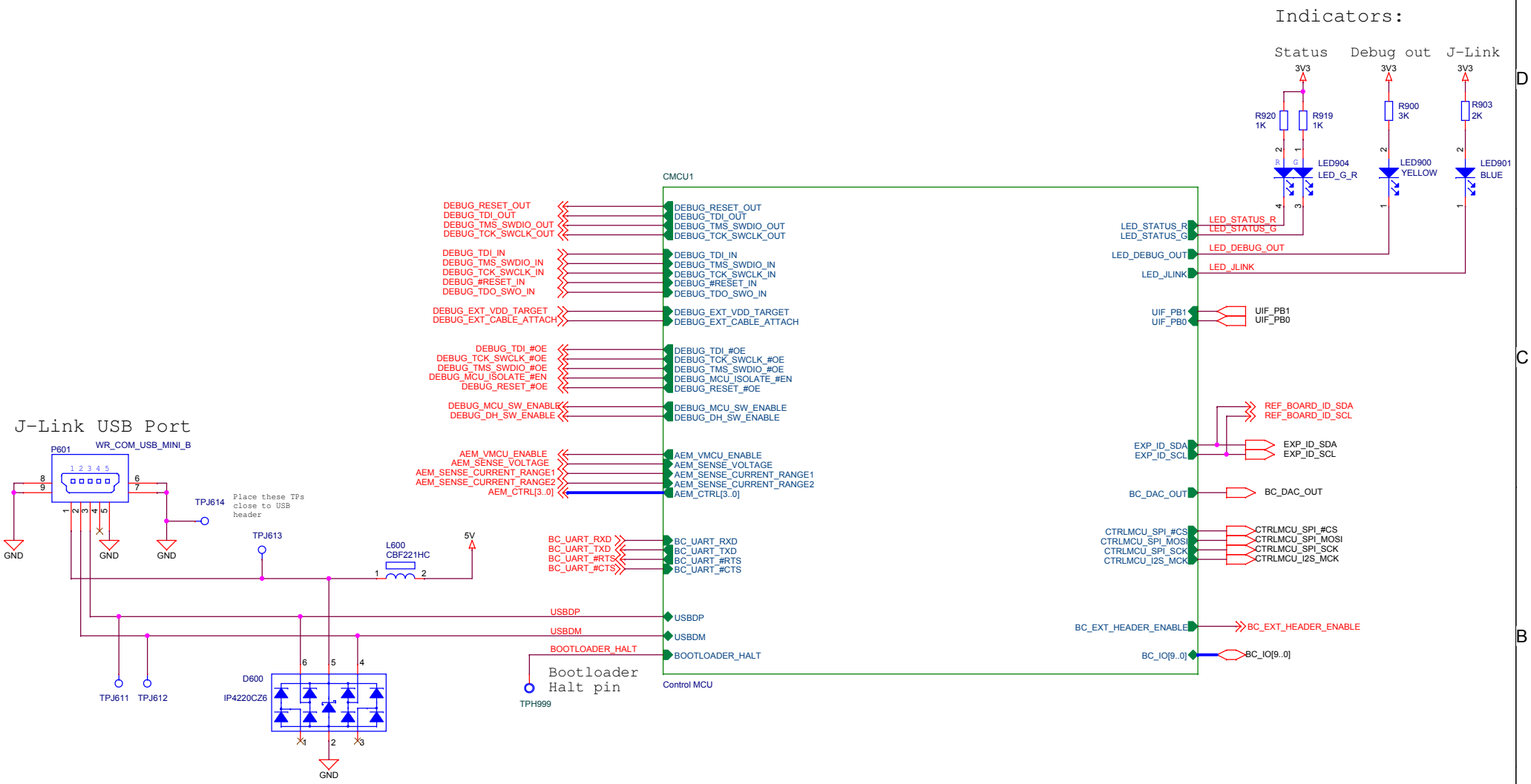
Designed: DDB	Approved: JNO
Size A3	BOM Doc No:
Design Created Date: Monday, May 12, 2014	

Schematic Title
EFM8BB1 Busy Bee STK

Page Title
Advanced Energy Monitor

Document number BRD5200A		Revision A03
Sheet Created Date Tuesday, May 13, 2014	Sheet Modified Date Wednesday, December 13, 2017	Sheet 6 of 12



/HB1
MCU STK Platform

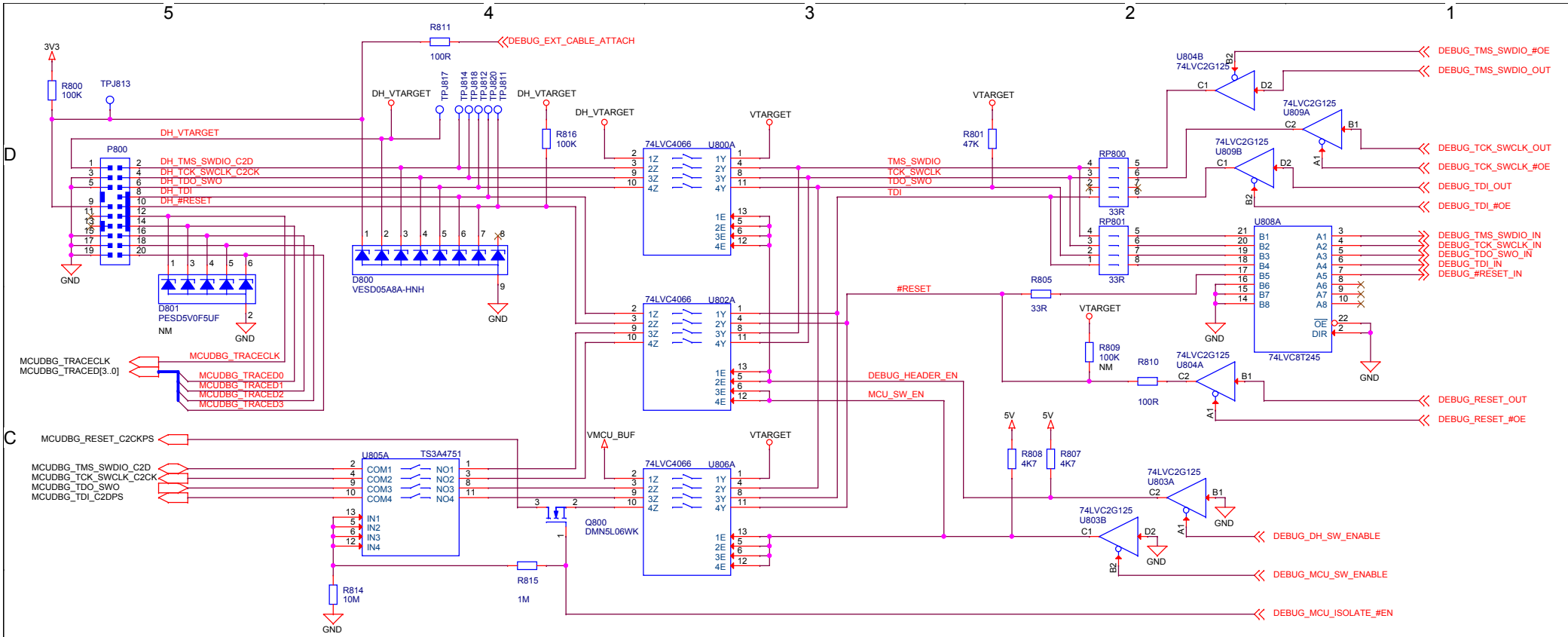
SILICON LABS

Designed: ANB	Approved: JNO
Size A3	BOM Doc No:
Design Created Date: Monday, May 12, 2014	

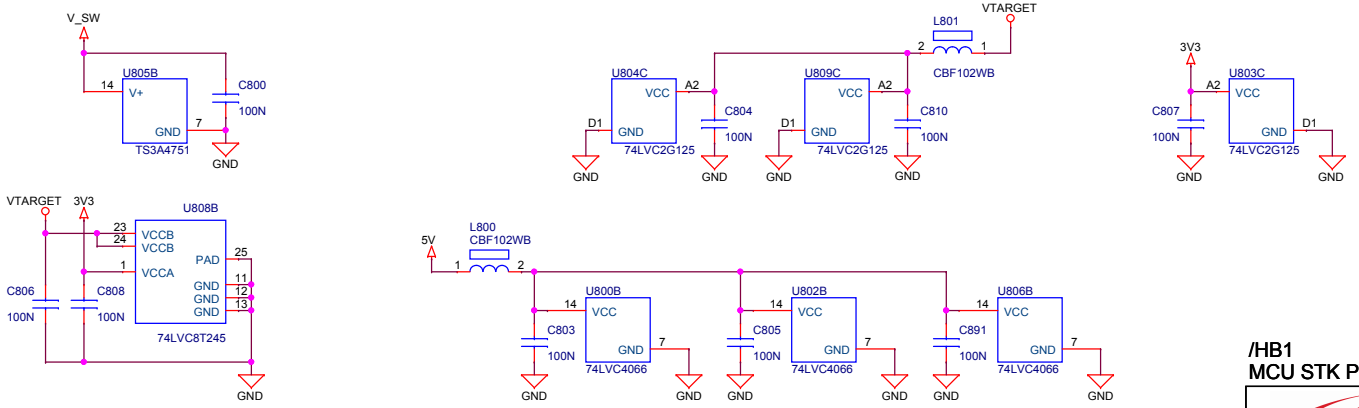
Schematic Title
EFM8BB1 Busy Bee STK

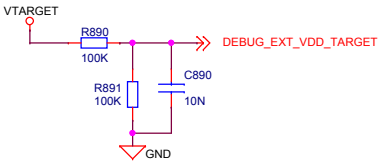
Page Title
Control MCU

Document number BRD5200A		Revision A03
Sheet Created Date Wednesday, May 14, 2014	Sheet Modified Date Wednesday, December 13, 2017	Sheet 7 of 12



Power & Decoupling





Mode	DEBUG_MCU_SW_ENABLE	DEBUG_DH_SW_ENABLE	DEBUG_BUF_#OE	ISOLATE_#EN	DH_VTARGET	VTARGET
Debug Out	0	1	0	0	External voltage	External voltage
MCU Debug	1	0	0	1	Disconnected	VMCU
Debug In	1	1	1	1	VMCU	VMCU
Debug Off	1	1	1	0	-	-

/HB1
MCU STK Platform

SILICON LABS

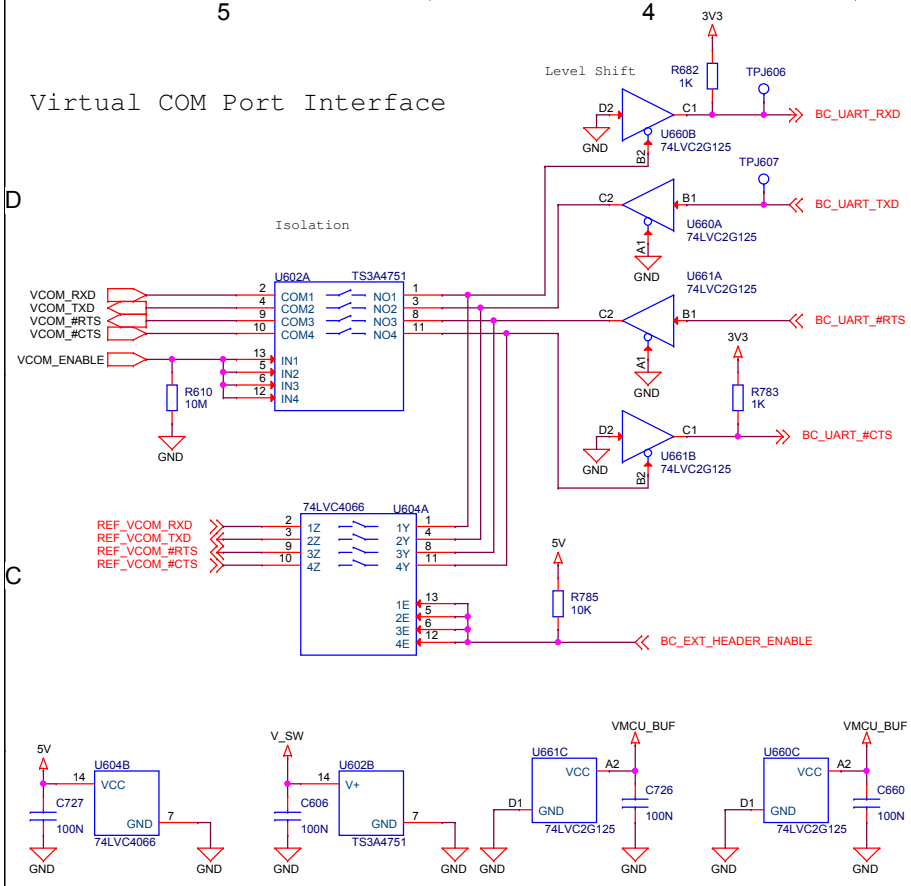
Designed: DDB	Approved: JNO
Size A3	BOM Doc No:
Design Created Date: Monday, May 12, 2014	

Schematic Title
EFM8BB1 Busy Bee STK

Page Title
Debug Interface

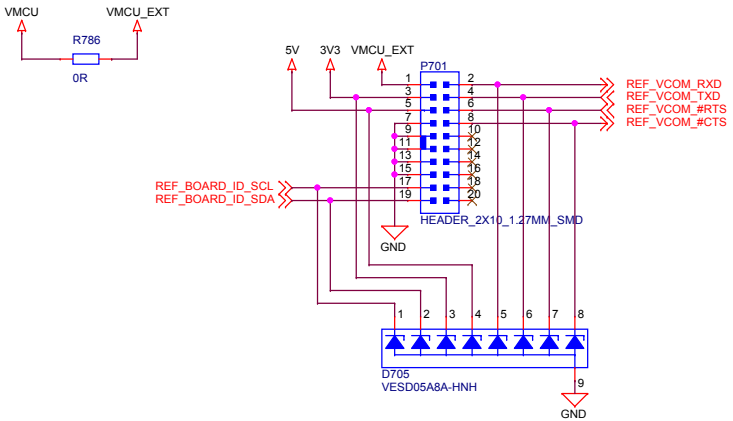
Document number BRD5200A	Revision A03
Sheet Created Date: Monday, May 12, 2014	Sheet Modified Date: Wednesday, December 13, 2017
	Sheet 8 of 12

Virtual COM Port Interface

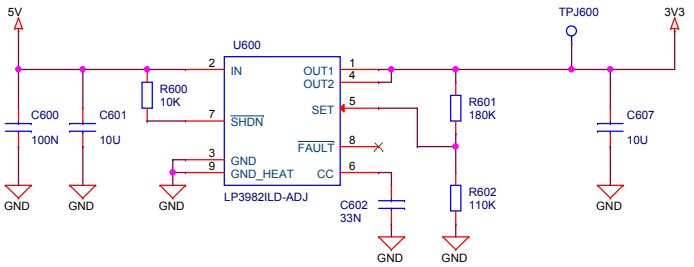


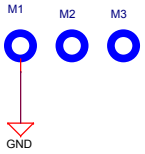
Connector for external reference designs boards

EXTERNAL BOARD

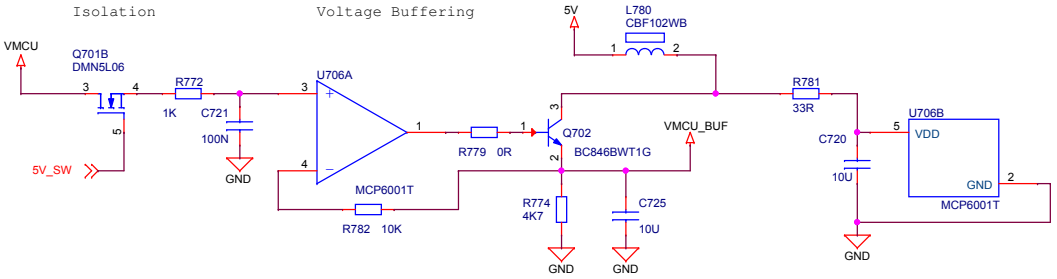


3V3 Regulator





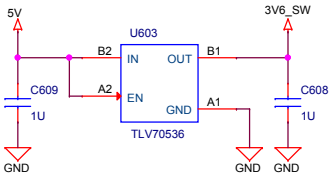
VMCU Voltage Mirror

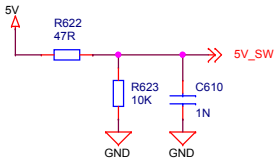


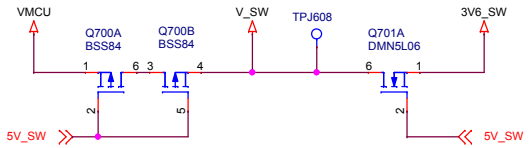
Power Supply for Analog Switches

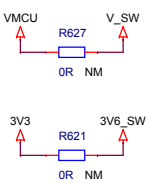
The USB VBUS voltage is used to bias these transistors, turning the P-Channel MOSFETs (Q700) off, and the N-Channel MOSFETs (Q701) on.

J-Link USB Cable	PMOS State	NMOS State	V_SW	VMCU_SENSE
Connected	Off	ON	3.6V	VMCU
Disconnected	ON	OFF	VMCU	Isolated









/HB1
MCU STK Platform

SILICON LABS

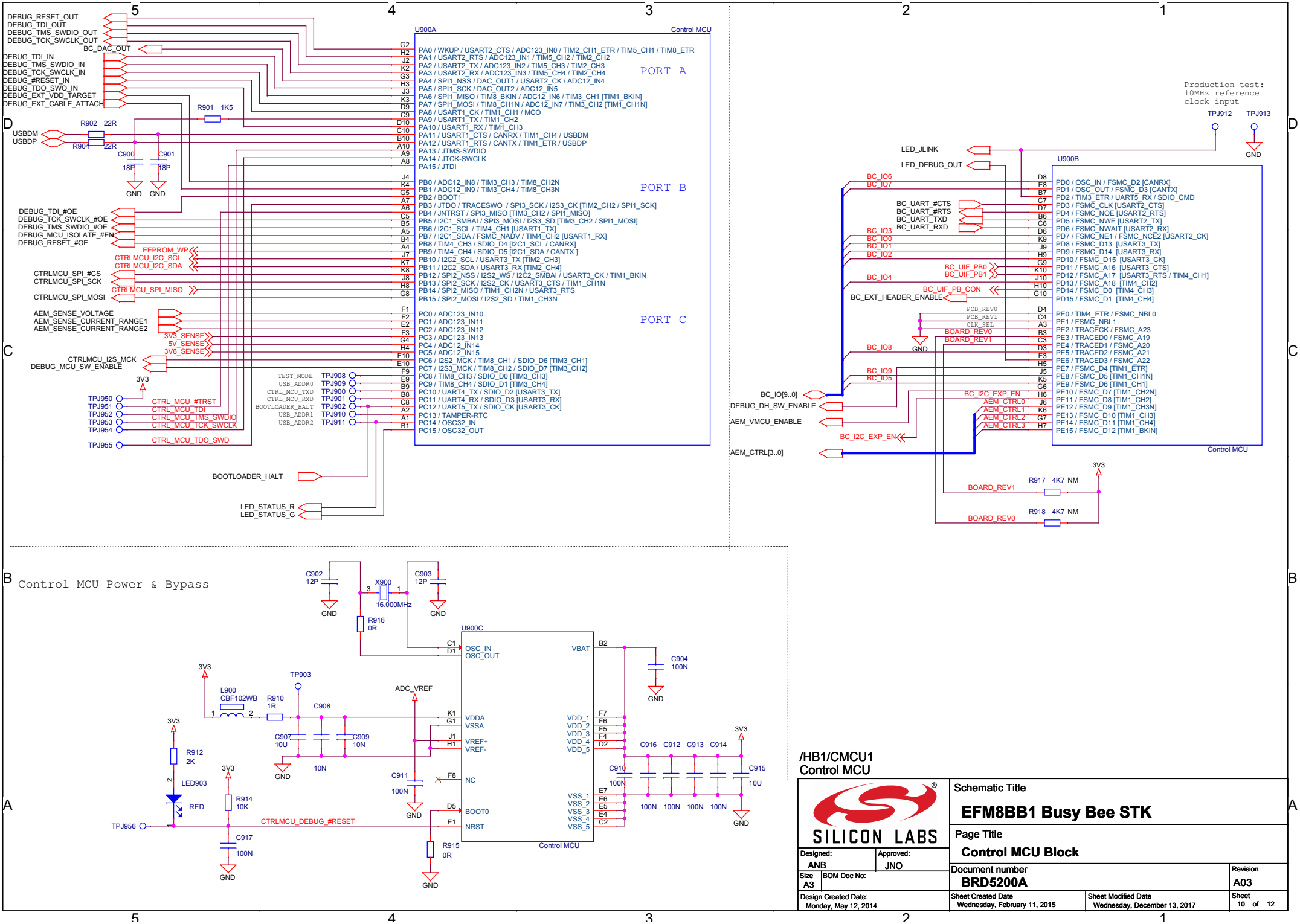
Designed: DDB	Approved: JNO
Size A3	BOM Doc No:
Design Created Date: Monday, May 12, 2014	

Schematic Title
EFM8BB1 Busy Bee STK

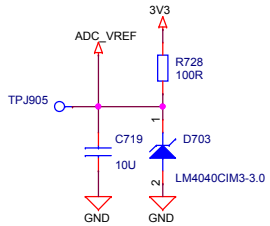
Page Title
Power & Misc.

Document number	Revision
BRD5200A	A03

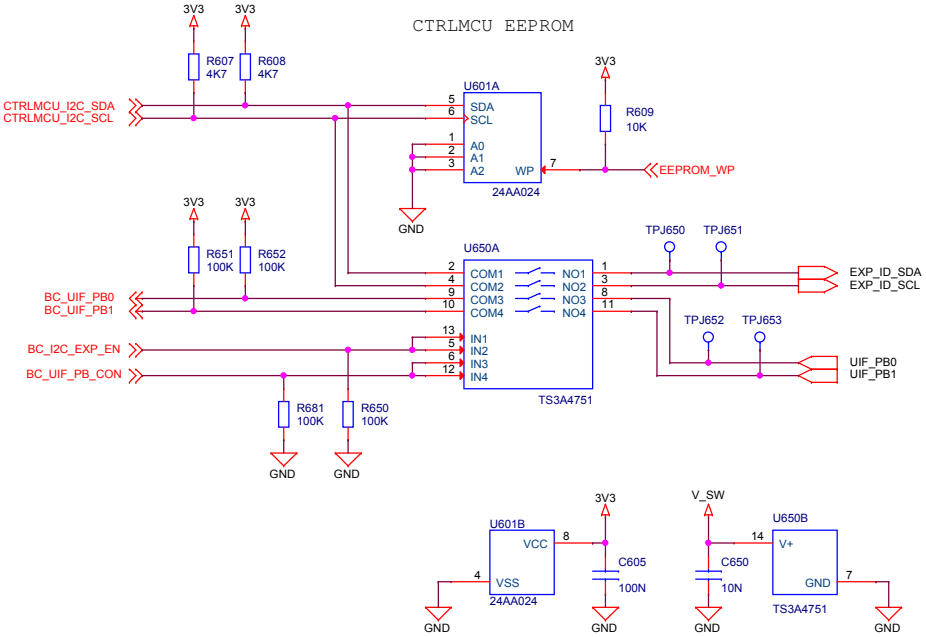
Sheet Created Date	Sheet Modified Date	Sheet
Monday, May 12, 2014	Wednesday, December 13, 2017	9 of 12



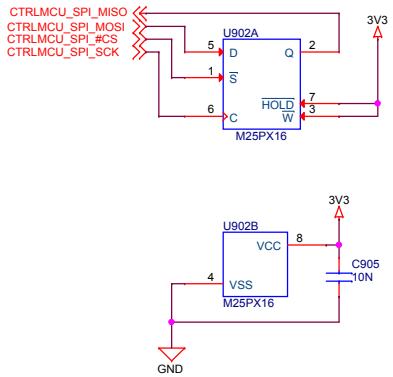
ADC reference voltage



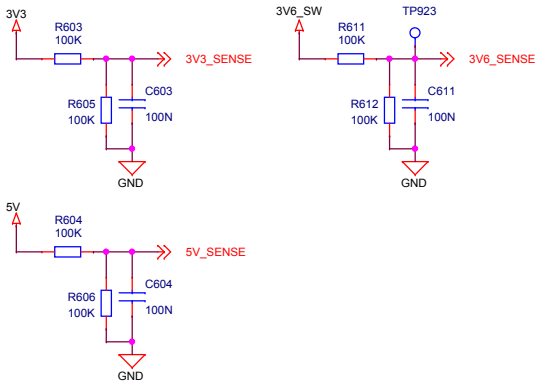
CTRLMCU EEPROM



CTRLMCU SERIAL FLASH



POWER SENSE



/HB1/CMCU1
Control MCU

SILICON LABS

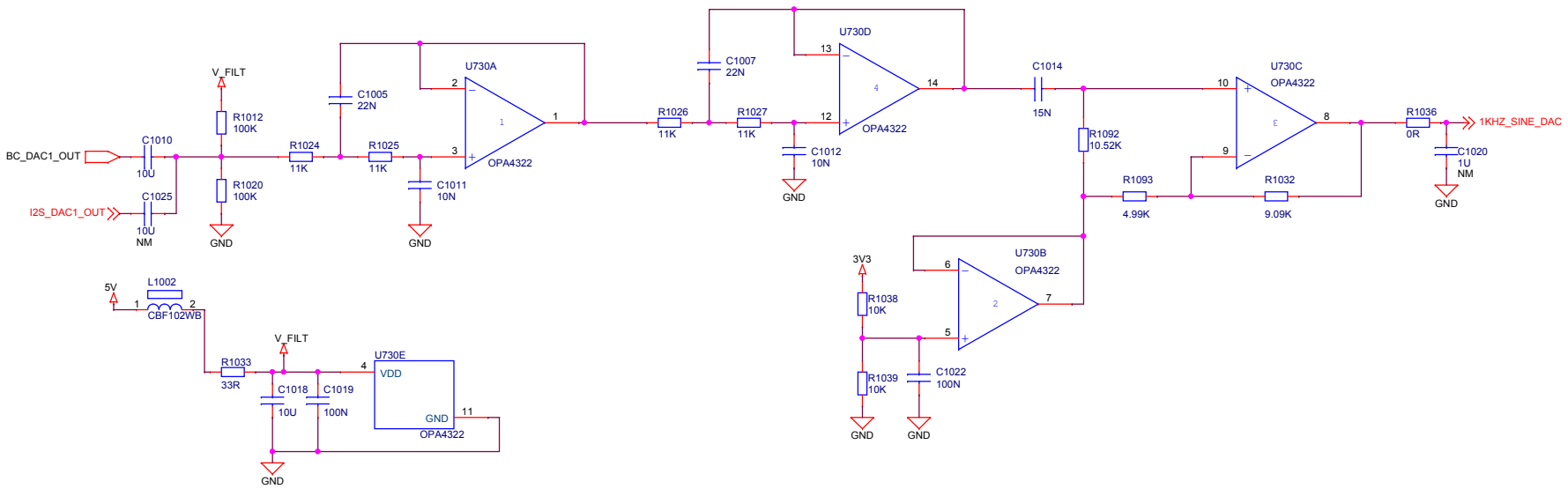
Designed: ANB	Approved: JNO
Size: A3	BOM Doc No:
Design Created Date: Monday, May 12, 2014	

Schematic Title: **EFM8BB1 Busy Bee STK**

Page Title: **Control MCU Misc.**

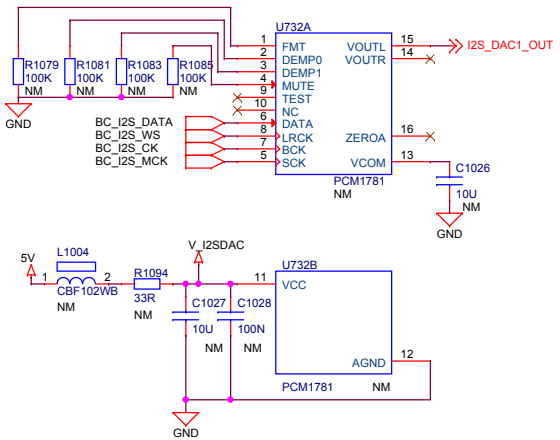
Document number: **BRD5200A**	Revision: A03
Sheet Created Date: Wednesday, February 11, 2015	Sheet Modified Date: Tuesday, December 19, 2017
	Sheet: 11 of 12

LPF

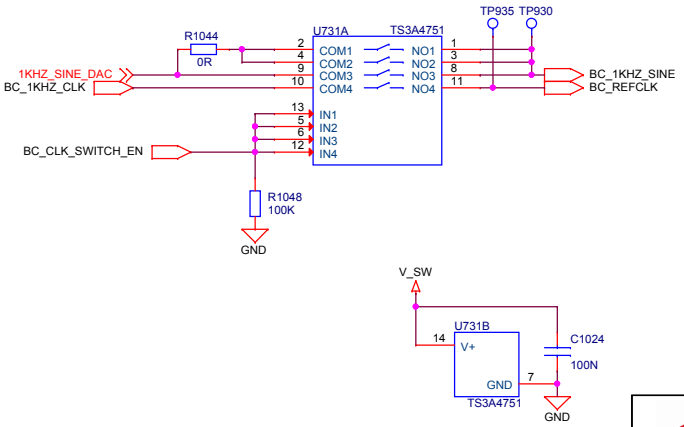


I2S DAC

Layout note: Place All components here + C1025 on secondary sice



Analog Switch



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Designed: MRW	Approved: JNO
Size A3	BOM Doc No:
Design Created Date: Wednesday, December 03, 2008	

Schematic Title: **EFM8BB1 Busy Bee STK**

Page Title: **Clock & Filter**

Document number: **BRD5200A**		Revision: A03
Sheet Created Date: Monday, June 16, 2014	Sheet Modified Date: Wednesday, December 13, 2017	Sheet 12 of 12