

*** PCB SPECIFICATION FOR BARE BOARD MANUFACTURING ***

PRODUCT OWNER : Silicon Labs
DOCUMENT/BOARD : PCB5207B Rev A00
DATE : 2021-04-16
REVISION : A00

PREPARED BY : Øyvind Schibsted
BOARDS pr PANEL: 4 (1 x 4)
PANEL SIZE : 141.0 x 280.0 mm
BOARD SIZE : 115.0 x 60.0 mm
BOARD THICKNESS: 1.6 mm +/- 10 %
NO OF LAYERS : 6
MATERIAL(S) : Glass Epoxy FR-4, IPC-4101 (current revision) /99 or /124 (Tg min 150 C)
Materials in compliance with the RoHS and WEEE directives
MARKINGS : All PCB manufacturer's markings (logo/UL code/DC code)
shall be put in the PCB frame. No marking on the boards is allowed.
(Avoid areas reserved for DataMatrix, Barcodes or Labels)
QUALITY REQ. : IPC-A-600 (current revisions) Class 2, and IPC specifications
referred to by IPC-A-600
GENERAL REQ. : - Copper, e.g. balancing, must not be added or removed from inside
the board outline(s), without written consent/approval.
If applicable, the following requirements are valid:
- Copper balancing may be applied on break-away-tabs,
or otherwise outside board outline(s), but must have
a minimum 1.5 mm clearance to possible fiducials.
- If Build-Up (Stack-Up) is specified, follow Build-Up,
otherwise use (board manufacturer) standard Build-Up.
- Break-away areas may be used for patterns, holes etc
by manufacturer for QA purposes.
- If V-CUT, use angle 30 +/- 5 degrees.
V-CUT minimum remaining thickness 0.5 +/- 0.1 mm.
Use of V-CUT test pads is allowed.
- Inner radius (contour/outline) 1.2 mm, unless stated otherwise.
COPPER THK. : SEE BUILD-UP
COPPER PASSIV. : ENIG to meet IPC-4552 Class 2 requirements (current revision)
(Electroless Nickel/Immersion Gold)
SOLDER MASK : IPC-SM-840 Class 2 (T) (current revision)
Solder Mask Color: GLOSSY BLACK
VIA HOLES : PLUGGED/FILLED, IPC-4761 (current revision) Type IV-b
Plugged and Covered Both Sides, Low CTE Plugging Paste
If Type IV-b is not available as a process, then Type IV-a
for the Top Side, and Overprinted (Tented) Bot Side is OK
Some vias may intentionally be open on one side. Normally vias
inside Exposed Pads under ICs. Follow Gerber.
LEGEND/SILKSCR.: WHITE, BOTH SIDES (TOP + BOT)
CONTROLLED IMP : Edge-coupled Coated Microstrip:
90 ohm (DP) +/-10% L6, REF=L5, W=0.12 mm Gap=0.12 mm
NOMINAL VALUES for Width, Spacing and VIA Diameter:
Cu TRACK(TRACE): Minimum conductor width : 0.10 mm (4 mil)
Cu SPACING : Minimum conductor spacing: 0.0889 mm (3.5 mil)
MINIMUM VIA : Minimum via pad diameter : 20 mil (via hole 0.25 mm)
Min via hole may have more than one pad diameter.

(SPECIFICATION CONTINUED ON NEXT PAGE)

BUILD-UP :

L1 =====| |===== 35 um Cu (ca) After plating
- - -| |- P R E P R E G - - - - 100 um
L2 =====| |===== 35 um Cu (1.0 Oz) (PLANE)
/////| |///// C O R E ///// 460 um
L3 =====| |===== 35 um Cu
- - -| |- P R E P R E G - - - - 225 um - - CENTER - -
L4 =====| |===== 35 um Cu
/////| |///// C O R E ///// 460 um
L5 =====| |===== 35 um Cu (PLANE)
- - -| |- P R E P R E G - - - - 100 um
L6 =====| |===== 35 um Cu

(Approximate Prepreg thicknesses)

TEST : 100% Electrical Test
Optical test, AOI (with automatic scanner)
Visual inspection
(Generate netlist from Gerber and Drill files)

Avoid use of 2125 Prepreg

If NB! is used in this specification, it is latin,
meaning "mark well" or "observe particularly"

Nominal tolerances (if no other tolerances given)
PTH +/- 0.10 mm for d <= 2.0 mm
PTH +/- 0.15 mm for 2.0 < d <= 5.3 mm
PTH +/- 0.20 mm for d > 5.3 mm
NPTH +/- 0.05 mm for d <= 5.3 mm
NPTH +/- 0.10 mm for d > 5.3 mm

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+++ YOUR CIRCUIT BOARD DESIGN PARTNER +++
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