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EFM8BB50 Pro Kit	
Board Function	Page
Title Page	1
User Interface	2
Signal Assignments	3
EFM8 Power & I/O	4
Target Voltage Supply	5
AEM	6
Debug Interface	7
Simplicity & VCOM	8
Power	9
Board Controller	10
Board Controller Misc	11

Revision History	
Rev.	Description
A00	Initial version

 SILICON LABS		Board Name EFM8BB50 Pro Kit	
Designed PEP		Page Title Title Page	
Size A3	Approved RGU	Board Number BRD5208A	Revision A00
Sheet Modified Date Friday, September 03, 2021		Revision A00	
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		Sheet 1 of 11	

Push Buttons

VMCU

R100
1M

C102
1N

GND

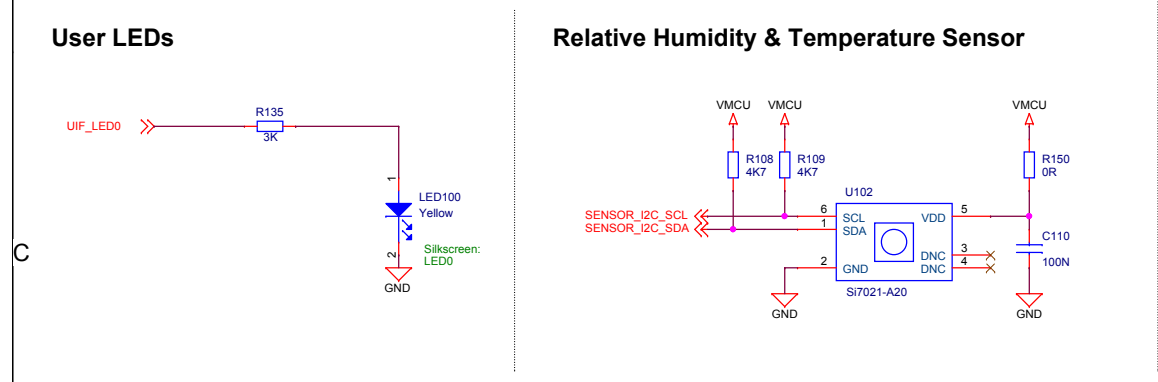
SW100
PTS810

R104
100R

GND

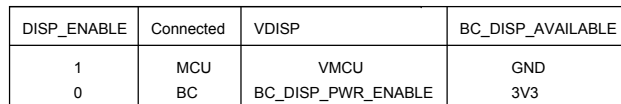
Silkscreen:
BTNO

UIF_BUTTON0



The EFM8 always controls ownership of the display using the DISP_ENABLE signal.

DISP_ENABLE	Connected	VDISP	BC_DISP_AVAILABLE
1	MCU	VMCU	GND
0	BC	BC_DISP_PWR_ENABLE	3V3



Header

EXP_HEADER[16..3]

EXP_HEADER3
EXP_HEADER5
EXP_HEADER7
EXP_HEADER9
EXP_HEADER11
EXP_HEADER13
EXP_HEADER15

BC_I2C_EXP_SCL
BC_I2C_EXP_SDA

GND

P101

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20

VMCU5V 3V3

EXP_HEADER4
EXP_HEADER6
EXP_HEADER8
EXP_HEADER10
EXP_HEADER12
EXP_HEADER14
EXP_HEADER16

HEADER_2X10_2.54MM_TH

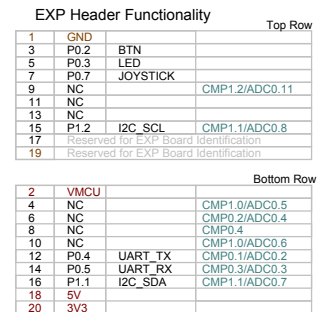
EXP Header Functionality

Top Row

1	GND		
3	P0.2	BTN	
5	P0.3	LED	
7	P0.7	JOYSTICK	
9	NC		CMP1.2/ADC0.11
11	NC		
13	NC		
15	P1.2	I2C_SCL	CMP1.1/ADC0.8
17		Reserved for EXP Board Identification	
19		Reserved for EXP Board Identification	

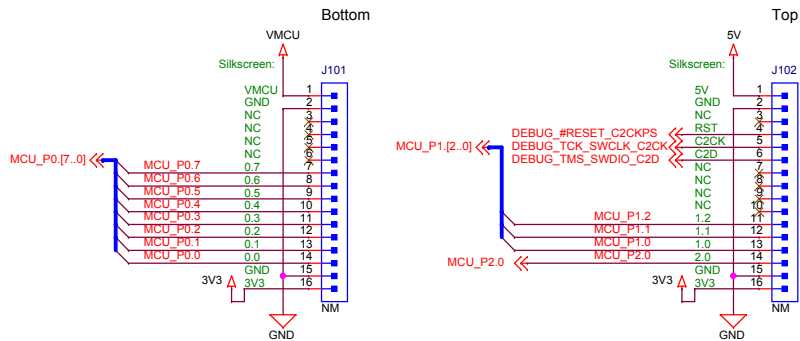
Bottom Row

2	VMCU		
4	NC		CMP1.0/ADC0.5
6	NC		CMP0.2/ADC0.4
8	NC		CMP0.4
10	NC		CMP1.0/ADC0.6
12	P0.4	UART_TX	CMP0.1/ADC0.2
14	P0.5	UART_RX	CMP0.3/ADC0.3
16	P1.1	I2C_SDA	CMP1.1/ADC0.7
18	5V		
20	3V3		

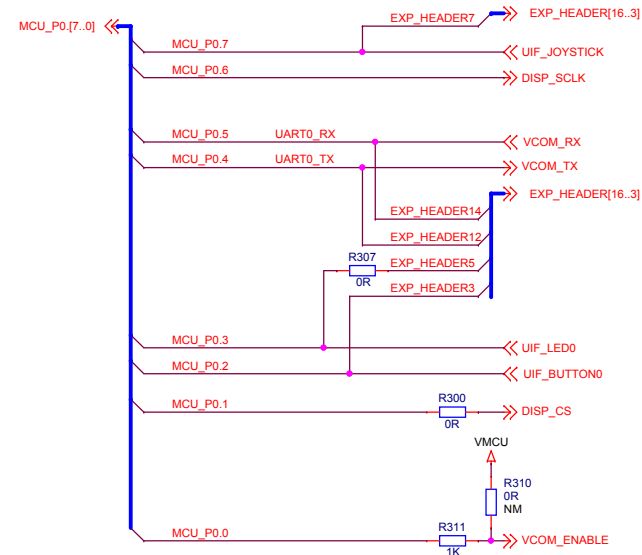


 SILICON LABS		Board Name	
		EFM8BB50 Pro Kit	
Designed		Page Title	
PEP		User Interface	
Approved		Board Number	
RGU		BRD5208A	
Size	Sheet Modified Date	Revision	
A3	Friday, July 30, 2021	A00	
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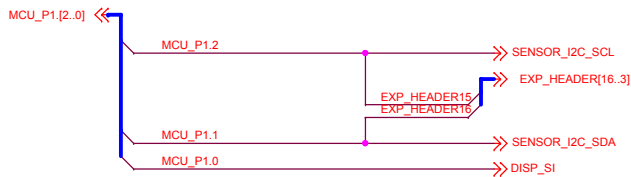
Breakout Connections



P0 Connections



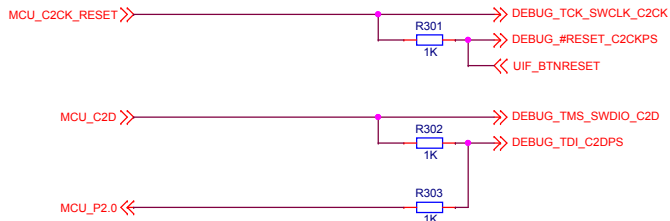
P1 Connections



P2 Connections

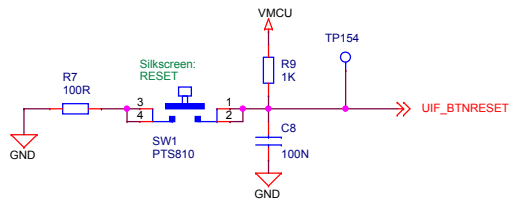


Debug Connections



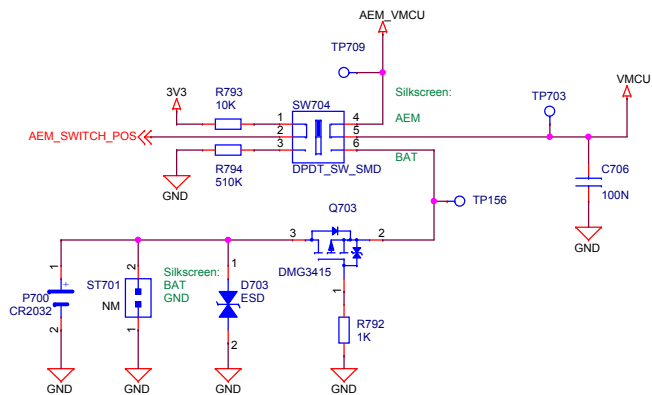
		Board Name	
		EFM8BB50 Pro Kit	
Designed PEP		Page Title	
Size A3		Signal Assignments	
Sheet Modified Date Friday, July 30, 2021		Board Number	
		BRD5208A	
		Revision	
		A00	
		Sheet	
		3 of 11	

Reset Push Button

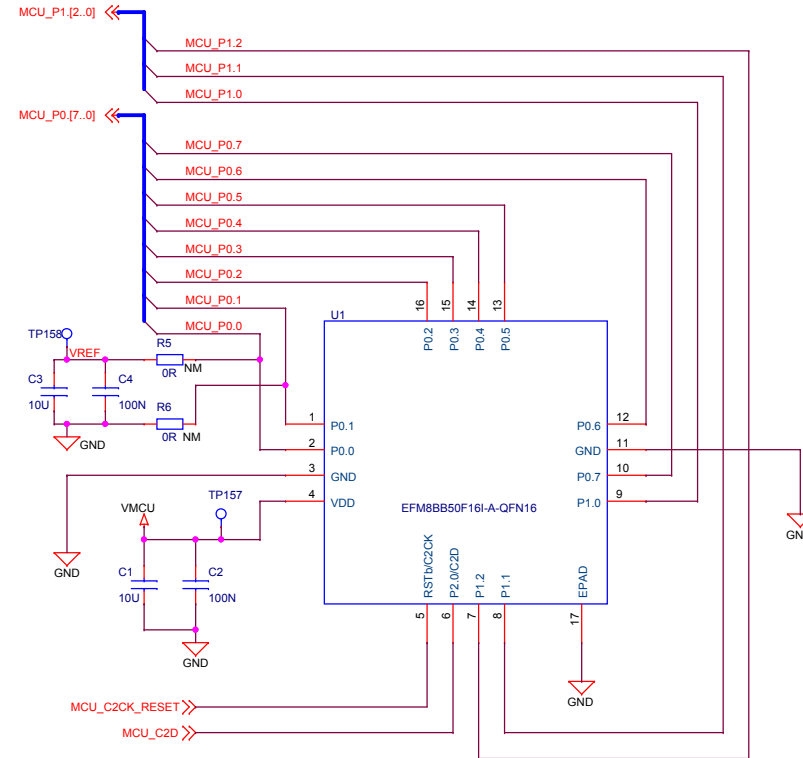


Power Select Switch: AEM/BAT

SWITCH POS	MODE DESCRIPTION
AEM	AEM Enabled, VMCU sourced from external 3.3V LDO powered by BC USB 5V supply
BAT	AEM Disabled, VMCU sourced from coin-cell battery or external power supply



EFM8 I/O



		Board Name	
		EFM8BB50 Pro Kit	
Designed PEP		Page Title	
Size A3		EFM8 Power & I/O	
Sheet Modified Date Wednesday, August 18, 2021		Board Number	Revision
		BRD5208A	A00
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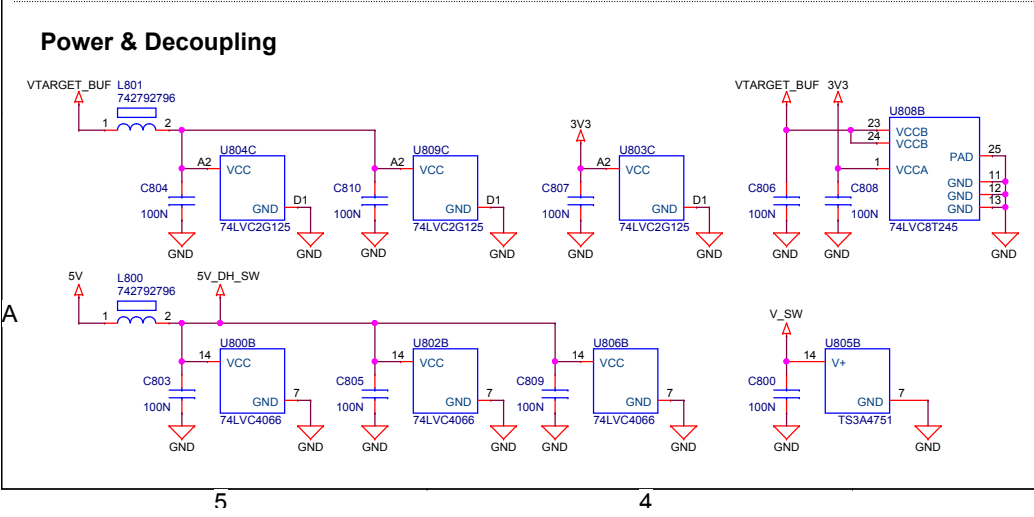
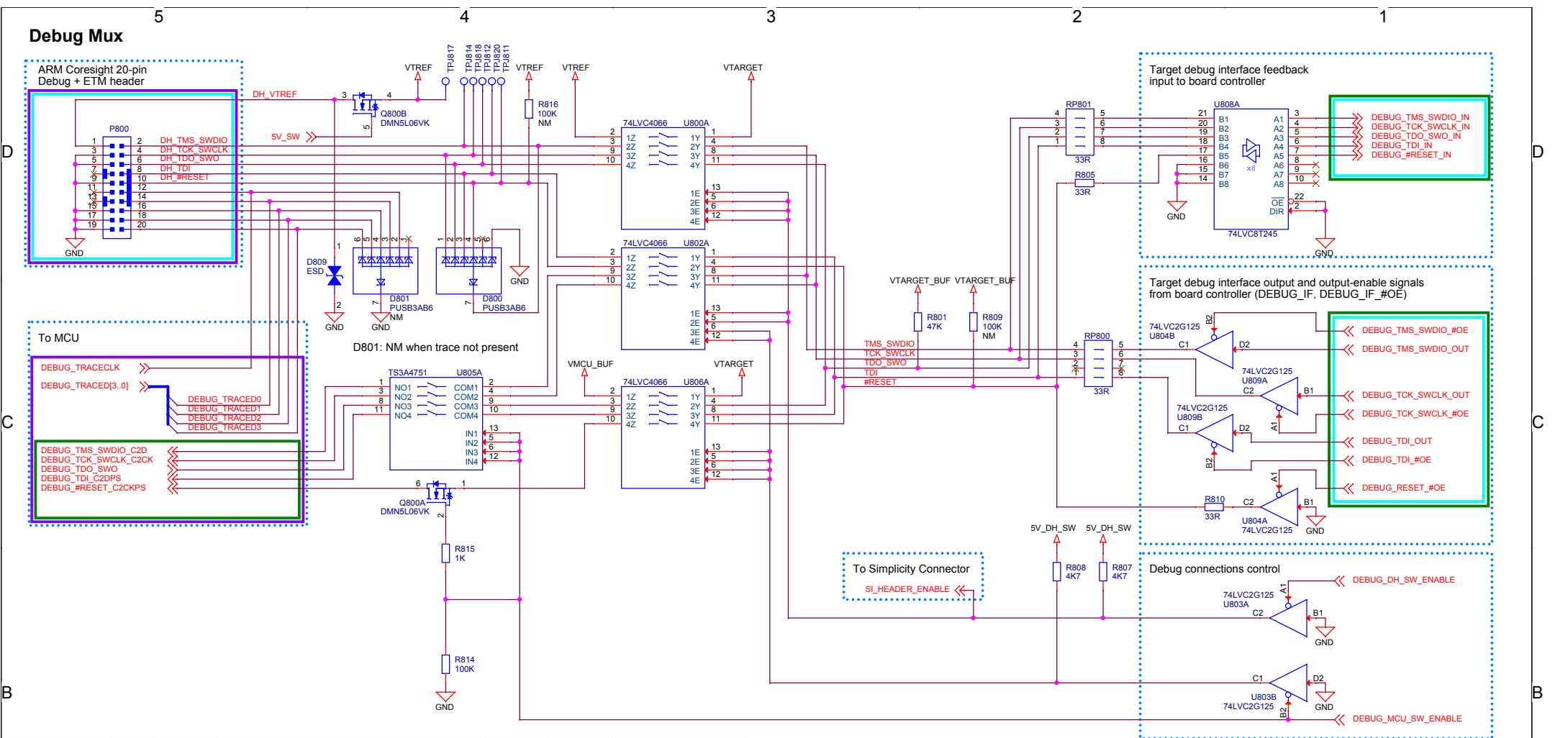
A



Calibration currents include contribution from sense and bleeder resistors.

A





Mode	DEBUG_DH_SW_ENABLE	DEBUG_MCU_SW_ENABLE	DEBUG_IF_#OE	VTREF	VTARGET
Debug Out	1	0	0/1	External voltage	External voltage
MCU Debug	0	1	0/1	Disconnected	VMCU
Debug In	1	1	1	VMCU	VMCU
Debug Off	0	0	1	-	-

Color coded frames indicates which groups of signal nodes that are active in a given debug mode



SILICON LABS

Board Name
EFM8BB50 Pro Kit

Page Title
Debug Interface

Board Number
BRD5208A

Revision
A00

Designed
PEP

Approved
RGU

Size
A3

Sheet Modified Date
Friday, July 30, 2021

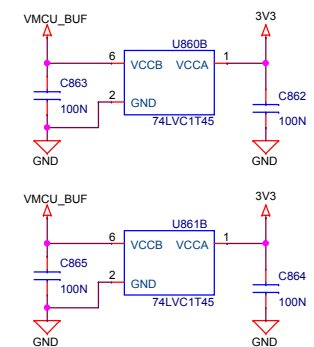
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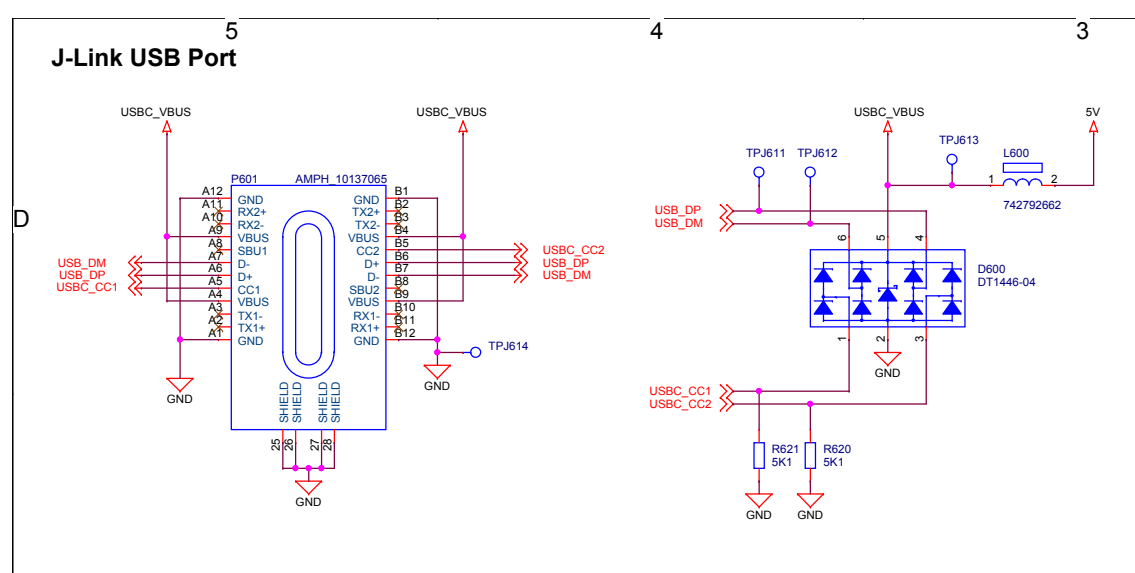
Sheet
7 of 11

A



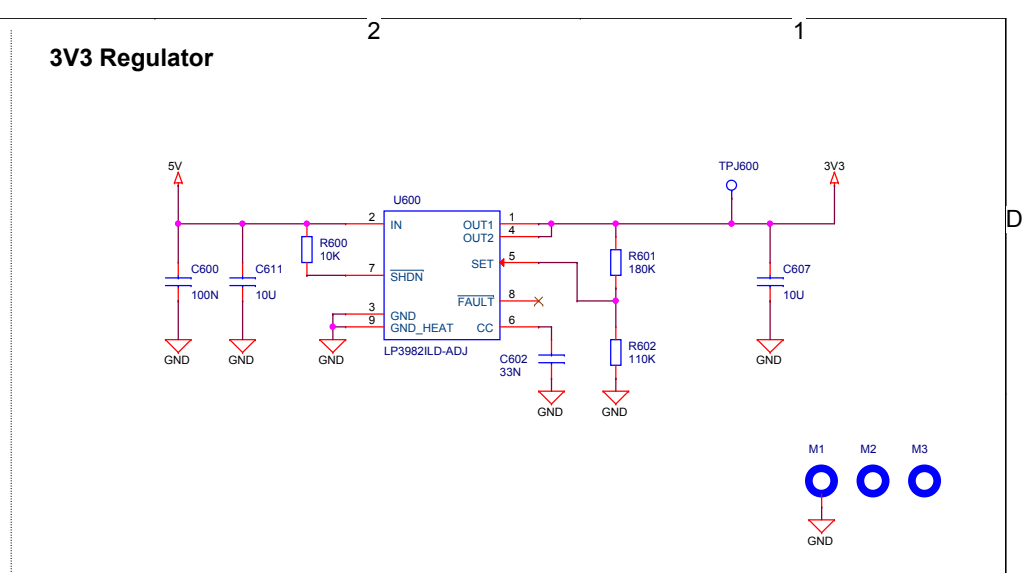
2

Sheet
8 of 11



3V3 Regulator

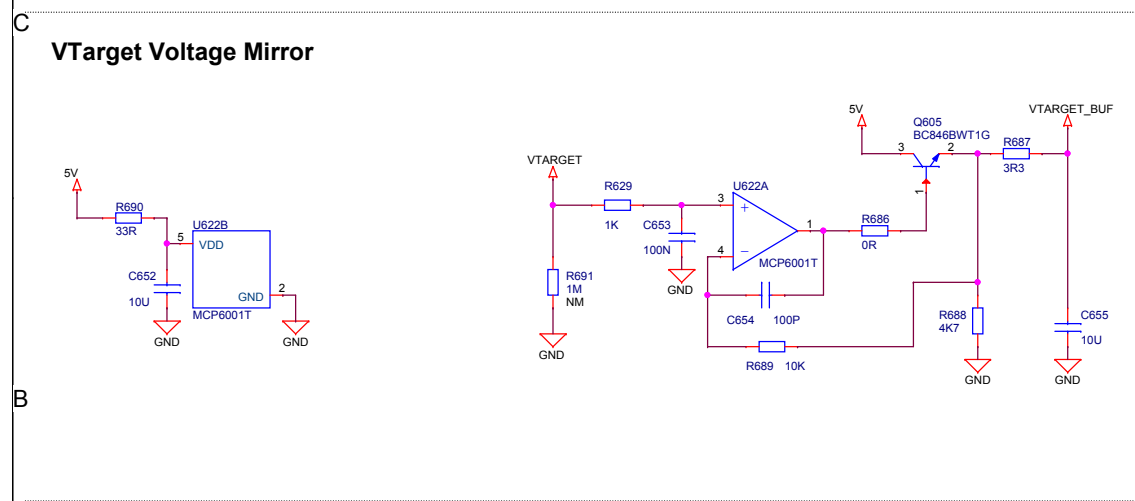
The schematic diagram illustrates a 3V3 Regulator circuit. The circuit is powered by a 5V supply. The input to the LP3982ILD-ADJ (U600) regulator is connected to the 5V supply through a 100nF capacitor (C600) and a 10uF capacitor (C611). The input is also connected to the regulator's IN pin (pin 2) through a 10k resistor (R600). The regulator's SHDN pin (pin 7) is connected to GND. The regulator's GND pin (pin 3) is connected to GND. The regulator's GND_HEAT pin (pin 9) is connected to GND. The regulator's OUT1 pin (pin 1) is connected to the 3V3 output through a 180k resistor (R601). The regulator's OUT2 pin (pin 4) is connected to the 3V3 output. The regulator's SET pin (pin 5) is connected to the 3V3 output through a 110k resistor (R602). The regulator's FAULT pin (pin 8) is connected to GND through a 33nF capacitor (C602). The regulator's CC pin (pin 6) is connected to GND. The 3V3 output is connected to a TPJ600 test point and a 10uF capacitor (C607) to GND. Three LEDs (M1, M2, M3) are connected to the 3V3 output through current-limiting resistors.



C

VTARGET Voltage Mirror

B



Power Supply for Analog Switches

Analog switches used for isolation are powered by 3V6_SW when the USB cable is connected, otherwise by VMCU.

J-Link USB Cable	PMOS State	NMOS State	V_SW	VMCU_SENSE
Connected	Off	On	3.6V	VMCU
Disconnected	On	Off	VMCU	Isolated

Power Supply for Analog Switches

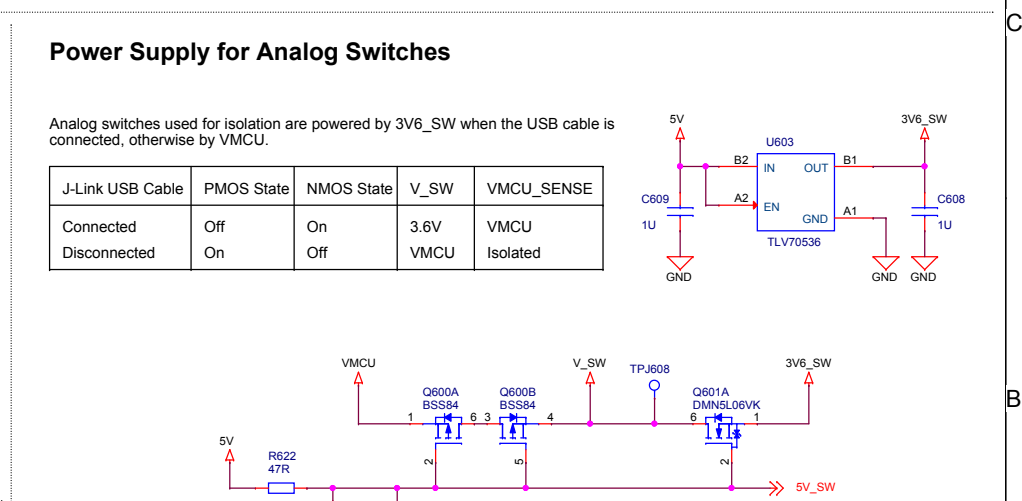
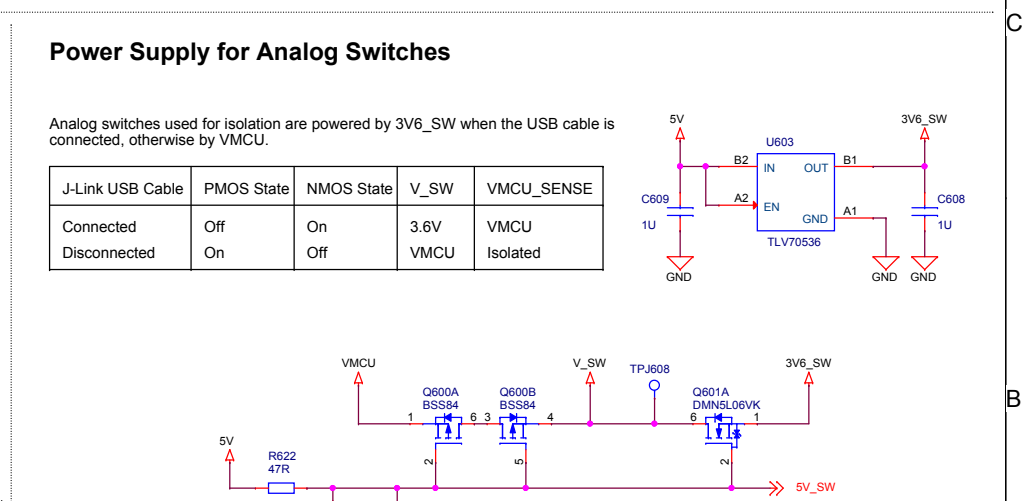
Analog switches used for isolation are powered by 3V6_SW when the USB cable is connected, otherwise by VMCU.

J-Link USB Cable	PMOS State	NMOS State	V_SW	VMCU_SENSE
Connected	Off	On	3.6V	VMCU
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Power Supply for Analog Switches

Analog switches used for isolation are powered by 3V6_SW when the USB cable is connected, otherwise by VMCU.

J-Link USB Cable	PMOS State	NMOS State	V_SW	VMCU_SENSE
Connected	Off	On	3.6V	VMCU
Disconnected	On	Off	VMCU	Isolated



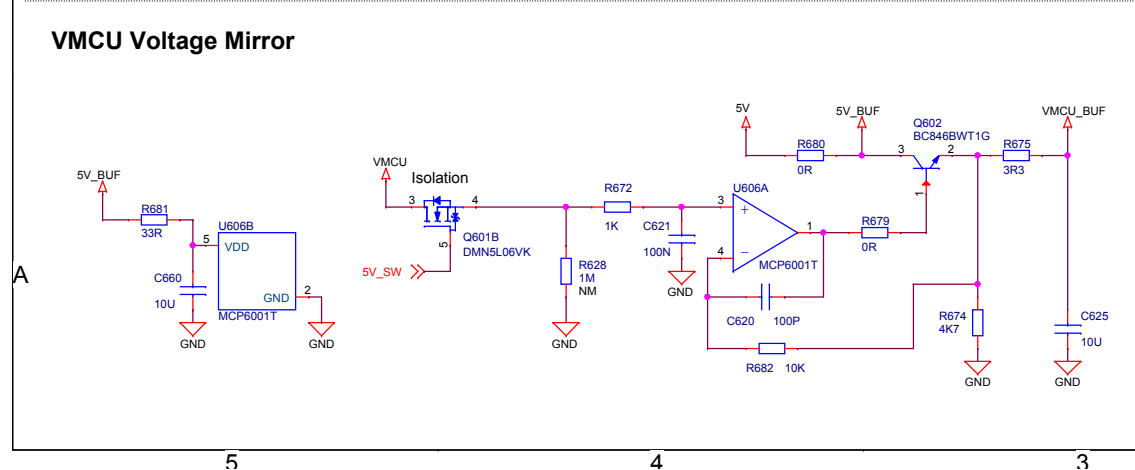
VMCU Voltage Mirror

The schematic diagram illustrates the VMCU Voltage Mirror circuit, which is divided into three main sections labeled 5, 4, and 3.

Section 5: The input signal 5V_BUF is connected to a 33R resistor (R681) and a 10U capacitor (C660) to ground. The signal then passes through the VDD pin (pin 5) of the MCP6001T op-amp (U060B). The op-amp's GND pin (pin 2) is connected to ground.

Section 4: The op-amp's output (pin 1) is connected to a 100P capacitor (C620) to ground and a 10K resistor (R682) to a 5V supply. The output also passes through a 1K resistor (R672) to a 5V_SW input, which is connected to an isolation switch (Q601B, DMN5L06VK). The switch's other terminal (pin 4) is connected to a 1M resistor (R628) to ground.

Section 3: The signal path continues through a 0R resistor (R679) to a BC846BWT1G transistor (Q602). The transistor's base (pin 3) is connected to a 5V_BUF input and a 0R resistor (R680). The transistor's emitter (pin 1) is connected to ground. The collector (pin 2) is connected to a 3R3 resistor (R675) and a 4K7 resistor (R674) to ground. The final output is VMCU_BUF, which is connected to a 10U capacitor (C625) to ground.



 SILICON LABS		Board Name EFM8BB50 Pro Kit	
		Page Title Power	
Designed PEP		Approved RGJ	
Size A3	Sheet Modified Date Friday, July 30, 2021	Board Number BRD5208A	Revision A00
COPYRIGHT SILICON LABORATORIES INC. 2021		CONFIDENTIAL – SUBJECT TO TERMS OF USE	
		Sheet 9 of 11	

 SILICON LABS		Board Name EFM8BB50 Pro Kit	
		Page Title Power	
Designed PEP		Approved RGJ	
Size A3	Sheet Modified Date Friday, July 30, 2021	Board Number BRD5208A	Revision A00
COPYRIGHT SILICON LABORATORIES INC. 2021		CONFIDENTIAL – SUBJECT TO TERMS OF USE	
		Sheet 9 of 11	

 SILICON LABS		Board Name EFM8BB50 Pro Kit	
		Page Title Power	
Designed PEP		Approved RGJ	
Size A3	Sheet Modified Date Friday, July 30, 2021	Board Number BRD5208A	Revision A00
COPYRIGHT SILICON LABORATORIES INC. 2021		CONFIDENTIAL – SUBJECT TO TERMS OF USE	
		Sheet 9 of 11	

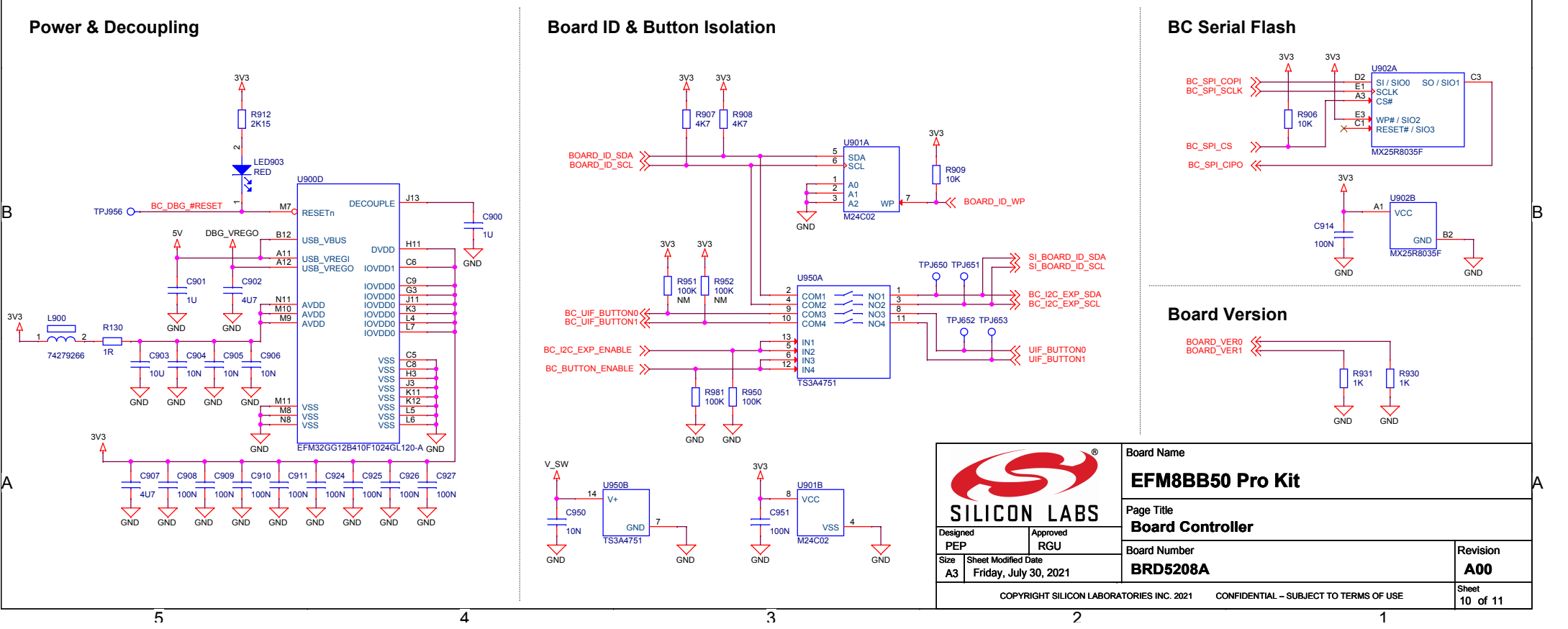
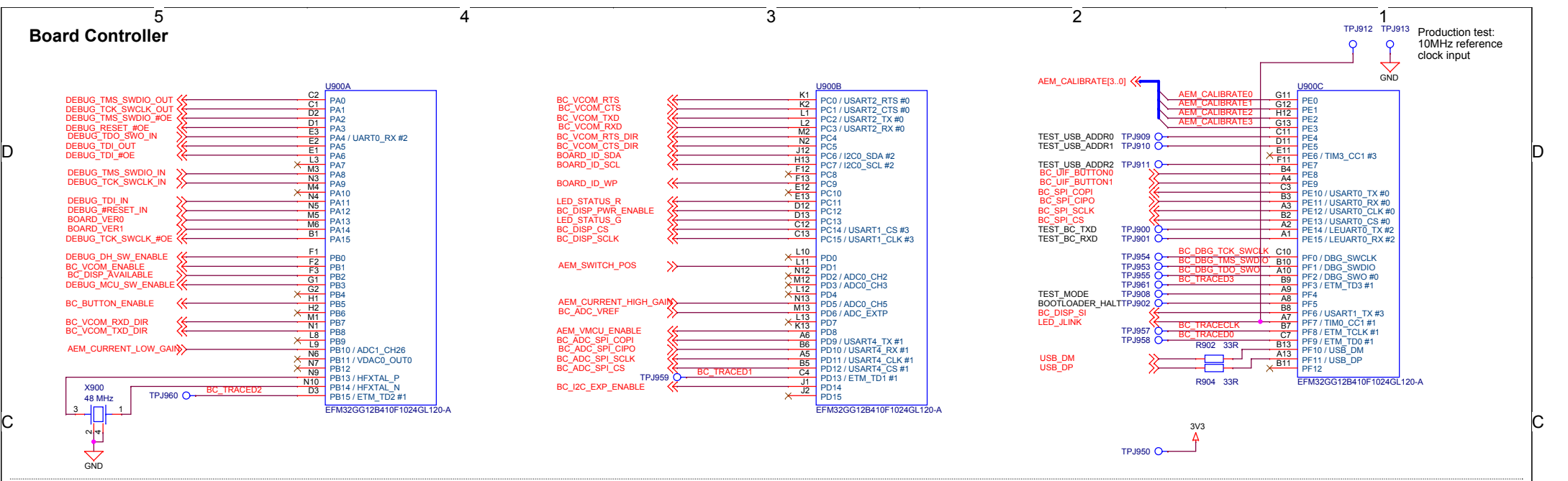
 SILICON LABS		Board Name EFM8BB50 Pro Kit	
		Page Title Power	
Designed PEP		Approved RGJ	
Size A3	Sheet Modified Date Friday, July 30, 2021	Board Number BRD5208A	Revision A00
COPYRIGHT SILICON LABORATORIES INC. 2021		CONFIDENTIAL – SUBJECT TO TERMS OF USE	
		Sheet 9 of 11	

 SILICON LABS		Board Name EFM8BB50 Pro Kit	
		Page Title Power	
Designed PEP		Approved RGU	
Size A3	Sheet Modified Date Friday, July 30, 2021	Board Number BRD5208A	Revision A00
COPYRIGHT SILICON LABORATORIES INC. 2021 CONFIDENTIAL – SUBJECT TO TERMS OF USE			Sheet 9 of 11

 SILICON LABS		Board Name EFM8BB50 Pro Kit	
		Page Title Power	
Designed PEP		Approved RGJ	
Size A3	Sheet Modified Date Friday, July 30, 2021	Board Number BRD5208A	Revision A00
COPYRIGHT SILICON LABORATORIES INC. 2021		CONFIDENTIAL – SUBJECT TO TERMS OF USE	
		Sheet 9 of 11	

 SILICON LABS		Board Name EFM8BB50 Pro Kit	
		Page Title Power	
Designed PEP		Approved RGU	
Size A3	Sheet Modified Date Friday, July 30, 2021	Board Number BRD5208A	Revision A00
COPYRIGHT SILICON LABORATORIES INC. 2021 CONFIDENTIAL – SUBJECT TO TERMS OF USE			Sheet 9 of 11

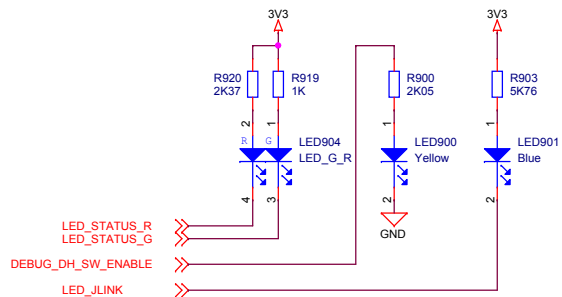
 SILICON LABS		Board Name EFM8BB50 Pro Kit	
		Page Title Power	
Designed PEP		Approved RGU	
Size A3	Sheet Modified Date Friday, July 30, 2021	Board Number BRD5208A	Revision A00
COPYRIGHT SILICON LABORATORIES INC. 2021 CONFIDENTIAL – SUBJECT TO TERMS OF USE			Sheet 9 of 11



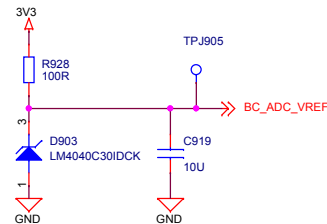
 SILICON LABS		Board Name EFM8BB50 Pro Kit	
		Page Title Board Controller	
Designed PEP	Approved RGU	Board Number BRD5208A	Revision A00
Size A3	Sheet Modified Date Friday, July 30, 2021	Sheet 10 of 11	

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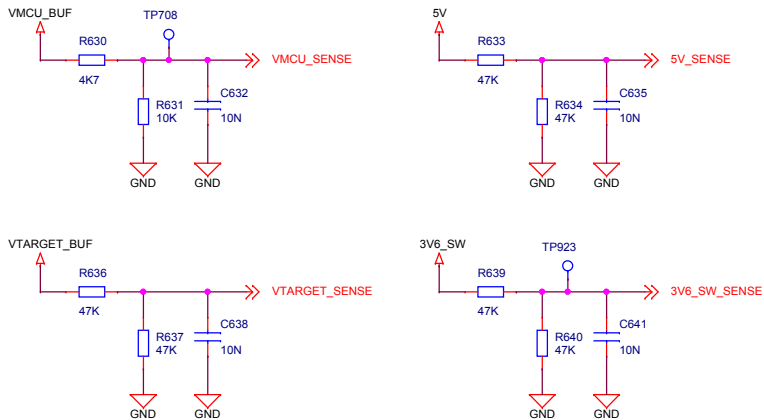
Indicator LEDs



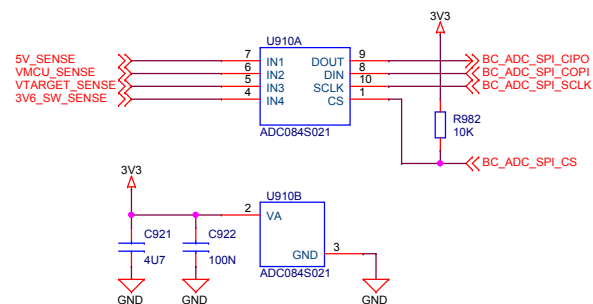
BC ADC Reference



BC Voltage Sense



BC Voltage Sense ADC



		Board Name	
		EFM8BB50 Pro Kit	
Designed PEP		Page Title	
Size A3		Board Controller Misc	
Sheet Modified Date Friday, July 30, 2021		Board Number	Revision
		BRD5208A	A00
COPYRIGHT SILICON LABORATORIES INC. 2021 CONFIDENTIAL – SUBJECT TO TERMS OF USE			Sheet 11 of 11