



EFM8BB50 Pro Kit	
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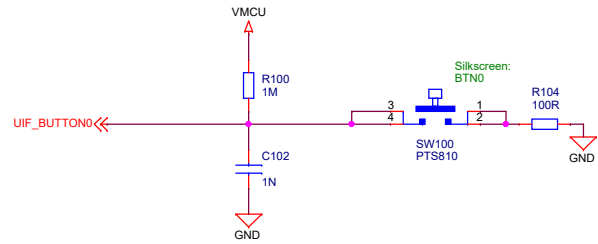


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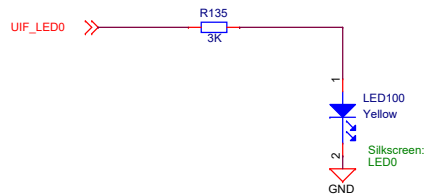
Revision History	
Rev.	Description
A00	Initial version
A01	Update U1

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		EFM8BB50 Pro Kit	
Designed MAH		Approved RGU	
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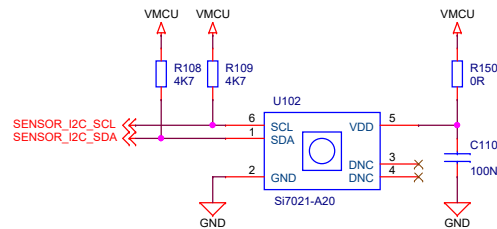
Push Buttons



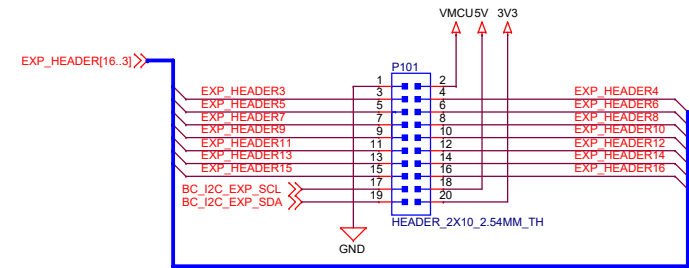
User LEDs



Relative Humidity & Temperature Sensor



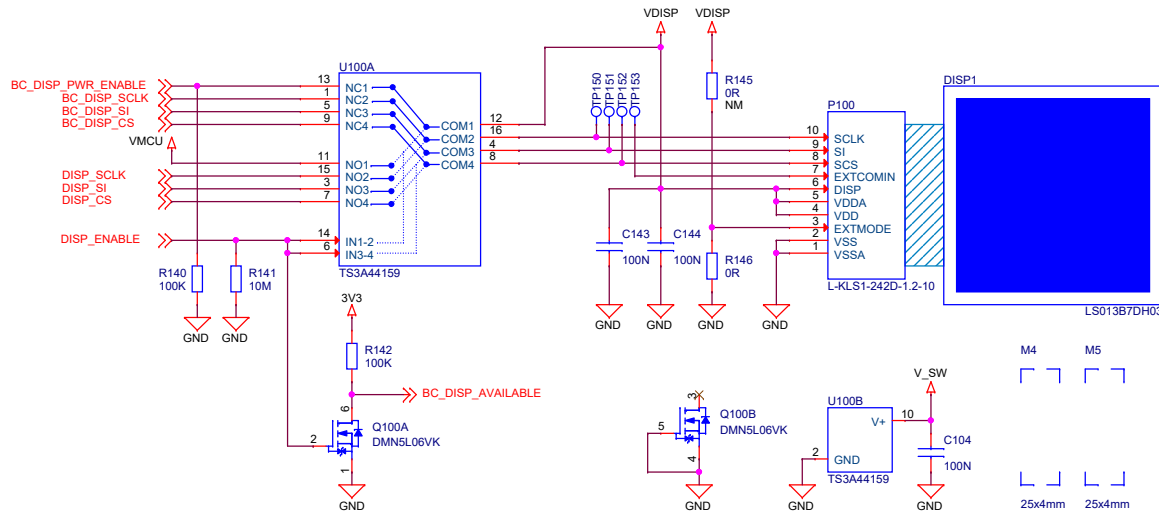
EXP Header



EXP Header Functionality

Top Row			
1	GND		
3	P0.2	BTN	
5	P0.3	LED	
7	P0.7	JOYSTICK	
9	NC		CMP1.2/ADC0.11
11	NC		
13	NC		
15	P1.2	I2C_SCL	CMP1.1/ADC0.8
17	Reserved for EXP Board Identification		
19	Reserved for EXP Board Identification		
Bottom Row			
2	VMCU		
4	NC		CMP1.0/ADC0.5
6	NC		CMP0.2/ADC0.4
8	NC		CMP0.4
10	NC		CMP1.0/ADC0.6
12	P0.4	UART_TX	CMP0.1/ADC0.2
14	P0.5	UART_RX	CMP0.3/ADC0.3
16	P1.1	I2C_SDA	CMP1.1/ADC0.7
18	5V		
20	3V3		

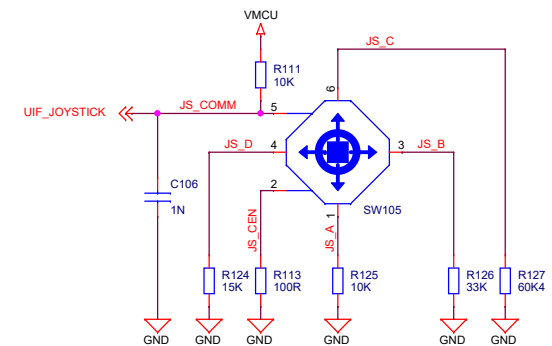
Memory LCD-TFT Display & Multiplexer



The EFM8 always controls ownership of the display using the DISP_ENABLE signal.

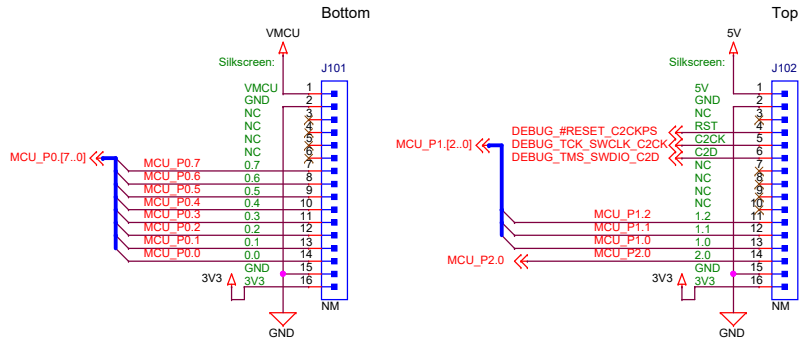
DISP_ENABLE	Connected	VDISP	BC_DISP_AVAILABLE
1	MCU	VMCU	GND
0	BC	BC_DISP_PWR_ENABLE	3V3

Analog Joystick

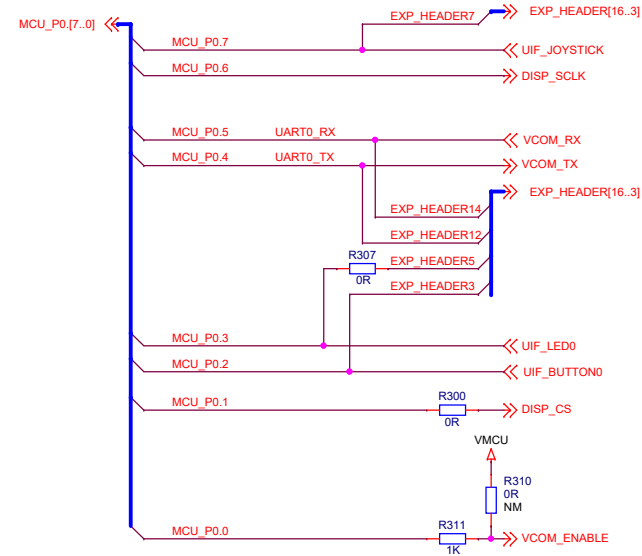


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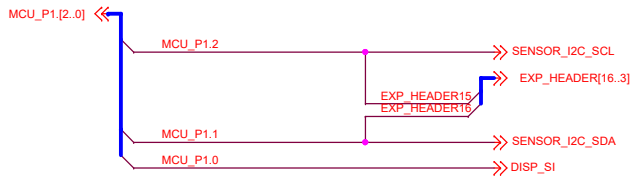
Breakout Connections



P0 Connections



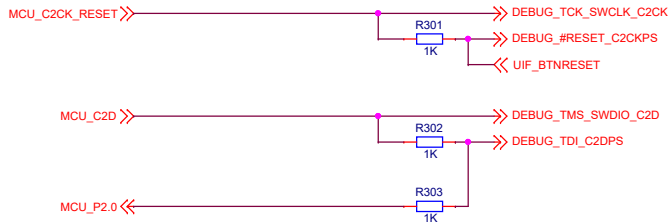
P1 Connections




P2 Connections

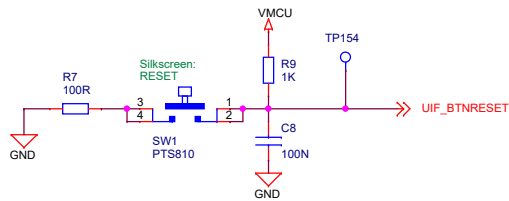


Debug Connections



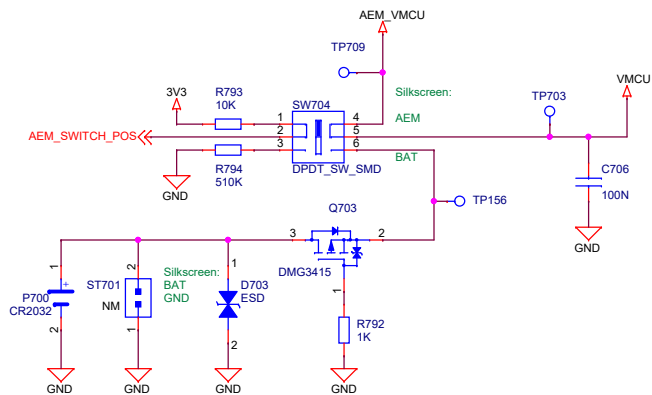
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Reset Push Button

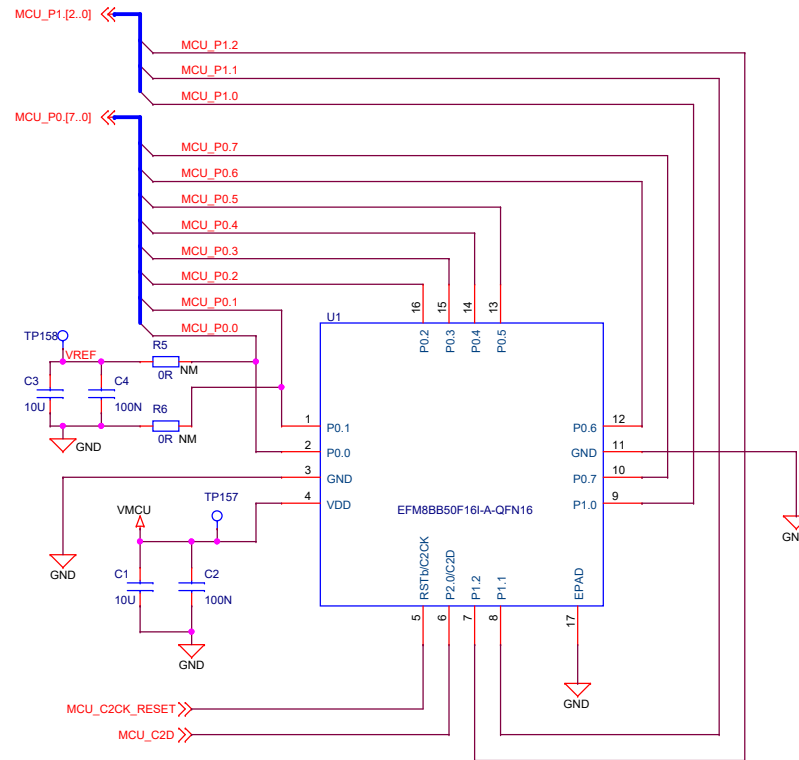



Power Select Switch: AEM/BAT

SWITCH POS	MODE DESCRIPTION
AEM	AEM Enabled, VMCU sourced from external 3.3V LDO powered by BC USB 5V supply
BAT	AEM Disabled, VMCU sourced from coin-cell battery or external power supply

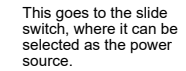


EFM8 I/O



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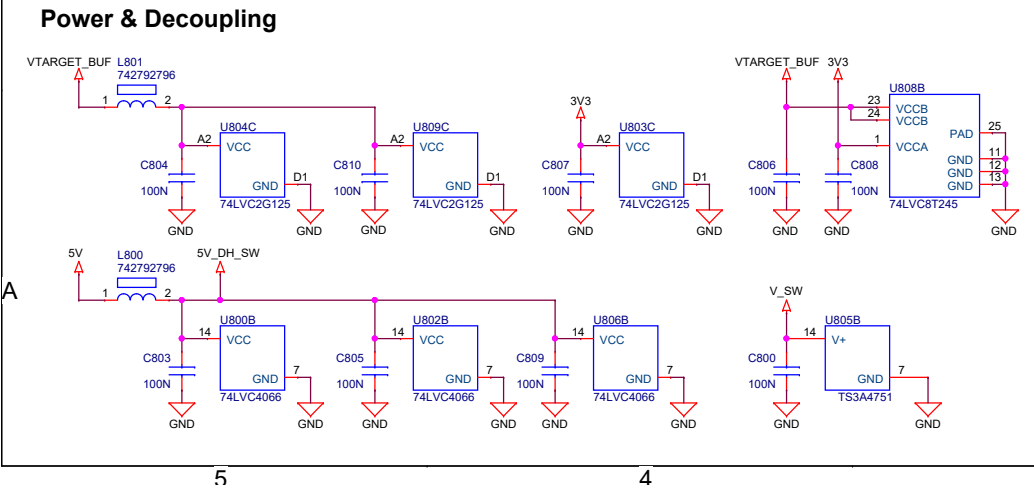
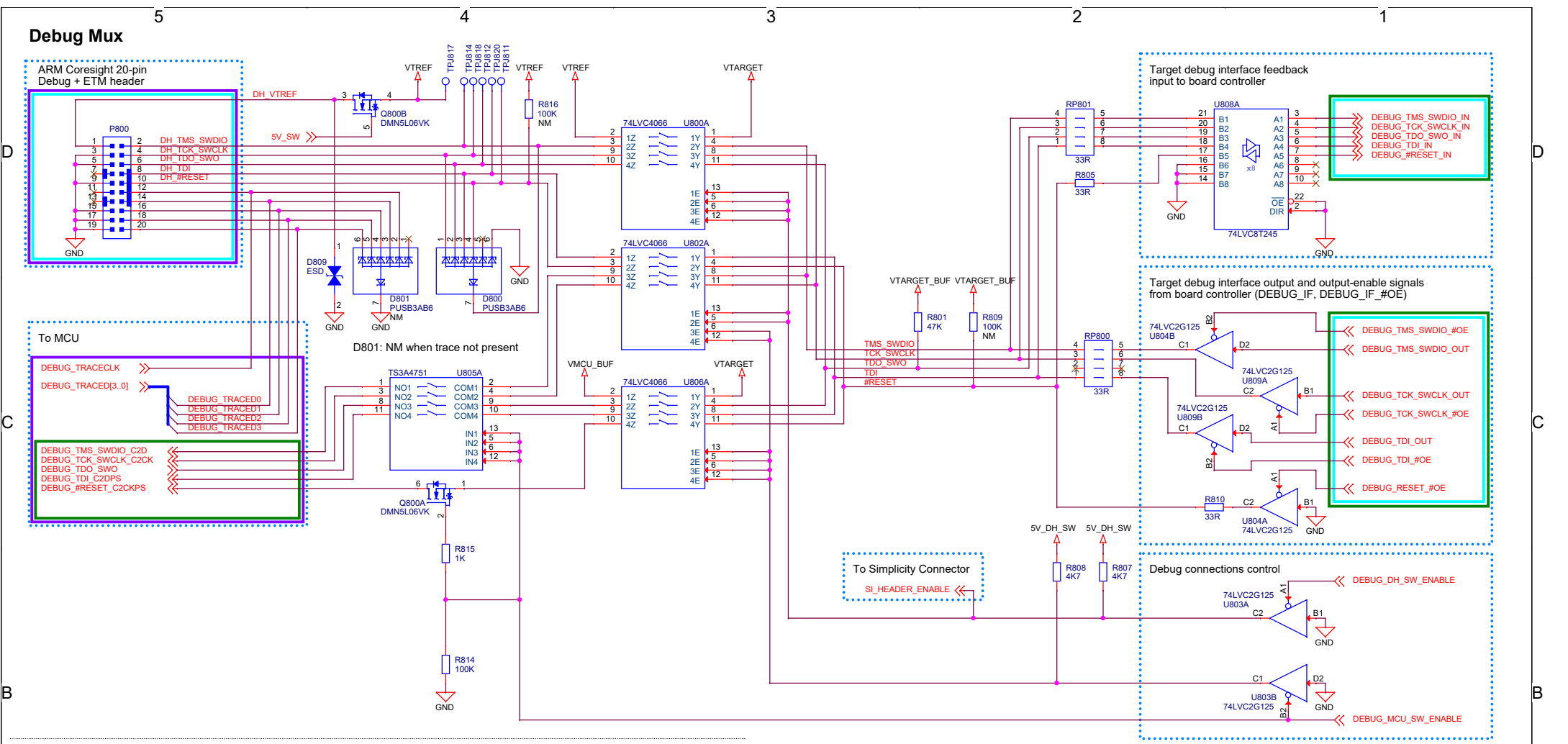


Calibration currents include contribution from sense and bleeder resistors.




A





Mode	DEBUG_DH_SW_ENABLE	DEBUG_MCU_SW_ENABLE	DEBUG_IF_#OE	VTREF	VTARGET
Debug Out	1	0	0/1	External voltage	External voltage
MCU Debug	0	1	0/1	Disconnected	VMCU
Debug In	1	1	1	VMCU	VMCU
Debug Off	0	0	1	-	-

Color coded frames indicates which groups of signal nodes that are active in a given debug mode



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Debug Interface

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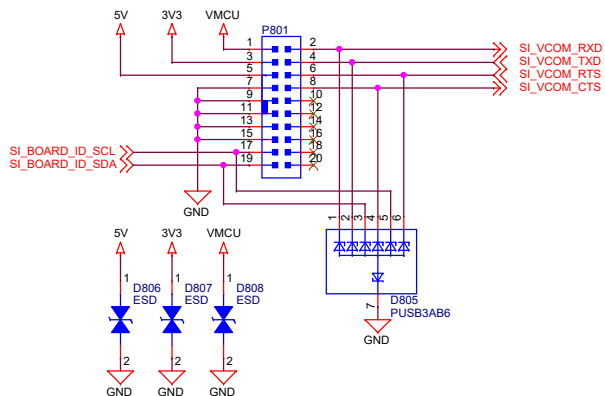
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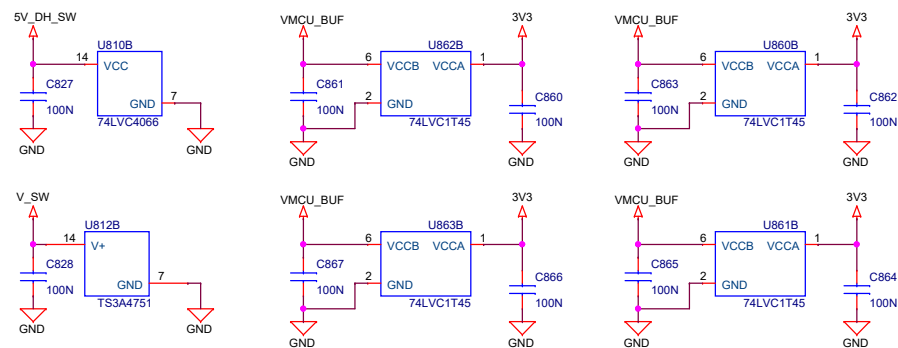
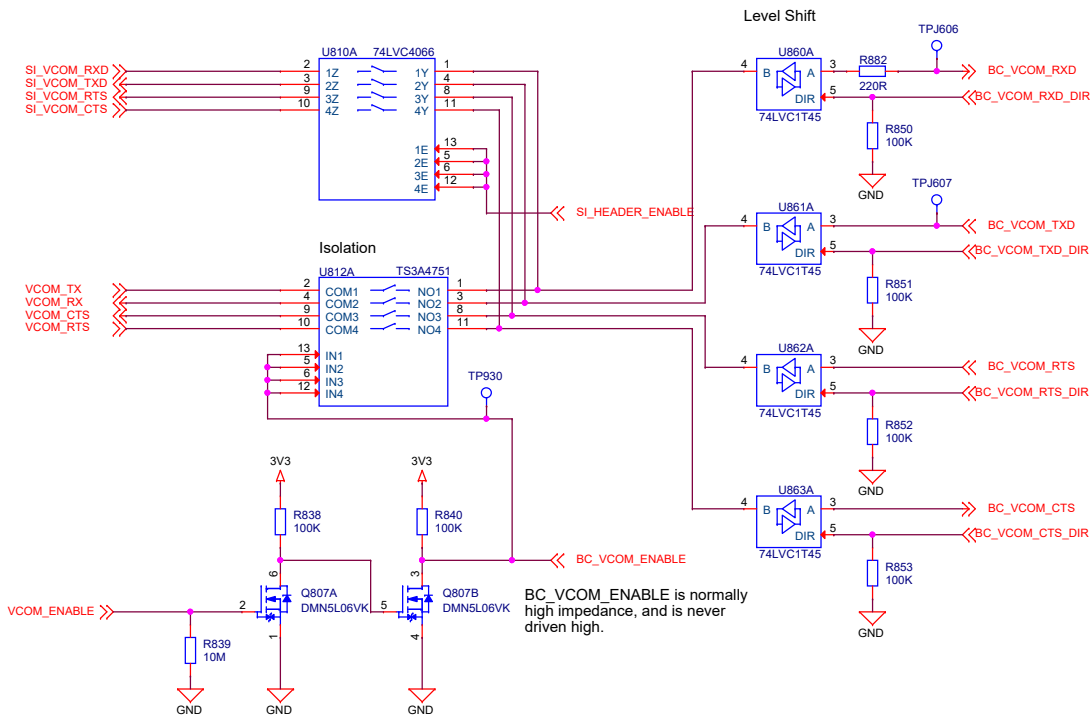
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Simplicity Connector



VCOM Interface



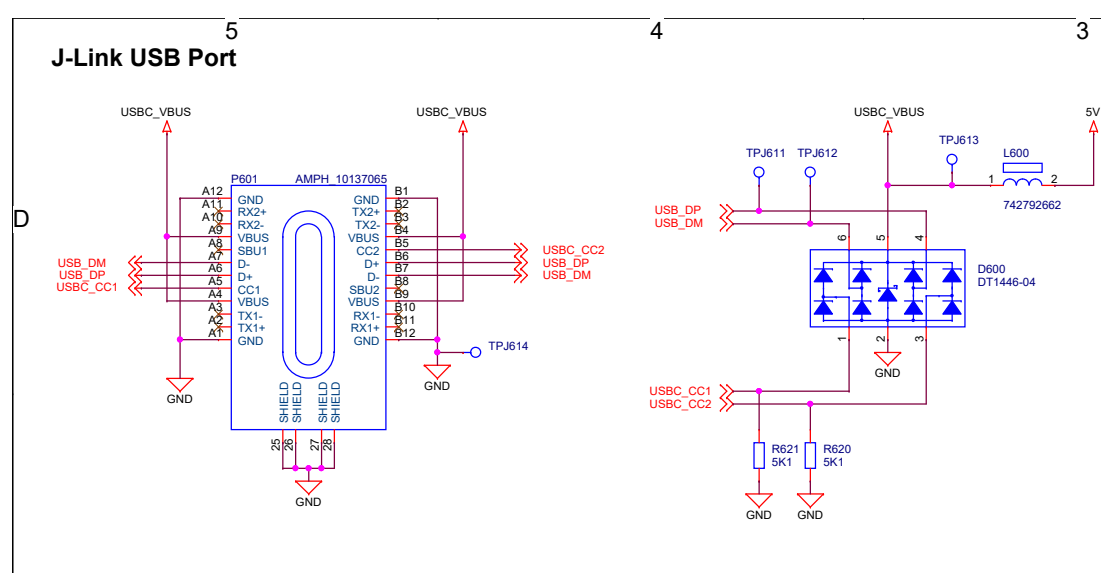
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The image displays three circuit diagrams, labeled 5, 4, and 3, showing the J-Link USB Port connection for different boards.

Diagram 5 (Left): Shows the connection for a board with a P601 AMPH 10137065. The USB DM, DP, and CC1 signals are connected to the board's A12, A11, A10, A9, A8, A7, A6, A5, A4, A3, A2, and A1 pins. The USB VBUS is connected to the board's B1, B2, B3, B4, B5, B6, B7, B8, B9, B10, B11, and B12 pins. The board's shield is connected to ground. The USB DP and DM signals are connected to the board's B1, B2, B3, B4, B5, B6, B7, B8, B9, B10, B11, and B12 pins. The USB CC1 signal is connected to the board's A12, A11, A10, A9, A8, A7, A6, A5, A4, A3, A2, and A1 pins. The USB VBUS is connected to the board's B1, B2, B3, B4, B5, B6, B7, B8, B9, B10, B11, and B12 pins. The board's shield is connected to ground. The USB DP and DM signals are connected to the board's B1, B2, B3, B4, B5, B6, B7, B8, B9, B10, B11, and B12 pins. The USB CC1 signal is connected to the board's A12, A11, A10, A9, A8, A7, A6, A5, A4, A3, A2, and A1 pins. The USB VBUS is connected to the board's B1, B2, B3, B4, B5, B6, B7, B8, B9, B10, B11, and B12 pins. The board's shield is connected to ground.

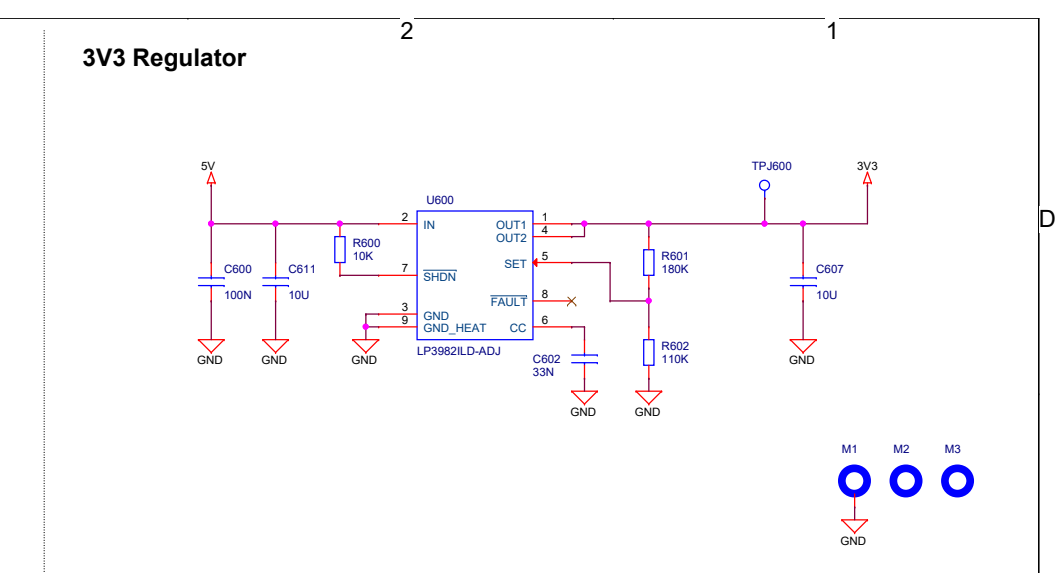
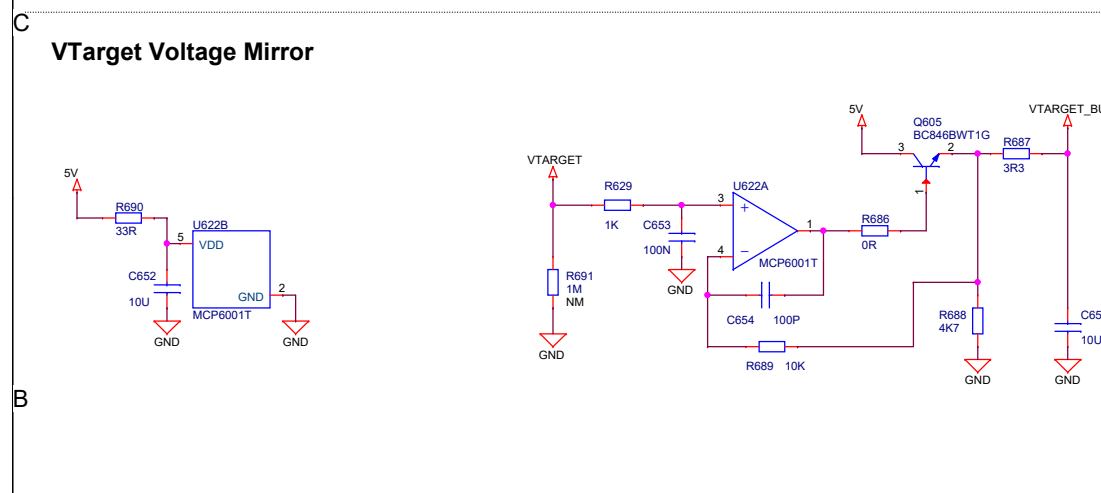
Diagram 4 (Middle): Shows the connection for a board with a D600 DT1446-04. The USB DM, DP, and CC1 signals are connected to the board's 1, 2, and 3 pins. The USB VBUS is connected to the board's 4, 5, and 6 pins. The board's shield is connected to ground. The USB DP and DM signals are connected to the board's 1, 2, and 3 pins. The USB CC1 signal is connected to the board's 4, 5, and 6 pins. The USB VBUS is connected to the board's 1, 2, and 3 pins. The board's shield is connected to ground.

Diagram 3 (Right): Shows the connection for a board with a D600 DT1446-04. The USB DM, DP, and CC1 signals are connected to the board's 1, 2, and 3 pins. The USB VBUS is connected to the board's 4, 5, and 6 pins. The board's shield is connected to ground. The USB DP and DM signals are connected to the board's 1, 2, and 3 pins. The USB CC1 signal is connected to the board's 4, 5, and 6 pins. The USB VBUS is connected to the board's 1, 2, and 3 pins. The board's shield is connected to ground.



3V3 Regulator

The schematic diagram illustrates a 3V3 Regulator circuit. The circuit is powered by a 5V supply. The input to the regulator (U600, LP3982ILD-ADJ) is connected to the 5V supply through a 100nF capacitor (C600) and a 10uF capacitor (C611). The input is also connected to the regulator's IN pin (pin 2) through a 10k resistor (R600). The regulator's SHDN pin (pin 7) is connected to GND. The regulator's GND pins (pins 3 and 9) are connected to GND. The regulator's GND_HEAT pin (pin 8) is connected to GND. The regulator's CC pin (pin 6) is connected to GND through a 33nF capacitor (C602). The regulator's OUT1 pin (pin 1) is connected to the 3V3 output through a 180k resistor (R601). The regulator's OUT2 pin (pin 4) is connected to the 3V3 output. The regulator's SET pin (pin 5) is connected to the 3V3 output through a 180k resistor (R601). The regulator's FAULT pin (pin 8) is connected to GND through a 110k resistor (R602). The 3V3 output is connected to a 10uF capacitor (C607) and a TPJ600 test point. The 3V3 output is also connected to three LEDs (M1, M2, M3) through a common GND connection.

[illegible]

Power Supply for Analog Switches

Analog switches used for isolation are powered by 3V6_SW when the USB cable is connected, otherwise by VMCU.

J-Link USB Cable	PMOS State	NMOS State	V_SW	VMCU_SENSE
Connected	Off	On	3.6V	VMCU
Disconnected	On	Off	VMCU	Isolated

Power Supply for Analog Switches

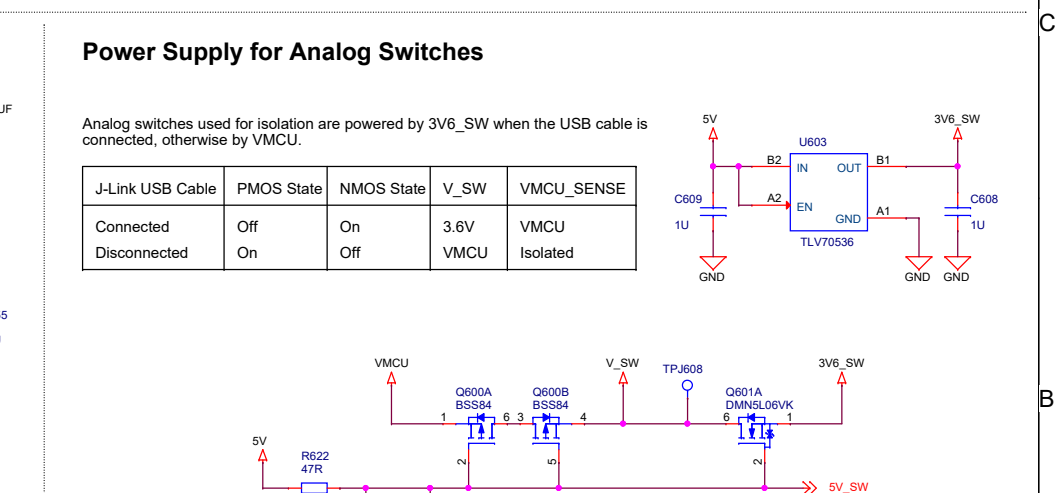
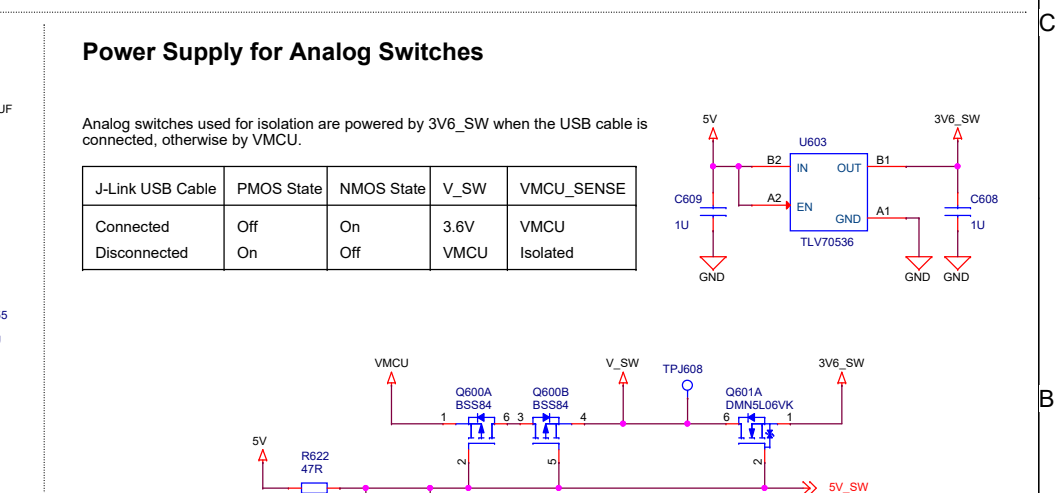
Analog switches used for isolation are powered by 3V6_SW when the USB cable is connected, otherwise by VMCU.

J-Link USB Cable	PMOS State	NMOS State	V_SW	VMCU_SENSE
Connected	Off	On	3.6V	VMCU
Disconnected	On	Off	VMCU	Isolated

Power Supply for Analog Switches

Analog switches used for isolation are powered by 3V6_SW when the USB cable is connected, otherwise by VMCU.

J-Link USB Cable	PMOS State	NMOS State	V_SW	VMCU_SENSE
Connected	Off	On	3.6V	VMCU
Disconnected	On	Off	VMCU	Isolated



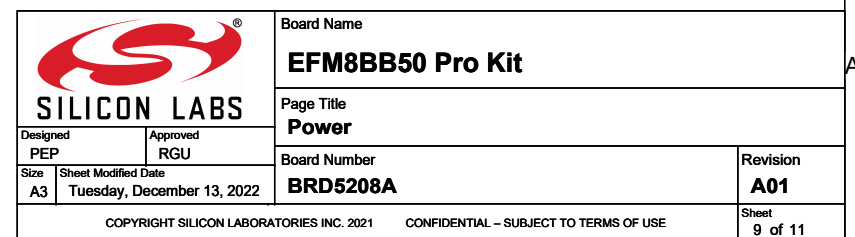
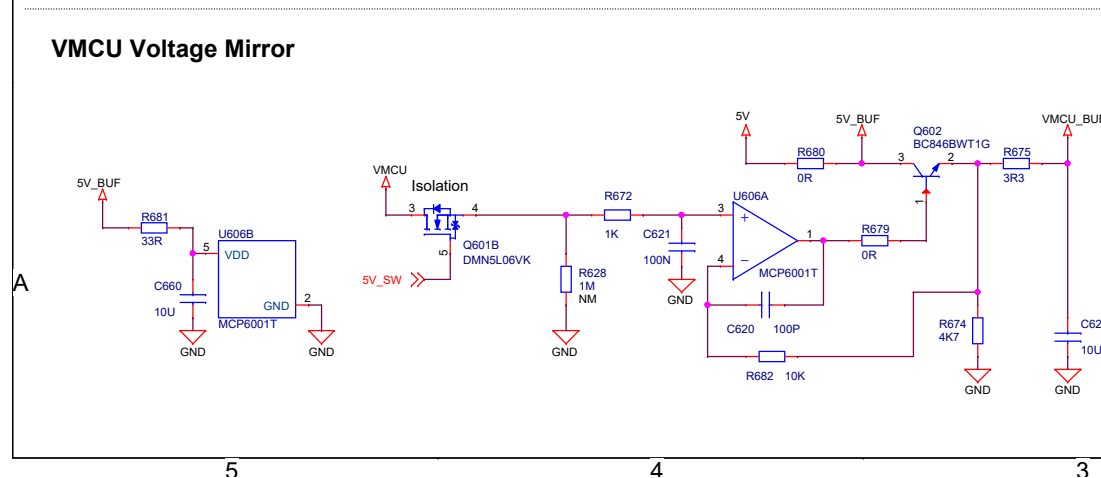
VMCU Voltage Mirror


The schematic diagram illustrates the VMCU Voltage Mirror circuit, which is divided into three main sections labeled 5, 4, and 3.

Section 5: The 5V_BUF input is connected to a 33R resistor (R681) and a 10uF capacitor (C660) to ground. The other end of the capacitor is connected to the VDD pin (pin 5) of the MCP6001T op-amp (U606B). The op-amp's GND pin (pin 2) is connected to ground.


Section 4: The VMCU input is connected to an isolation buffer (Q601B, DMN5L06VK) and a 1M resistor (R628) to ground. The output of the isolation buffer is connected to the non-inverting input (pin 3) of the MCP6001T op-amp. The op-amp's inverting input (pin 4) is connected to a 100nF capacitor (C621) to ground and a 100pF capacitor (C620) to the output. The output (pin 1) is connected to a 10K resistor (R682) to ground and a 4K7 resistor (R674) to the VMCU_BUF output.


Section 3: The VMCU_BUF output is connected to a 3R3 resistor (R675) to ground and a 10uF capacitor (C62) to ground. A 5V supply is connected to the VMCU_BUF output through a 33R resistor (R681) and a 10uF capacitor (C660) to ground. The VMCU_BUF output is also connected to a 3R3 resistor (R675) to ground and a 10uF capacitor (C62) to ground.





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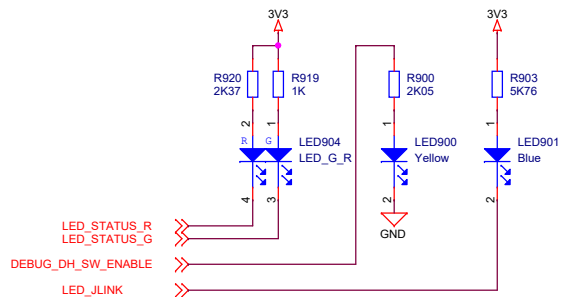
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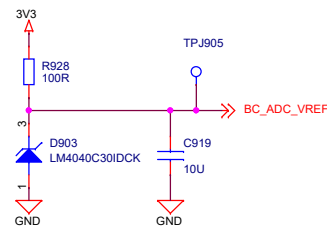
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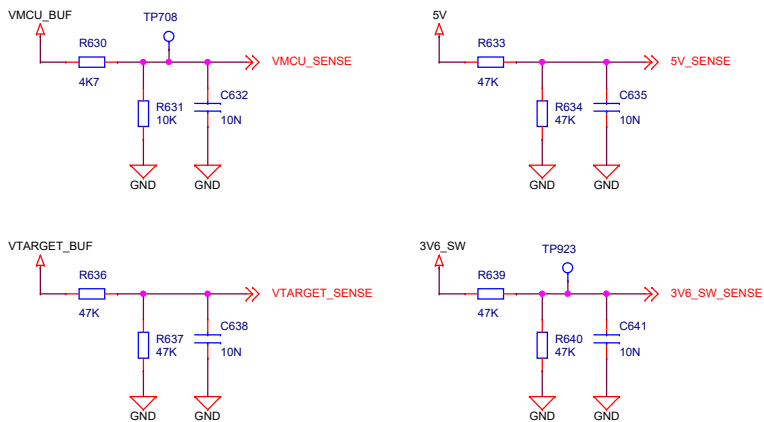
Indicator LEDs



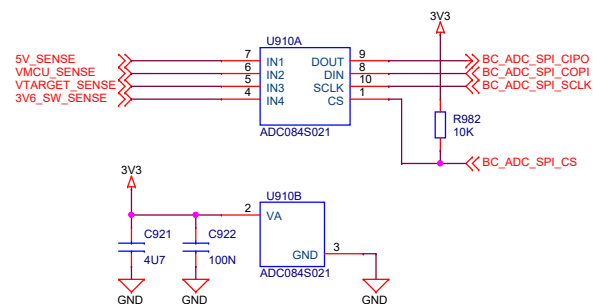
BC ADC Reference



BC Voltage Sense



BC Voltage Sense ADC



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