EFP0108 Evaluation Board

Single-Cell Boost Configuration

Board Function	Page
Title Page	1
EFP01	2
Host MCU	3
Debugger & Board Power	4

Revision History

Rev.	Description
A00	Initial version.
A01	Updated EFP01 chip revision and changed part number on L200 and L201.
A02	Updated PCB revision (changes to panelization).
A03	Updated EFP01 to IC rev. D.

PCB1

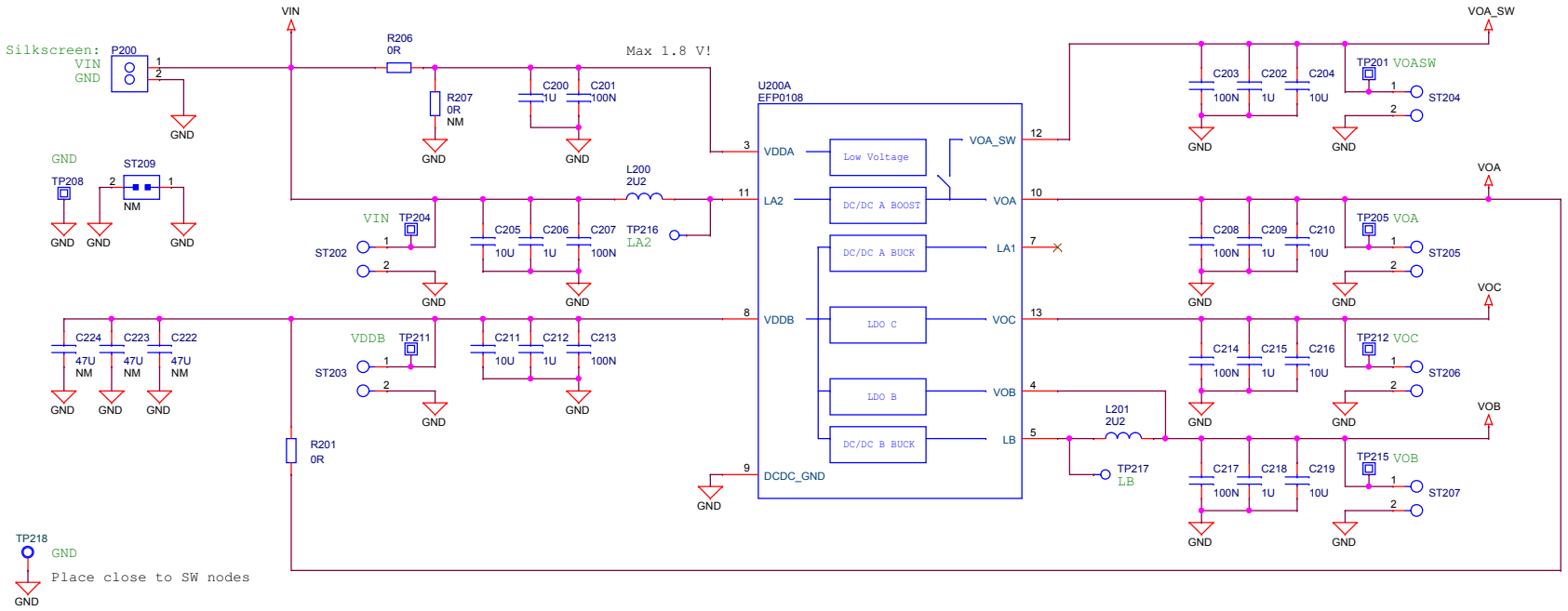
PCB8100A

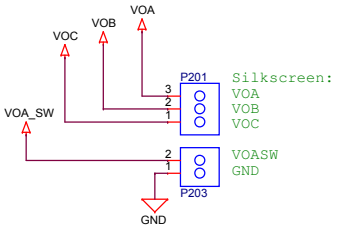
Designed: ESH	Approved: JSH	Schematic Title: EFP0108 Evaluation Board	
Size: A3	BOM Doc No:	Page Title: Title Page	
Design Created Date: Monday, February 04, 2019		Document number: BRD8100A	Revision: A03
		Sheet Created Date: Thursday, February 28, 2019	Sheet Modified Date: Thursday, January 09, 2020
			Sheet: 1 of 4

Power Input

EFP01

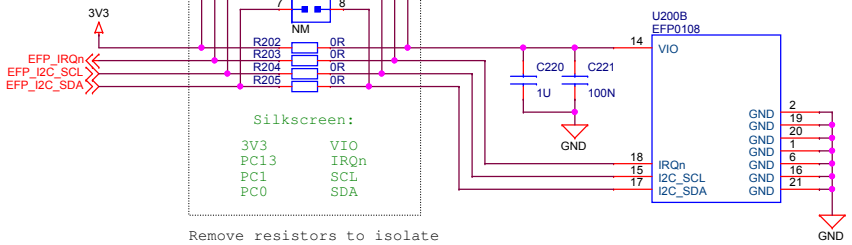
Power Output





EFP01 Digital Section

Host MCU Connection

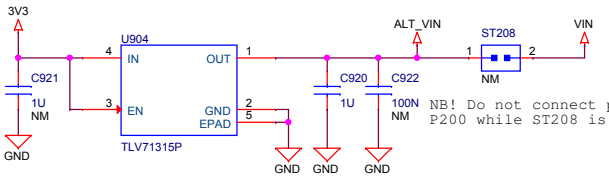


Remove resistors to isolate the EFP from the host MCU.

NB! Ground is not isolated

On-board LDO (from USB)

This rail is only intended for low power applications, and in the absence of a power source on P200.



BRD8100A: 1.5 V LDO
BRD8100B: 3.0 V LDO

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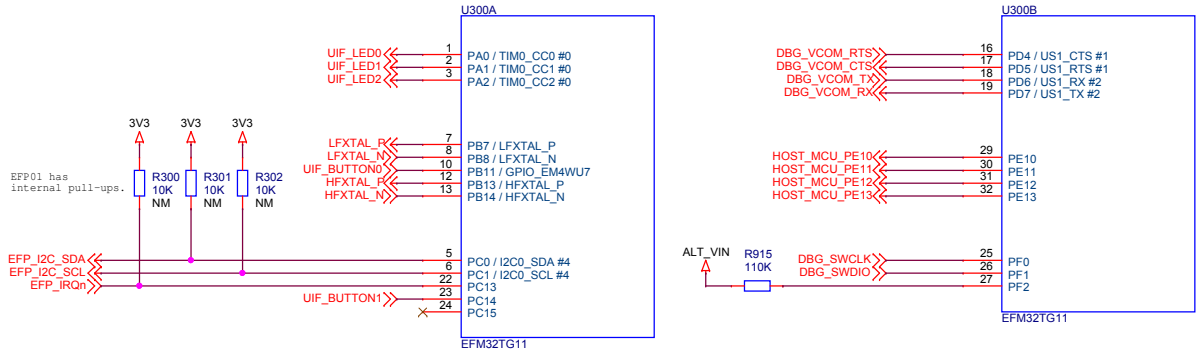
Schematic Title: **EFP0108 Evaluation Board**

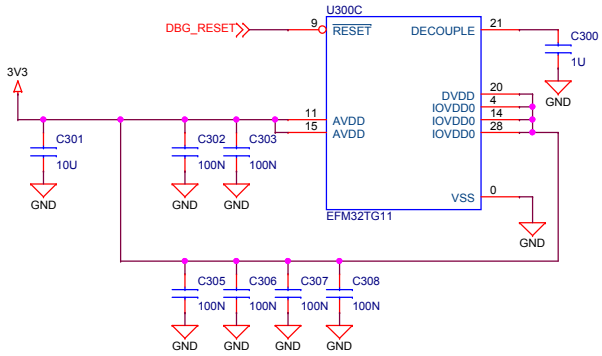
Page Title: **EFP01**

Document number: BRD8100A	Revision: A03
Sheet Created Date: Friday, March 01, 2019	Sheet Modified Date: Thursday, January 09, 2020
	Sheet 2 of 4

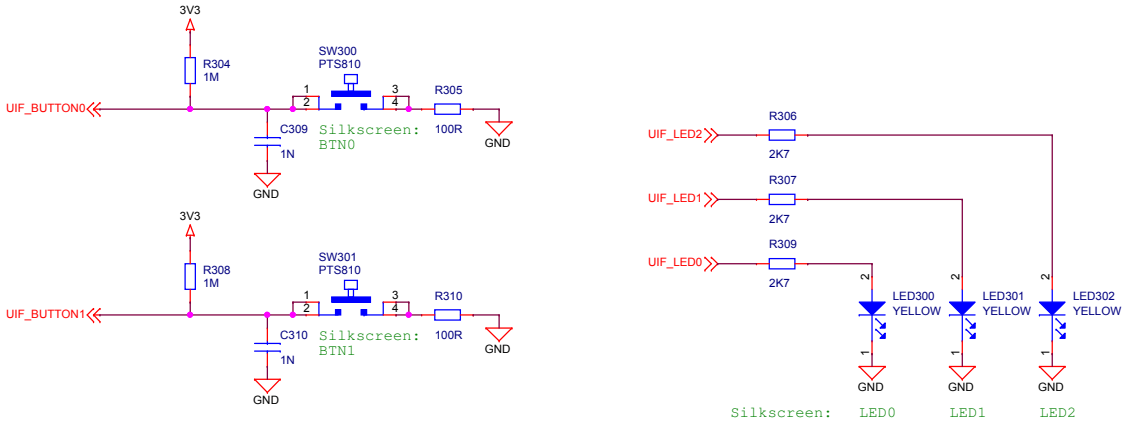
Host MCU I/O



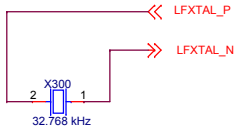
Host MCU Power



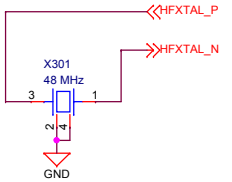
Buttons & LEDs



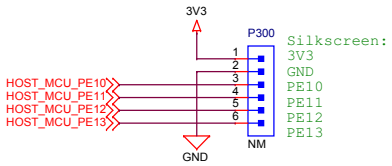
Low Frequency Clock



High Frequency Clock



Breakout Pads



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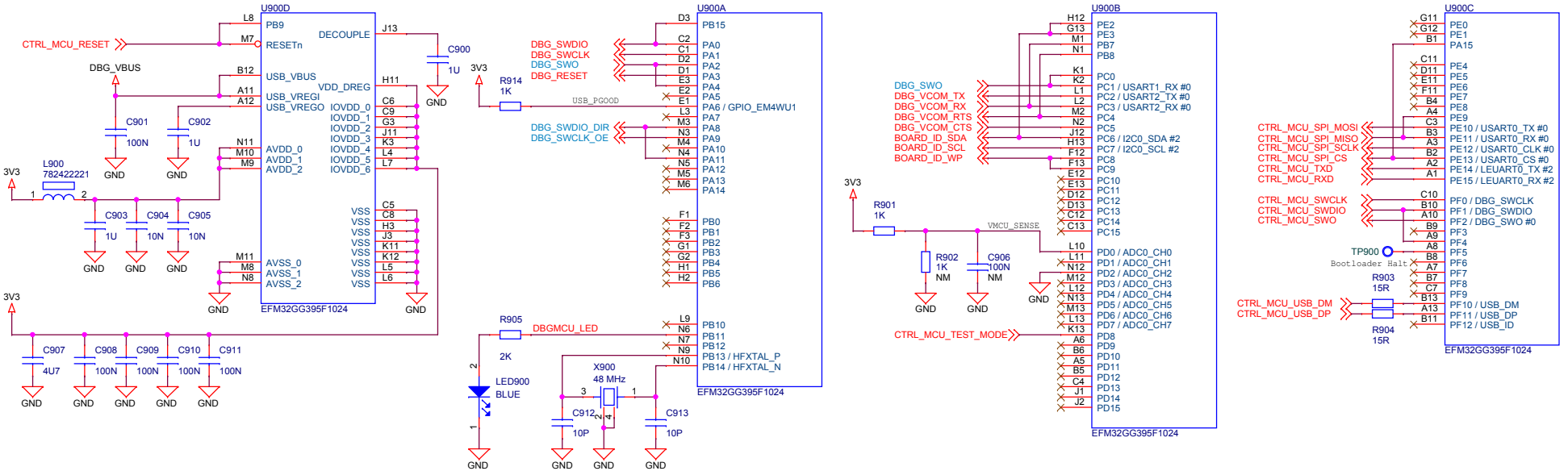
Schematic Title: **EFP0108 Evaluation Board**

Page Title: **Host MCU**

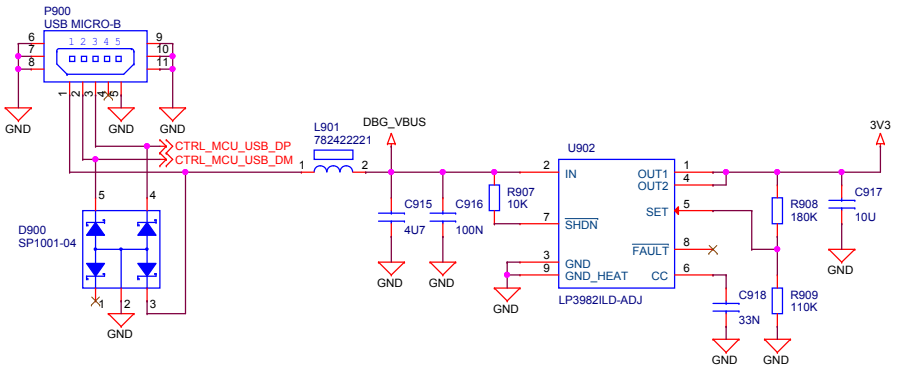
Document number: **BRD8100A**	Revision: A03
Sheet Created Date: Monday, February 04, 2019	Sheet Modified Date: Thursday, January 09, 2020
	Sheet: 3 of 4

On-board Debugger



Unused signals are marked in blue.

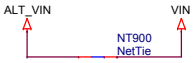
Debug USB Connection



3.3 V Regulator

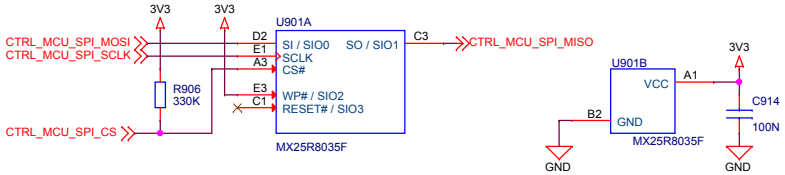
The Host MCU resides on the same power domain as the on-board debugger.

Misc.

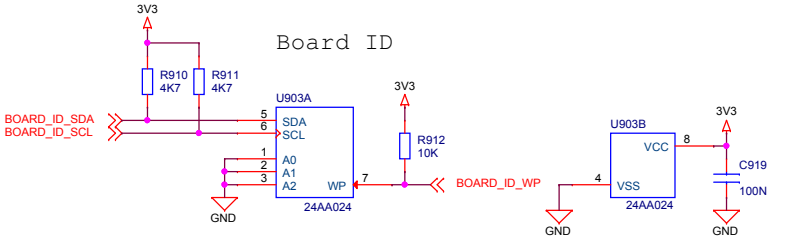


Place NT900 in panel.
The nets are not connected together after depanelization.

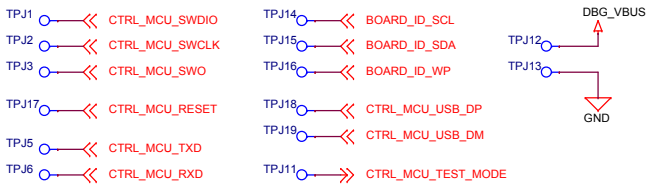
Serial Flash



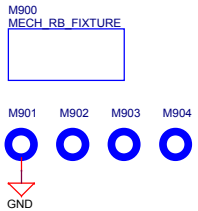
Board ID



Test Points



Mech



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Sheet	4 of 4