EFM32 Development Kit

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Revision History

Rev.	Description
PA18	Removed Control MCU testADC connection Added OE signal to BC_SPI buffer Clamped DIR signal on BC_SPI buffer
A00	Changed ST1 and ST2 to NM Initial Release
A01	Fixed EFM32_A80 connection
A02	Set D11 to Not Mounted Changed capacitors on trace lines to 8.2 pF

PCB1

PCB3201

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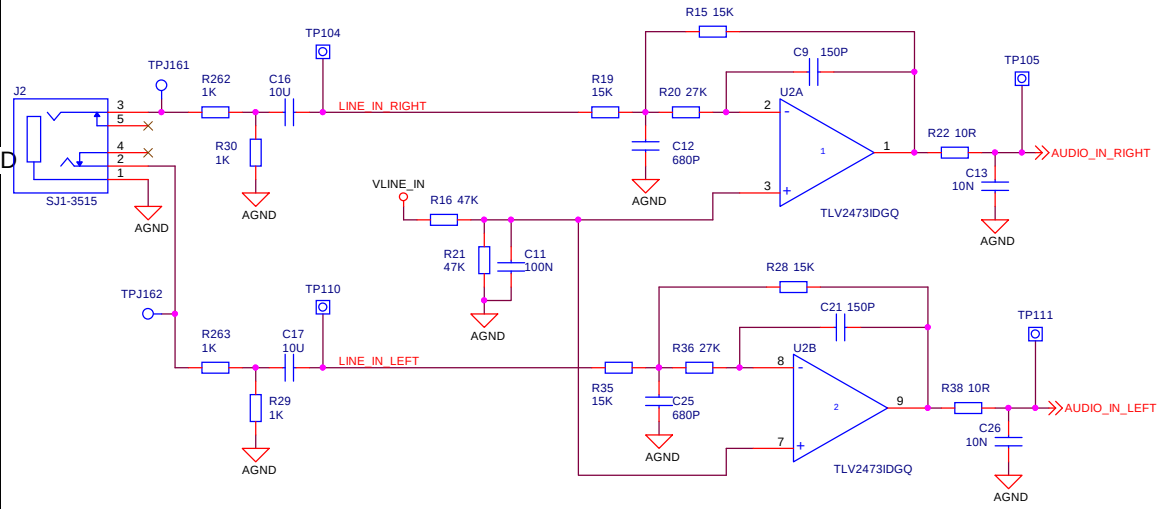
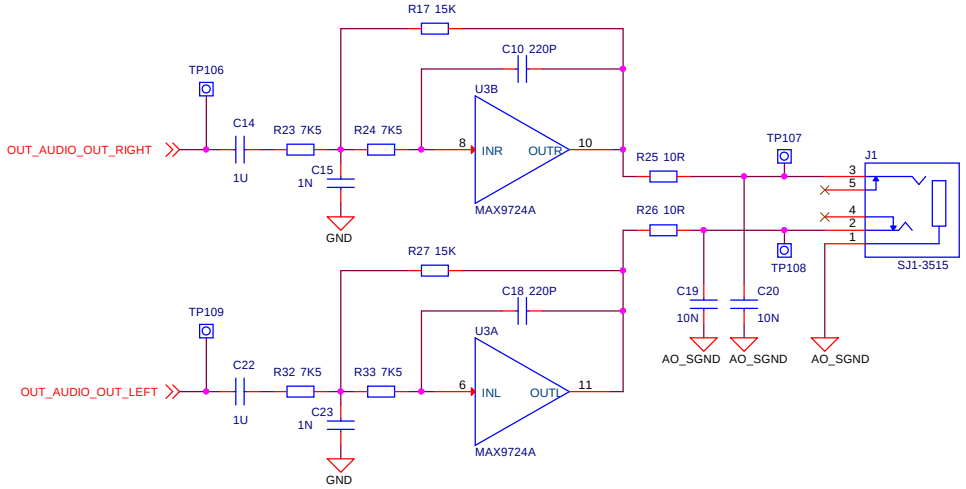
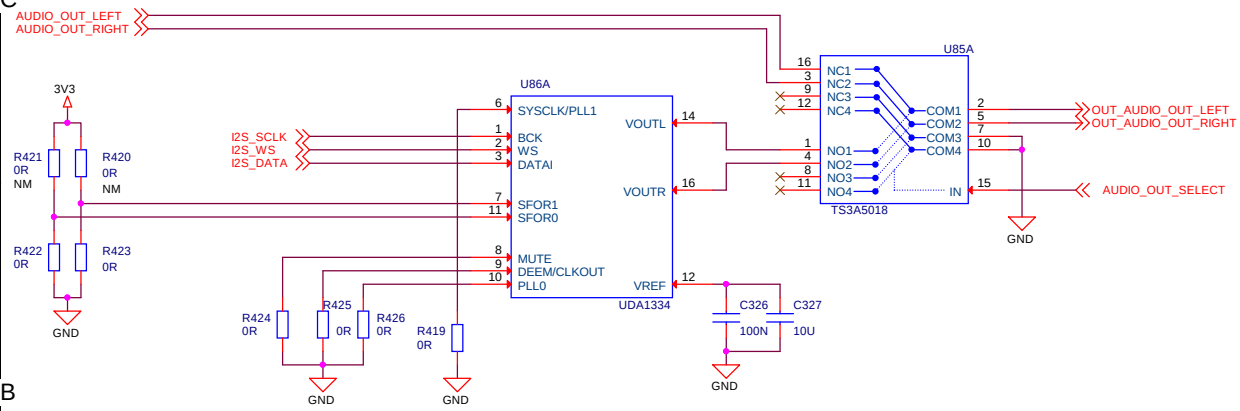
Line In Amplifier & Filter

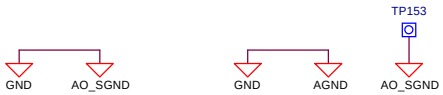


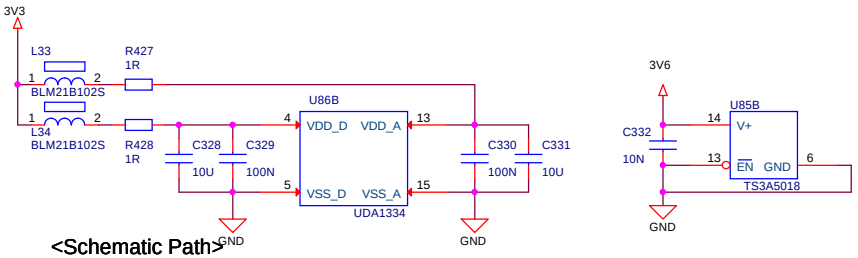
Line Out Driver & Filter



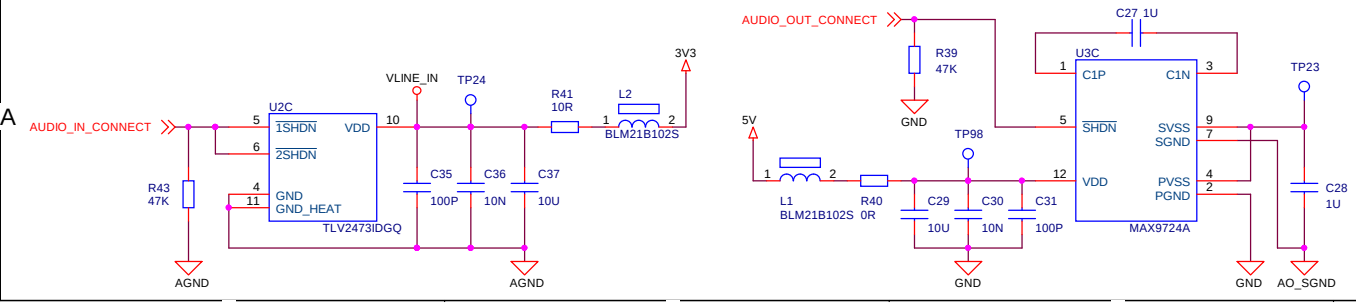
I2S DAC







Power Supply and Decoupling



<Schematic Path>
TOP

Schematic Title	**EFM32 Development Kit - Mainboard**
Page Title	**Interface - Analog**
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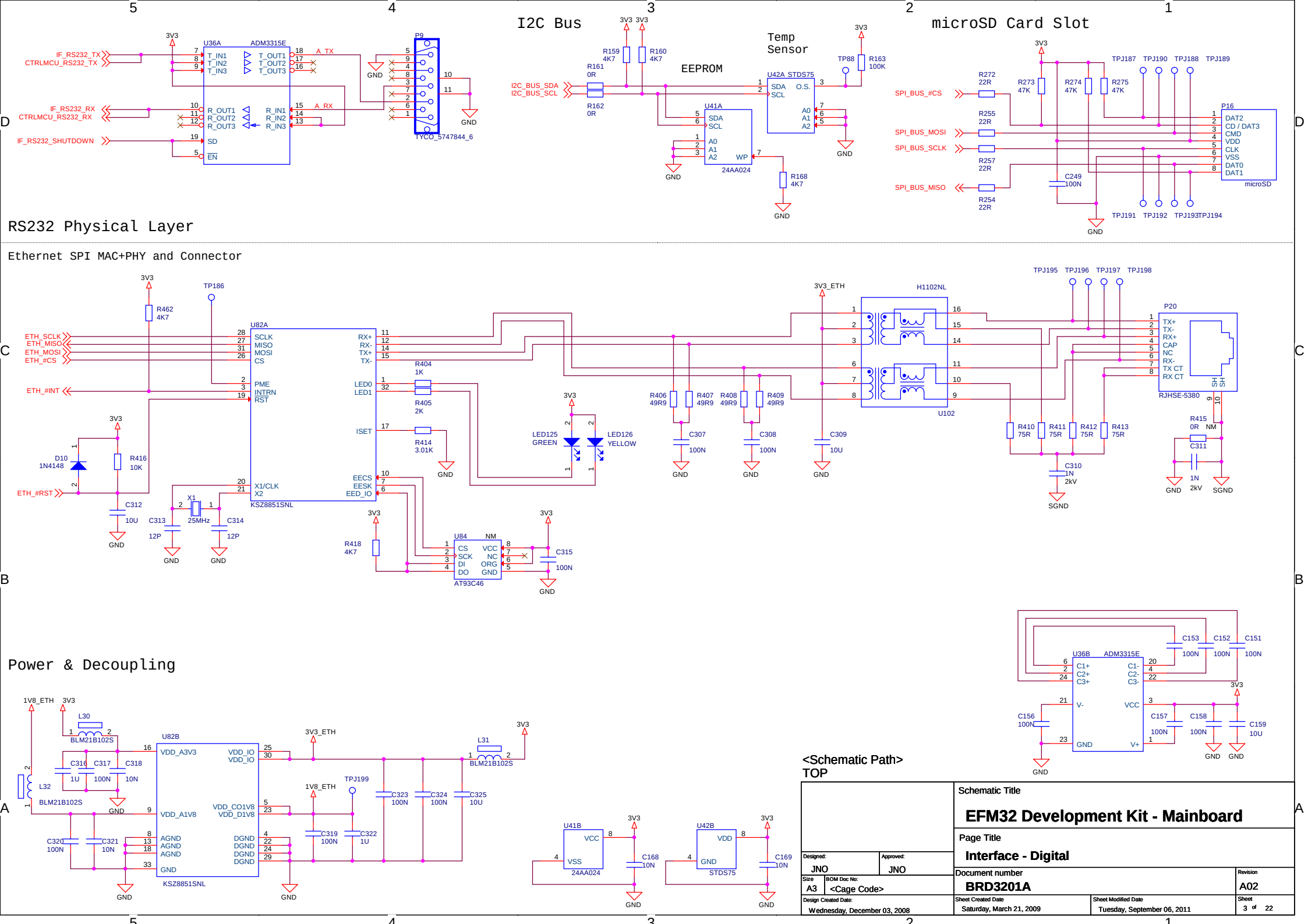
RS232 Physical Layer
U36A
ADM3315E
IF_RS232_TX
CTRLMCU_RS232_TX
IF_RS232_RX
CTRLMCU_RS232_RX
IF_RS232_SHUTDOWN
T_IN1
T_IN2
T_IN3
T_OUT1
T_OUT2
T_OUT3
R_OUT1
R_OUT2
R_OUT3
R_IN1
R_IN2
R_IN3
SD
EN
A_TX
A_RX
P9
TYCO_5747844_6
I2C Bus
I2C_BUS_SDA
I2C_BUS_SCL
R159 4K7
R160 4K7
R161 0R
R162 0R
EEPROM
U41A
24AA024
SDA
SCL
A0
A1
A2
WP
Temp Sensor
U42A STDS75
O.S.
TP88
R163 100K
R168 4K7
microSD Card Slot
SPI_BUS_#CS
SPI_BUS_MOSI
SPI_BUS_SCLK
SPI_BUS_MISO
R272 22R
R273 47K
R274 47K
R275 47K
R255 22R
R257 22R
R254 22R
C249 100N
TPJ187
TPJ190
TPJ188
TPJ189
TPJ191
TPJ192
TPJ193
TPJ194
P16
DAT2
CD / DAT3
CMD
VDD
CLK
VSS
DAT0
DAT1
microSD
Ethernet SPI MAC+PHY and Connector
U82A
KSZ8851SNL
ETH_SCLK
ETH_MISO
ETH_MOSI
ETH_#CS
ETH_#INT
ETH_#RST
SCLK
MISO
MOSI
CS
PME
INTRN
RST
RX+
RX-
TX+
TX-
LED0
LED1
ISET
EECS
EESK
EED_IO
X1/CLK
X2
R462 4K7
TP186
R404 1K
R405 2K
R414 3.01K
R416 10K
D10 1N4148
C312 10U
C313 12P
C314 12P
X1 25MHz
R418 4K7
U84 NM
AT93C46
CS
SCK
DI
DO
VCC
NC
ORG
GND
C315 100N
LED125 GREEN
LED126 YELLOW
R406 49R9
R407 49R9
R408 49R9
R409 49R9
C307 100N
C308 100N
C309 10U
3V3_ETH
H1102NL
U102
TPJ195
TPJ196
TPJ197
TPJ198
P20
RJHSE-5380
TX+
TX-
RX+
CAP
NC
RX-
TX CT
RX CT
SH
R410 75R
R411 75R
R412 75R
R413 75R
C310 1N 2kV
R415 0R NM
C311 1N 2kV
SGND
Power & Decoupling
1V8_ETH
3V3
L30 BLM21B102S
L32 BLM21B102S
C316 1U
C317 100N
C318 10N
C320 100N
C321 10N
U82B
VDD_A3V3
VDD_A1V8
VDD_IO
VDD_CO1V8
VDD_D1V8
AGND
DGND
GND
L31 BLM21B102S
TPJ199
C319 100N
C322 1U
C323 100N
C324 100N
C325 10U
U41B
24AA024
VCC
VSS
C168 10N
U42B
STDS75
VDD
GND
C169 10N
U36B
ADM3315E
C1+
C2+
C3+
C1-
C2-
C3-
V-
VCC
V+
C153 100N
C152 100N
C151 100N
C156 100N
C157 100N
C158 100N
C159 10U
<Schematic Path>
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Schematic Title
EFM32 Development Kit - Mainboard
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Interface - Digital
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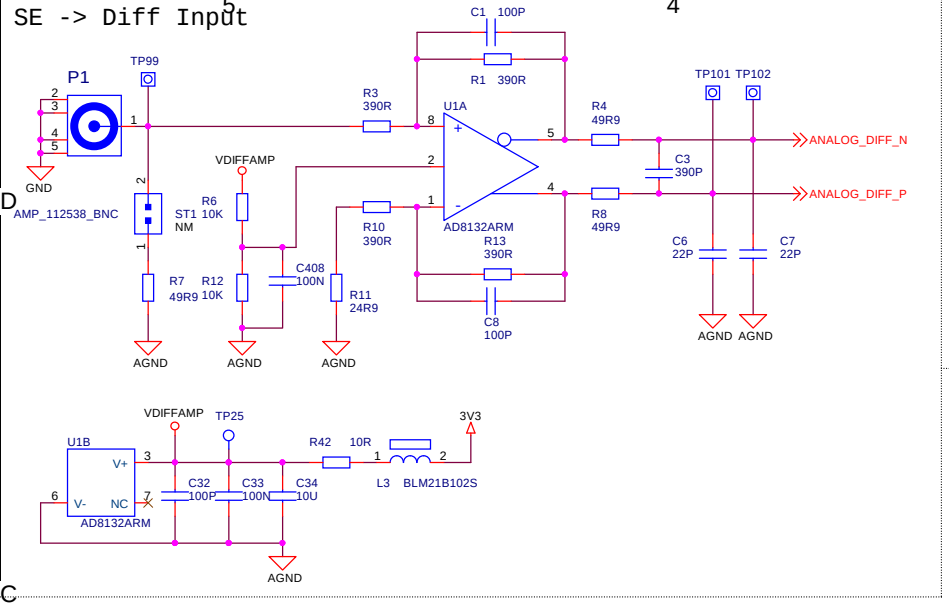
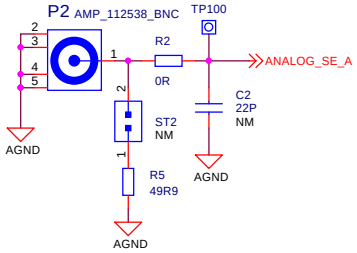
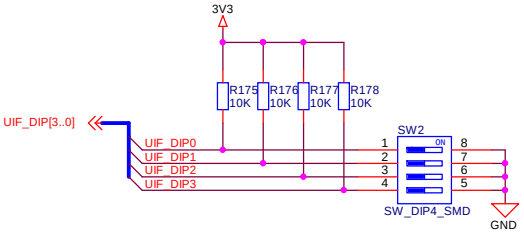
SE -> Diff Input



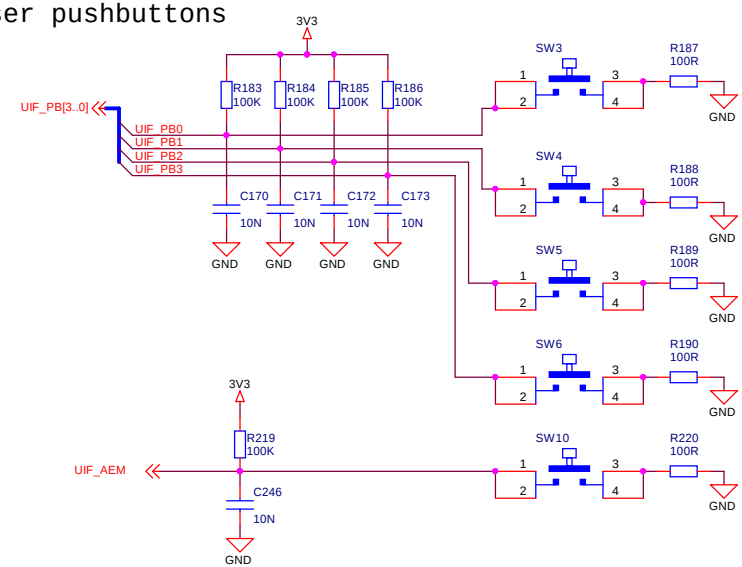
Single-Ended Input/Output



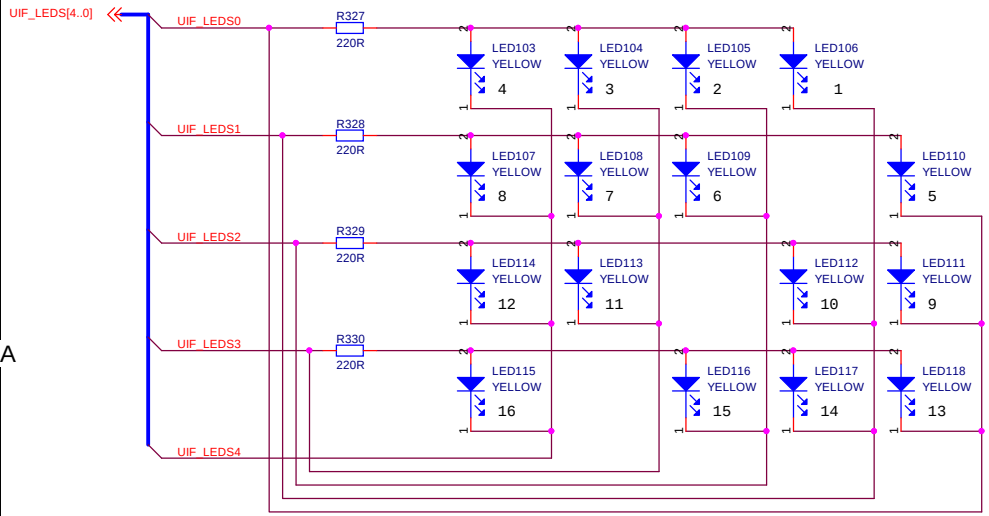
User switches



User pushbuttons

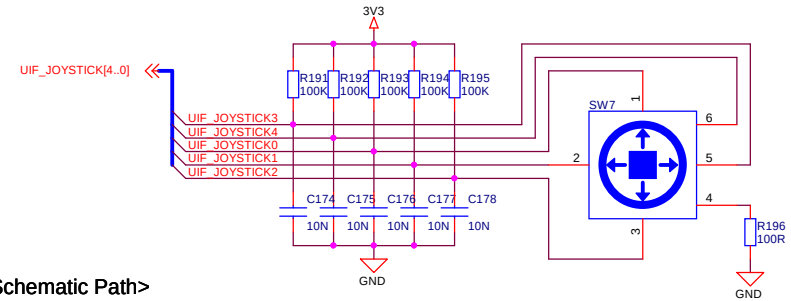


User LEDs



Inputs	LED
zzz01	1
zz0z1	2
z0zz1	3
0zzz1	4
zzz10	5
zz01z	6
z0z1z	7
0zz1z	8
zz1z0	9
zz10z	10
z01zz	11
0z1zz	12
z1zz0	13
z1z0z	14
z10zz	15
01zzz	16

Joystick



<Schematic Path>
TOP

Schematic Title	**EFM32 Development Kit - Mainboard**
Page Title	**Interface - Analog & UI**
Designed: JNO	Approved: JNO
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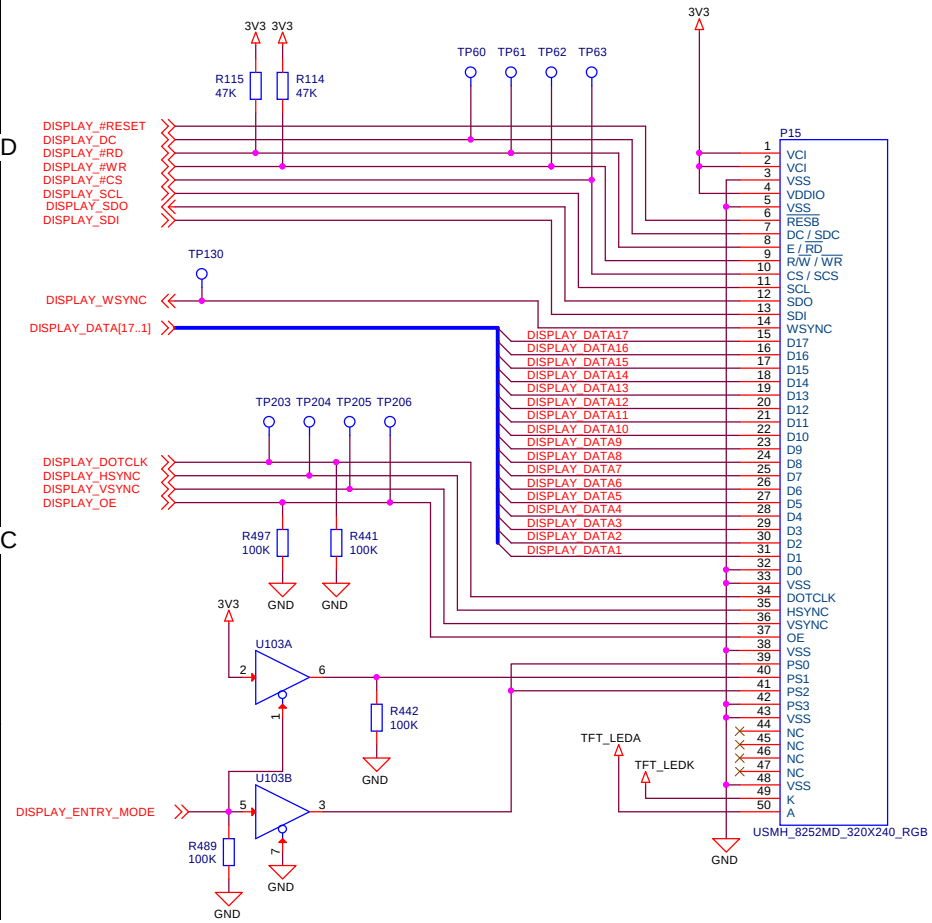
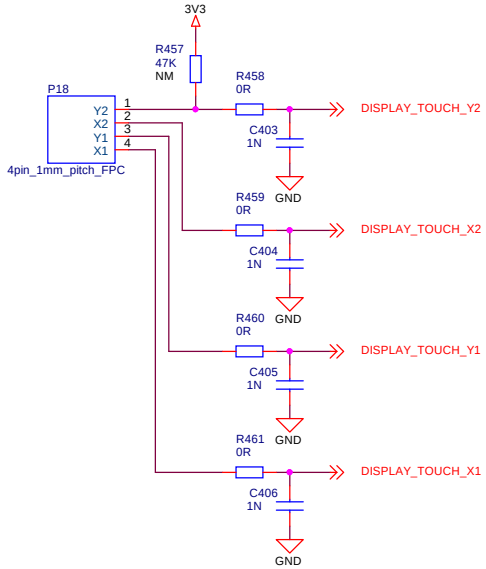
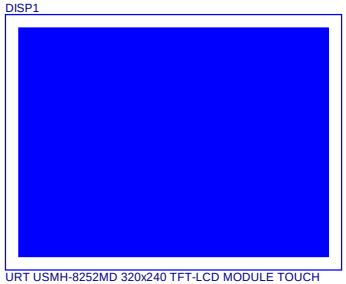
TFT-LCD Flat Panel Connector (FPC)

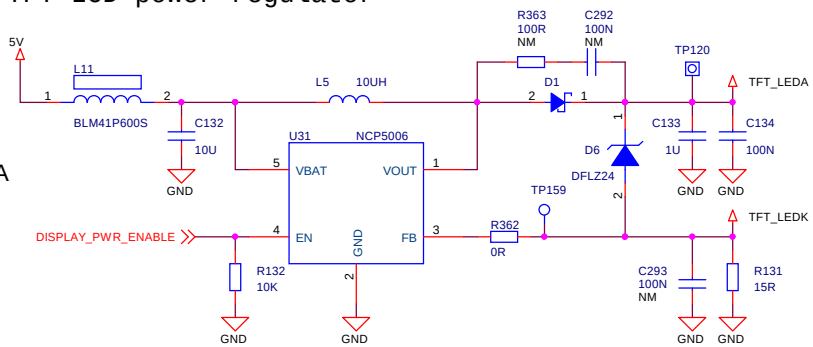


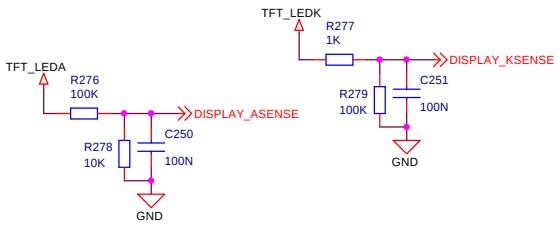


ENTRY_MODE	PS[3..0]	Description
0	0010	16 bit 8080 mode
1	0101	16 bit generic mode + SPI

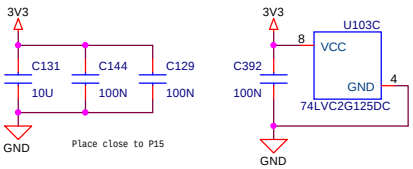


TFT-LCD power regulator

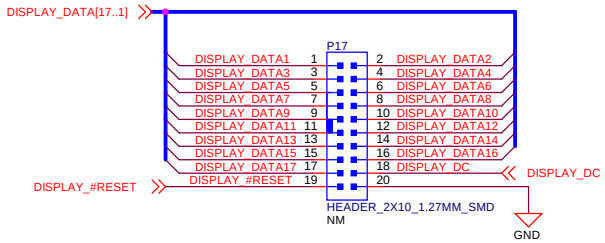




TFT-LCD decoupling



FPGA debug connector



<Schematic Path>
TOP

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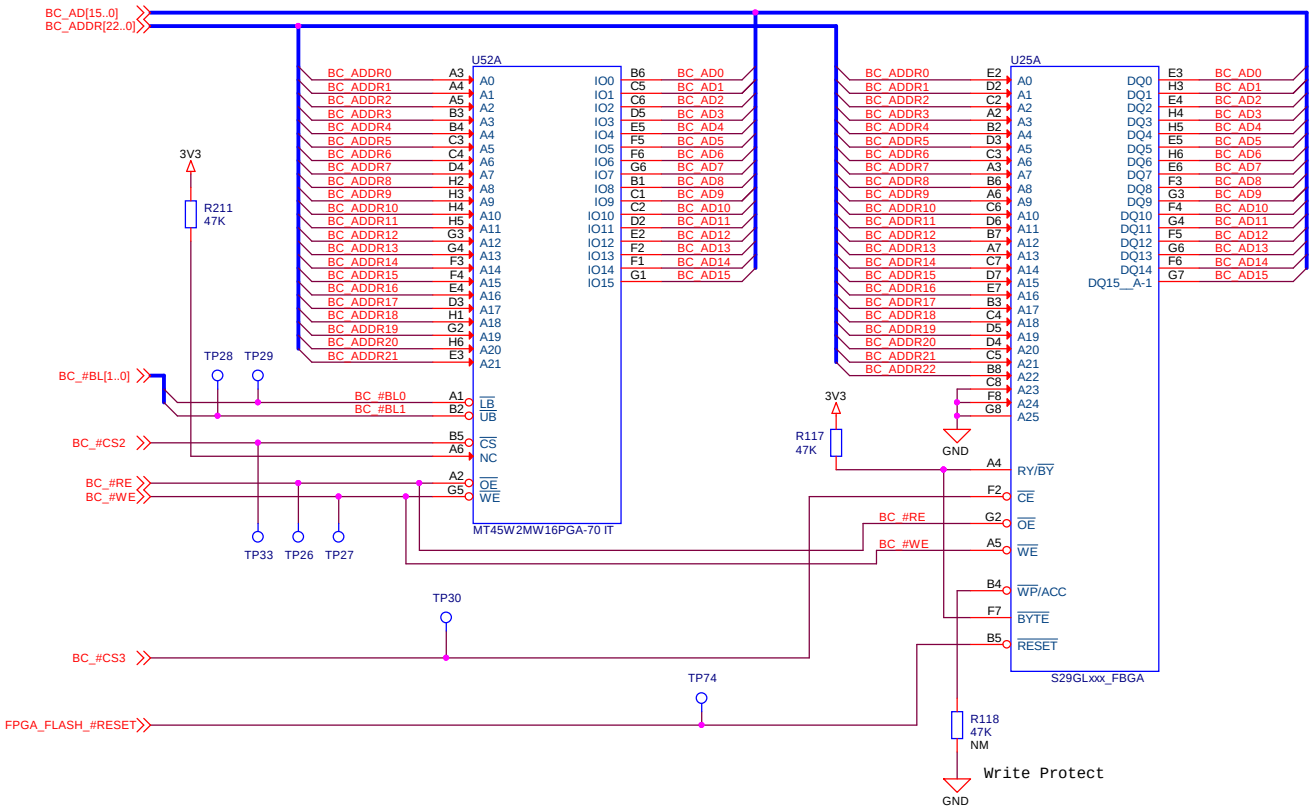
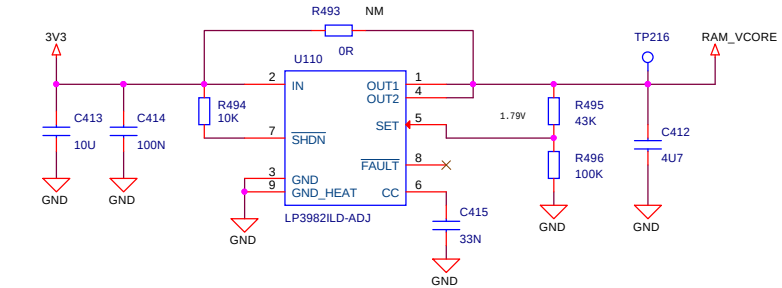
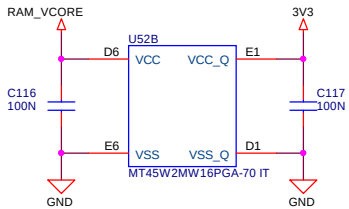
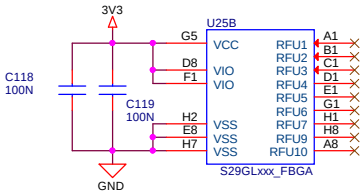


1.8V PSRAM regulator







<Schematic Path>
TOP

Schematic Title	**EFM32 Development Kit - Mainboard**
Page Title	**NOR Flash / SRAM**
Designed: JNO	Approved: JNO
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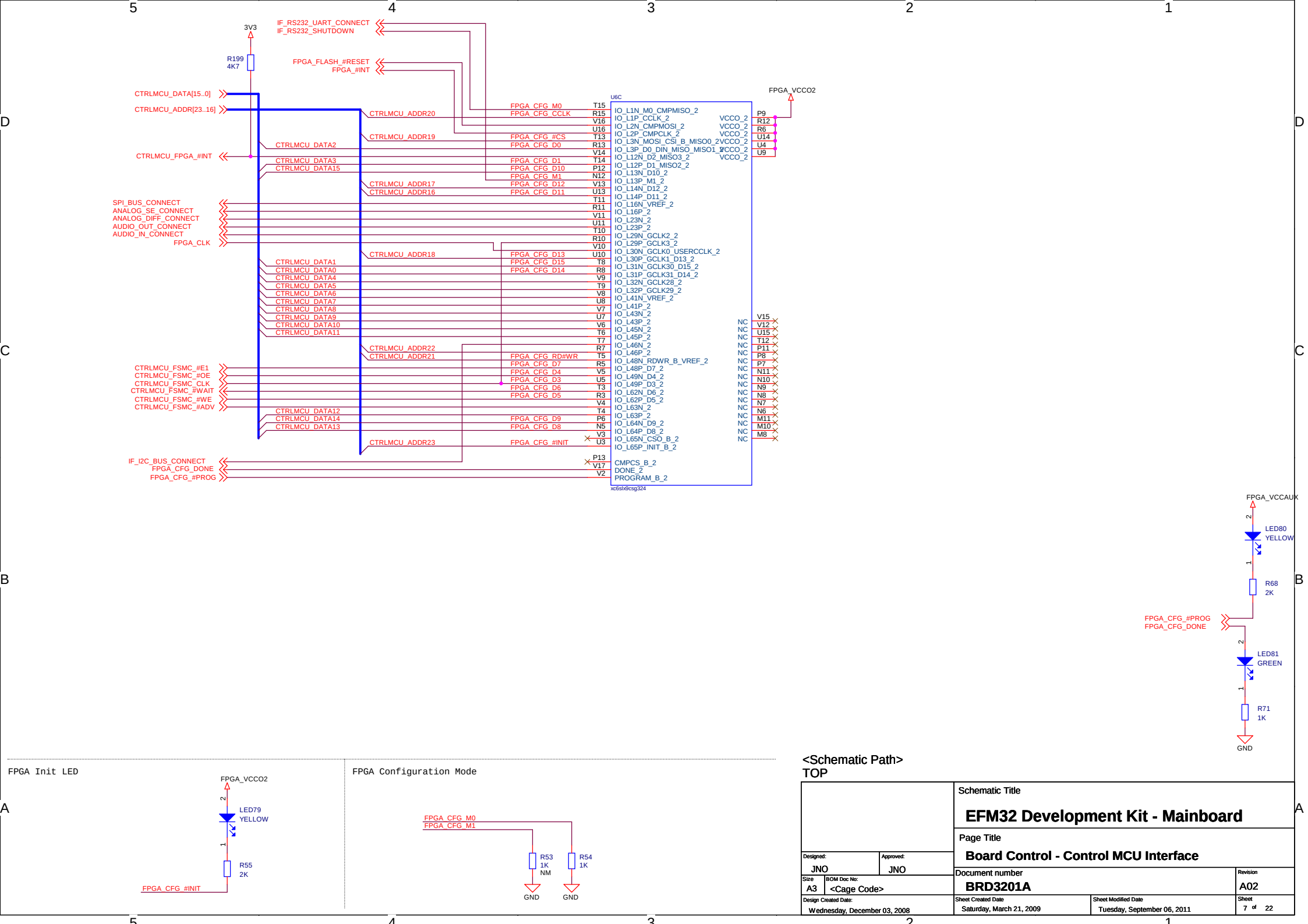

<Schematic Path>
TOP

Schematic Title	**EFM32 Development Kit - Mainboard**
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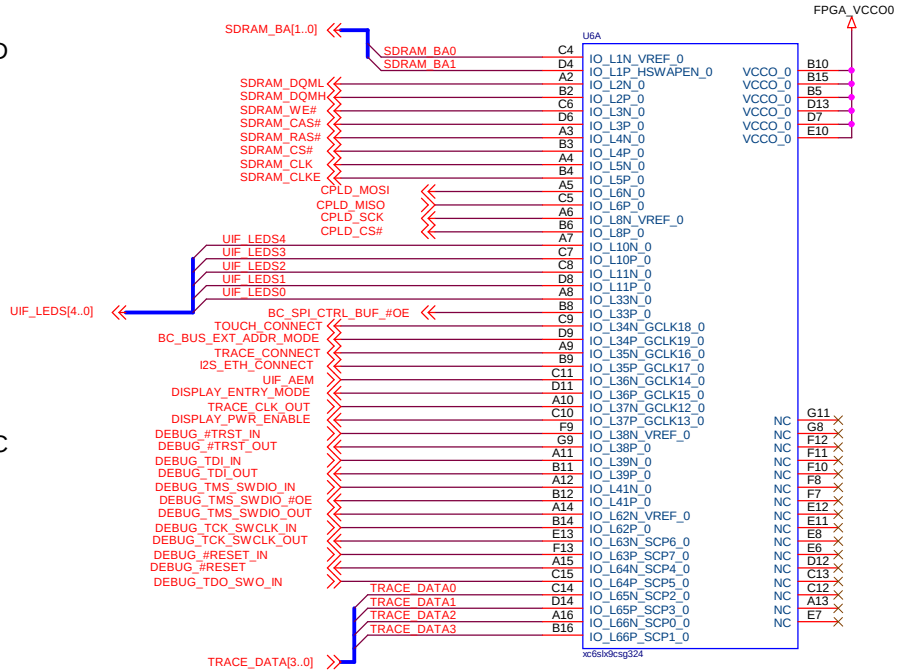

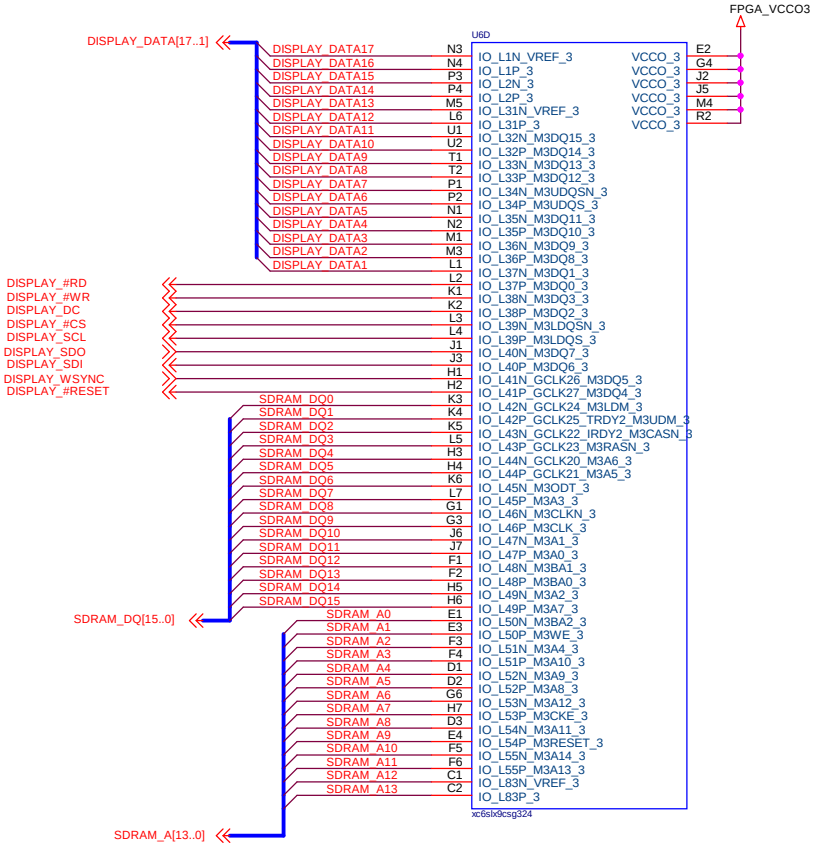

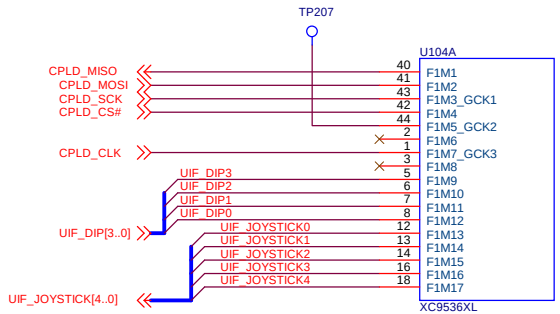

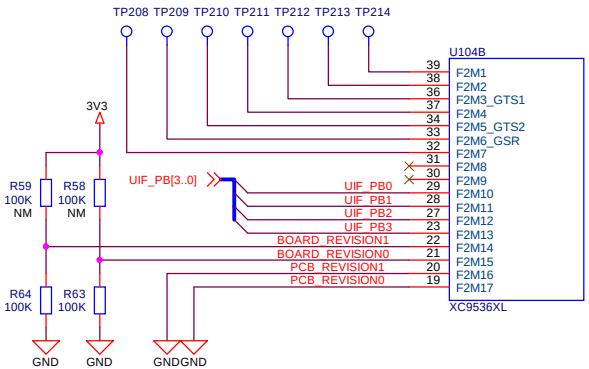

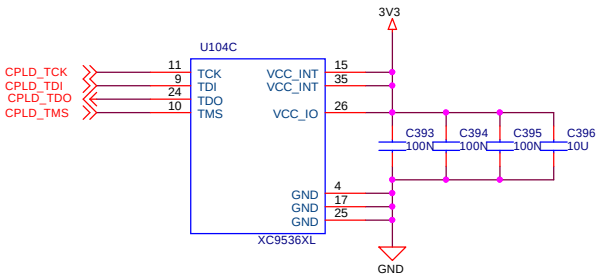

<Schematic Path>
TOP

Schematic Title	**EFM32 Development Kit - Mainboard**
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Designed: JNO	Approved: JNO
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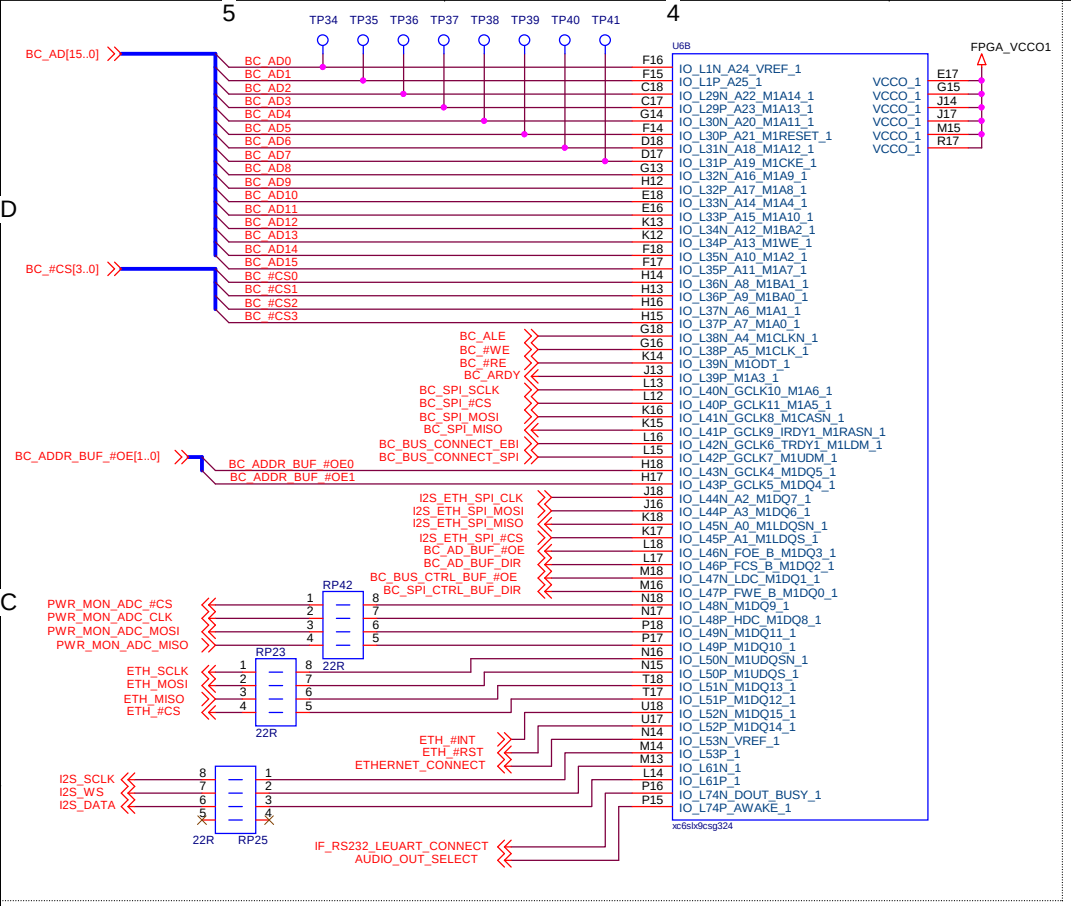

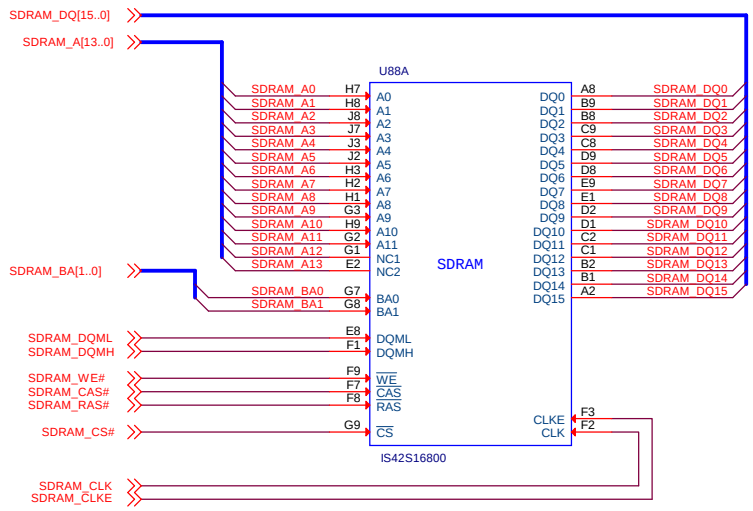

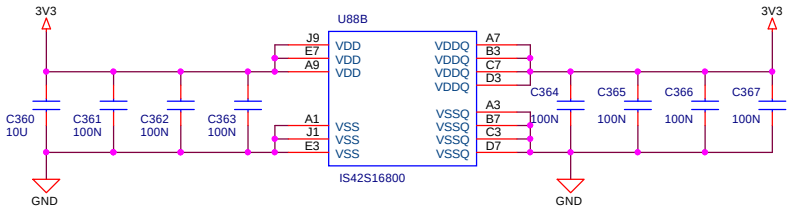

<Schematic Path>
TOP

Schematic Title	**EFM32 Development Kit - Mainboard**
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Designed: JNO	Approved: JNO
Size: A3	BOM Doc No: <Cage Code>
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Design Created Date	Wednesday, December 03, 2008
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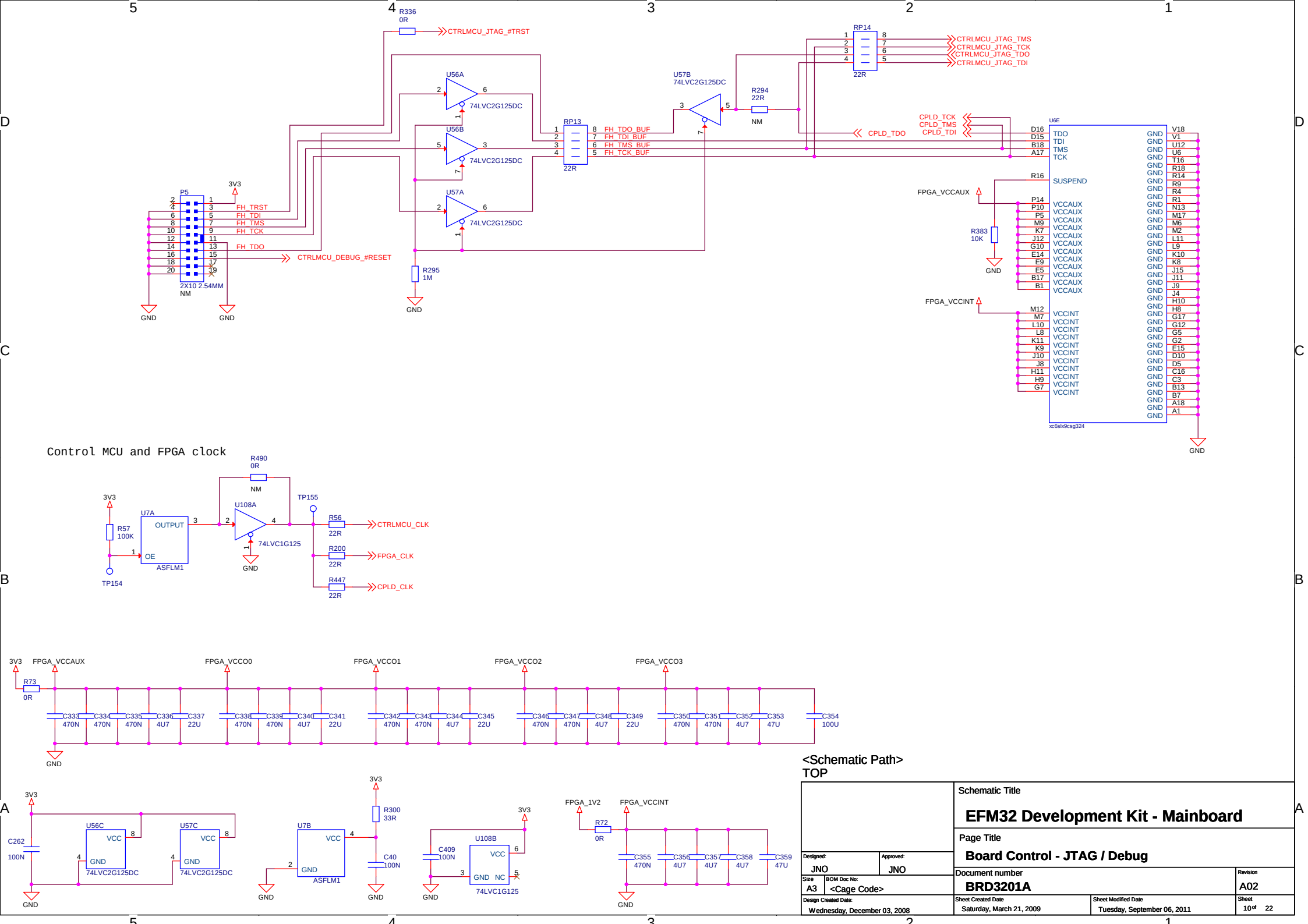

<Schematic Path>
TOP

Schematic Title	**EFM32 Development Kit - Mainboard**
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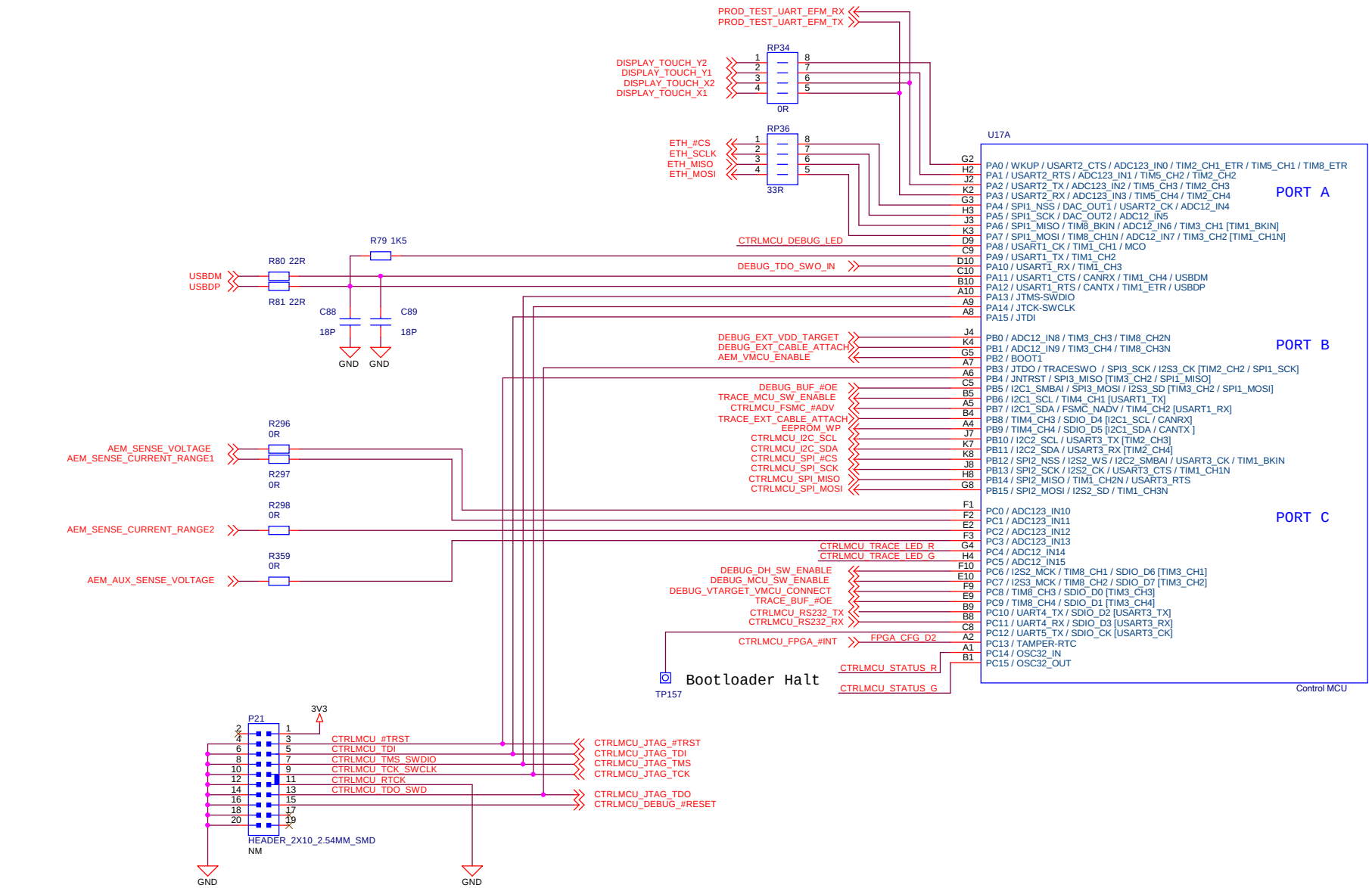

<Schematic Path>
TOP

Schematic Title	**EFM32 Development Kit**
Page Title	**Control MCU**
Designed: JNO	Approved: JNO
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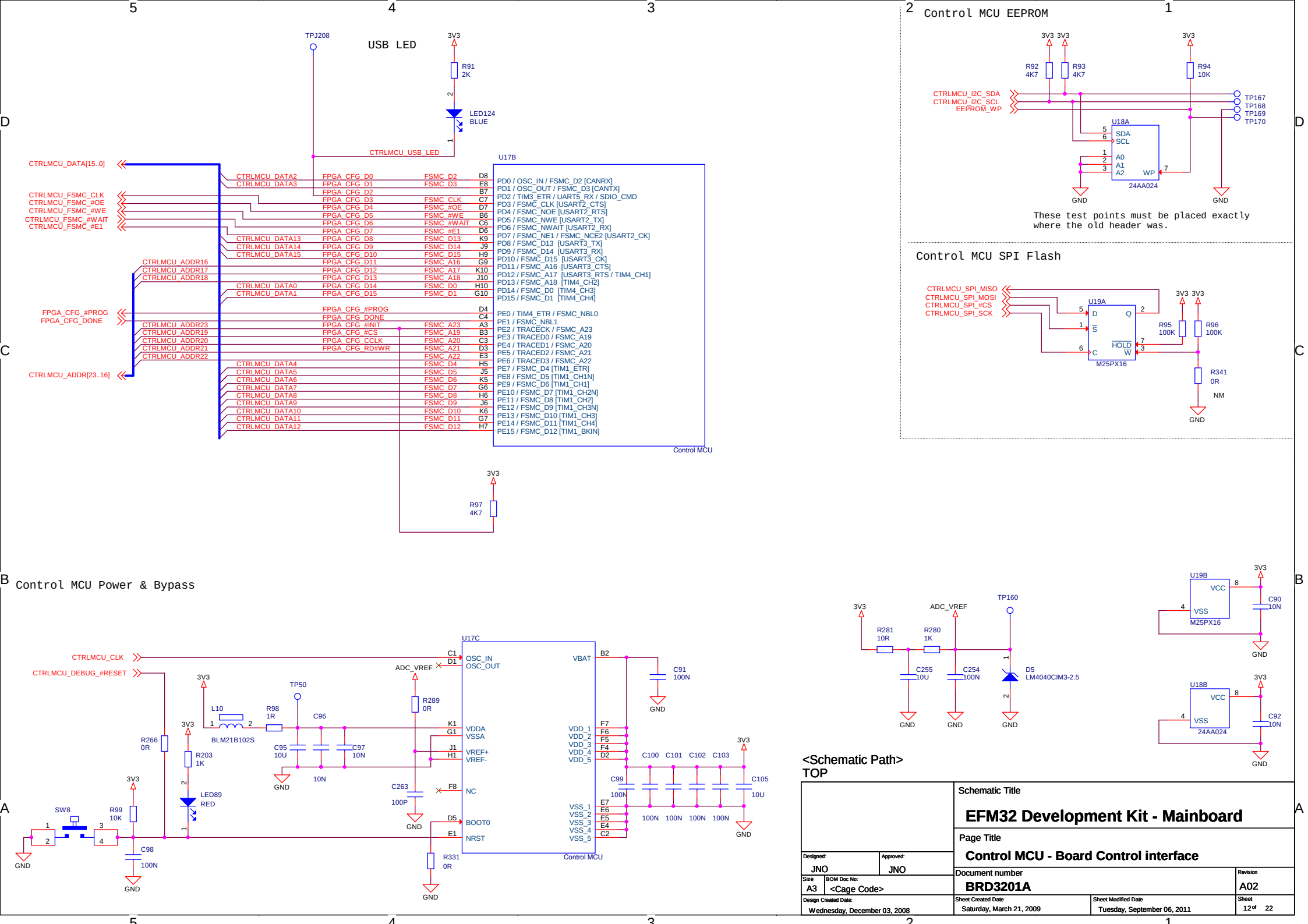
USB LED
TPJ208
3V3
R91
2K
LED124
BLUE
CTRLMCU_USB_LED
U17B
CTRLMCU_DATA[15..0]
CTRLMCU_FSMC_CLK
CTRLMCU_FSMC_#OE
CTRLMCU_FSMC_#WE
CTRLMCU_FSMC_#WAIT
CTRLMCU_FSMC_#E1
CTRLMCU_ADDR16
CTRLMCU_ADDR17
CTRLMCU_ADDR18
FPGA_CFG_#PROG
FPGA_CFG_DONE
CTRLMCU_ADDR23
CTRLMCU_ADDR19
CTRLMCU_ADDR20
CTRLMCU_ADDR21
CTRLMCU_ADDR22
CTRLMCU_ADDR[23..16]
CTRLMCU_DATA2 FPGA_CFG_D0 FSMC_D2 D8
CTRLMCU_DATA3 FPGA_CFG_D1 FSMC_D3 E8
FPGA_CFG_D2 B7
FPGA_CFG_D3 FSMC_CLK C7
FPGA_CFG_D4 FSMC_#OE D7
FPGA_CFG_D5 FSMC_#WE B6
FPGA_CFG_D6 FSMC_#WAIT C6
FPGA_CFG_D7 FSMC_#E1 D6
CTRLMCU_DATA13 FPGA_CFG_D8 FSMC_D13 K9
CTRLMCU_DATA14 FPGA_CFG_D9 FSMC_D14 J9
CTRLMCU_DATA15 FPGA_CFG_D10 FSMC_D15 H9
FPGA_CFG_D11 FSMC_A16 G9
FPGA_CFG_D12 FSMC_A17 K10
FPGA_CFG_D13 FSMC_A18 J10
CTRLMCU_DATA0 FPGA_CFG_D14 FSMC_D0 H10
CTRLMCU_DATA1 FPGA_CFG_D15 FSMC_D1 G10
FPGA_CFG_#PROG D4
FPGA_CFG_DONE C4
FPGA_CFG_#INIT FSMC_A23 A3
FPGA_CFG_#CS FSMC_A19 B3
FPGA_CFG_CCLK FSMC_A20 C3
FPGA_CFG_RD#WR FSMC_A21 D3
FSMC_A22 E3
CTRLMCU_DATA4 FSMC_D4 H5
CTRLMCU_DATA5 FSMC_D5 J5
CTRLMCU_DATA6 FSMC_D6 K5
CTRLMCU_DATA7 FSMC_D7 G6
CTRLMCU_DATA8 FSMC_D8 H6
CTRLMCU_DATA9 FSMC_D9 J6
CTRLMCU_DATA10 FSMC_D10 K6
CTRLMCU_DATA11 FSMC_D11 G7
CTRLMCU_DATA12 FSMC_D12 H7
PD0 / OSC_IN / FSMC_D2 [CANRX]
PD1 / OSC_OUT / FSMC_D3 [CANTX]
PD2 / TIM3_ETR / UART5_RX / SDIO_CMD
PD3 / FSMC_CLK [USART2_CTS]
PD4 / FSMC_NOE [USART2_RTS]
PD5 / FSMC_NWE [USART2_TX]
PD6 / FSMC_NWAIT [USART2_RX]
PD7 / FSMC_NE1 / FSMC_NCE2 [USART2_CK]
PD8 / FSMC_D13 [USART3_TX]
PD9 / FSMC_D14 [USART3_RX]
PD10 / FSMC_D15 [USART3_CK]
PD11 / FSMC_A16 [USART3_CTS]
PD12 / FSMC_A17 [USART3_RTS / TIM4_CH1]
PD13 / FSMC_A18 [TIM4_CH2]
PD14 / FSMC_D0 [TIM4_CH3]
PD15 / FSMC_D1 [TIM4_CH4]
PE0 / TIM4_ETR / FSMC_NBL0
PE1 / FSMC_NBL1
PE2 / TRACECK / FSMC_A23
PE3 / TRACED0 / FSMC_A19
PE4 / TRACED1 / FSMC_A20
PE5 / TRACED2 / FSMC_A21
PE6 / TRACED3 / FSMC_A22
PE7 / FSMC_D4 [TIM1_ETR]
PE8 / FSMC_D5 [TIM1_CH1N]
PE9 / FSMC_D6 [TIM1_CH1]
PE10 / FSMC_D7 [TIM1_CH2N]
PE11 / FSMC_D8 [TIM1_CH2]
PE12 / FSMC_D9 [TIM1_CH3N]
PE13 / FSMC_D10 [TIM1_CH3]
PE14 / FSMC_D11 [TIM1_CH4]
PE15 / FSMC_D12 [TIM1_BKIN]
Control MCU
R97
4K7
Control MCU EEPROM
R92
4K7
R93
4K7
R94
10K
CTRLMCU_I2C_SDA
CTRLMCU_I2C_SCL
EEPROM_WP
TP167
TP168
TP169
TP170
U18A
SDA
SCL
A0
A1
A2
WP
24AA024
GND
These test points must be placed exactly where the old header was.
Control MCU SPI Flash
CTRLMCU_SPI_MISO
CTRLMCU_SPI_MOSI
CTRLMCU_SPI_#CS
CTRLMCU_SPI_SCK
U19A
D
Q
S
HOLD
W
C
M25PX16
R95
100K
R96
100K
R341
0R
NM
Control MCU Power & Bypass
CTRLMCU_CLK
CTRLMCU_DEBUG_#RESET
U17C
OSC_IN
OSC_OUT
ADC_VREF
VDDA
VSSA
VREF+
VREF-
NC
BOOT0
NRST
VBAT
VDD_1
VDD_2
VDD_3
VDD_4
VDD_5
VSS_1
VSS_2
VSS_3
VSS_4
VSS_5
Control MCU
TP50
L10
BLM21B102S
R98
1R
C96
10N
C95
10U
C97
10N
R289
0R
C263
100P
R331
0R
R266
0R
R203
1K
LED89
RED
SW8
R99
10K
C98
100N
C91
100N
C100
C101
C102
C103
C99
100N
C105
10U
TP160
R281
10R
R280
1K
C255
10U
C254
100N
D5
LM4040CIM3-2.5
U19B
VCC
VSS
M25PX16
C90
10N
U18B
24AA024
C92
10N
<Schematic Path>
TOP
Schematic Title
EFM32 Development Kit - Mainboard
Page Title
Control MCU - Board Control interface
Designed: JNO
Approved: JNO
Size A3
BOM Doc No: <Cage Code>
Document number BRD3201A
Revision A02
Design Created Date: Wednesday, December 03, 2008
Sheet Created Date: Saturday, March 21, 2009
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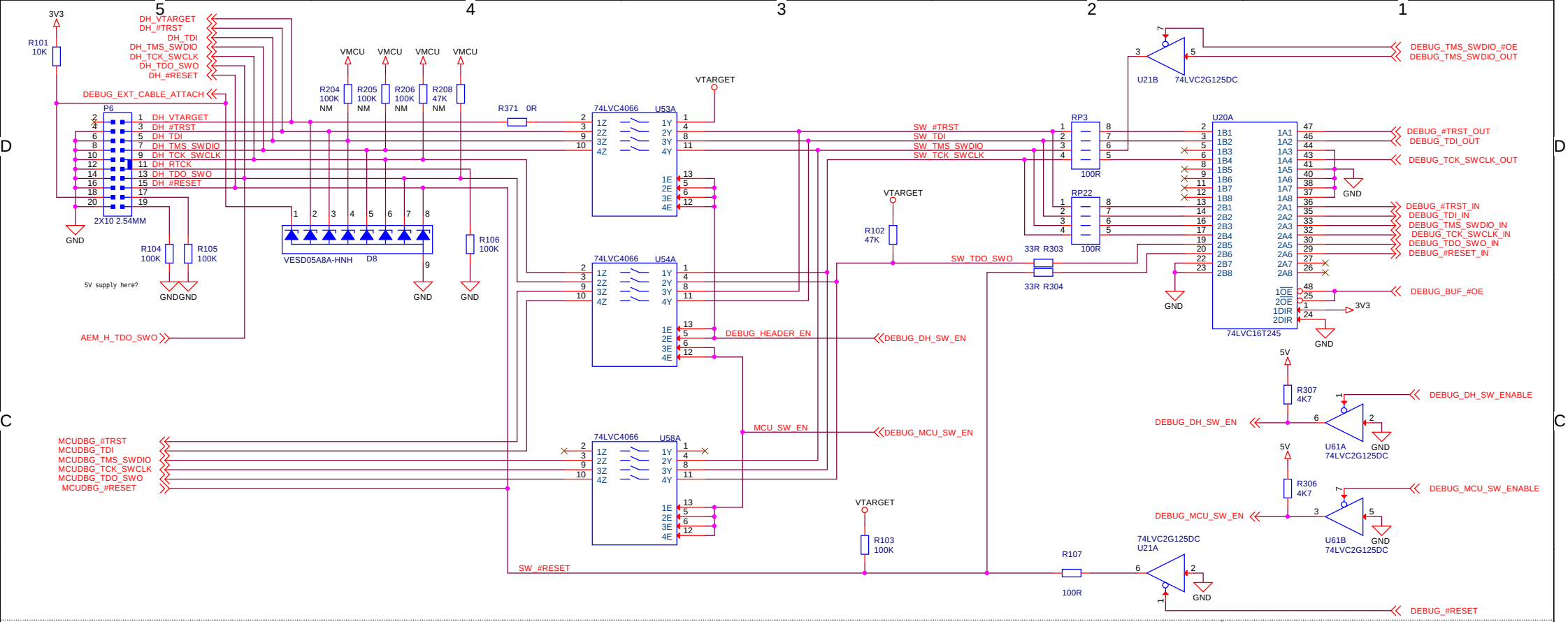
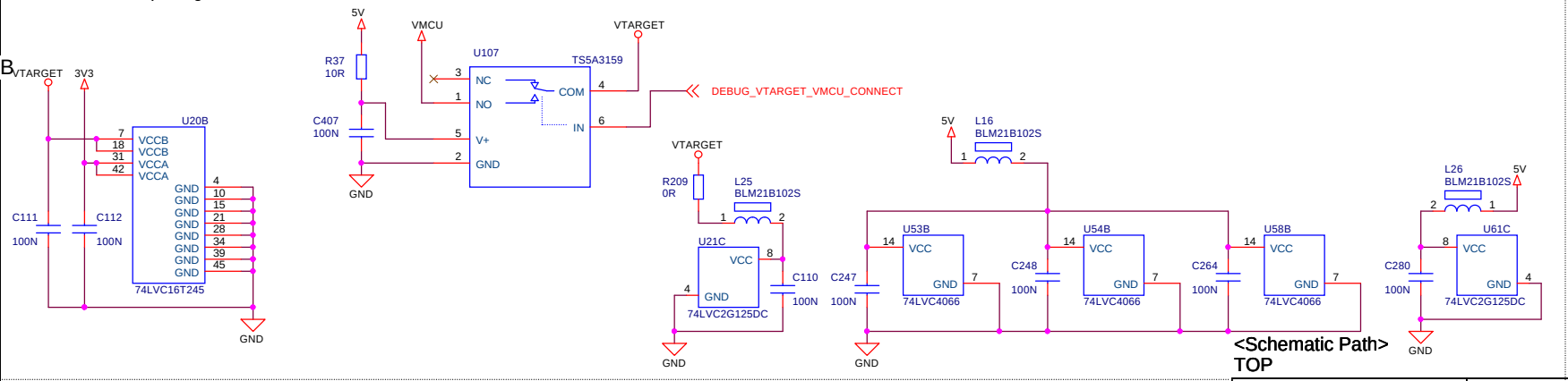
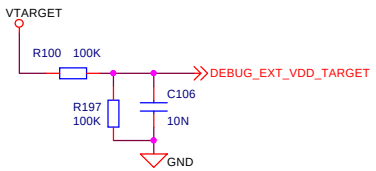


Power & Decoupling



Ext. Debug Voltage Measurement



Mode	DEBUG_MCU_SW_ENABLE	DEBUG_DH_SW_ENABLE	DEBUG_BUF_#OE	DH_VTARGET	VTARGET
Debug Out	0	1	0	External voltage	External voltage
MCU Debug	1	0	0	Disconnected	VMCU
Debug In	1	1	1	VMCU	VMCU

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Page Title	Debug Interface
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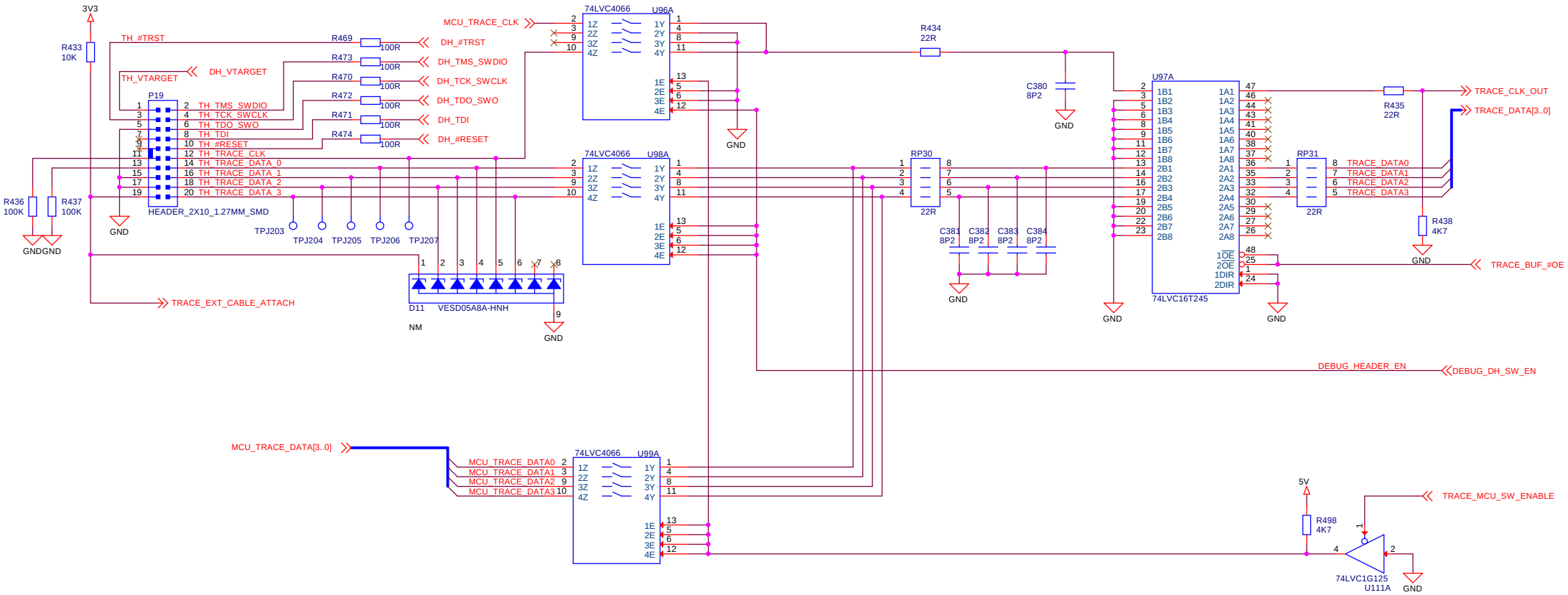
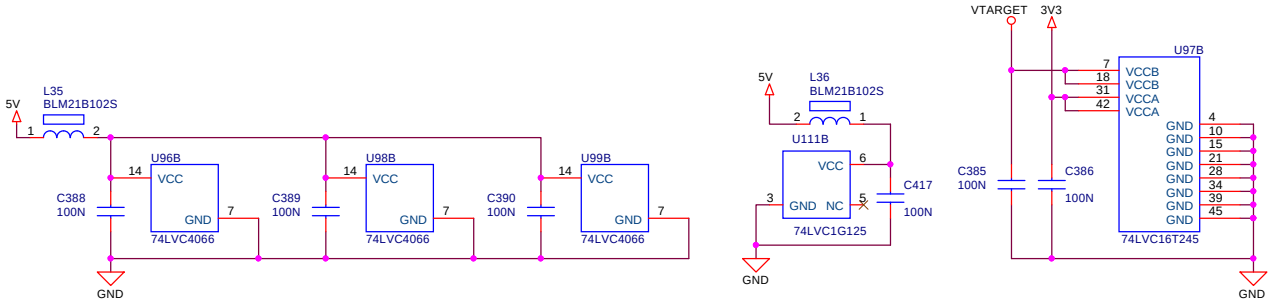


Mode	DEBUG_MCU_SW_ENABLE	DEBUG_TH_SW_ENABLE	TRACE_BUF_#OE
Trace OUT	0	1	0
MCU Trace	1	0	0
Trace IN	1	1	1



<Schematic Path>
TOP

Schematic Title	**EFM32 Development Kit - Mainboard**
Page Title	**Trace Interface**
Designed: AG	Approved: JNO
Size: A3	BOM Doc No: <Cage Code>
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Design Created Date:	Wednesday, December 03, 2008
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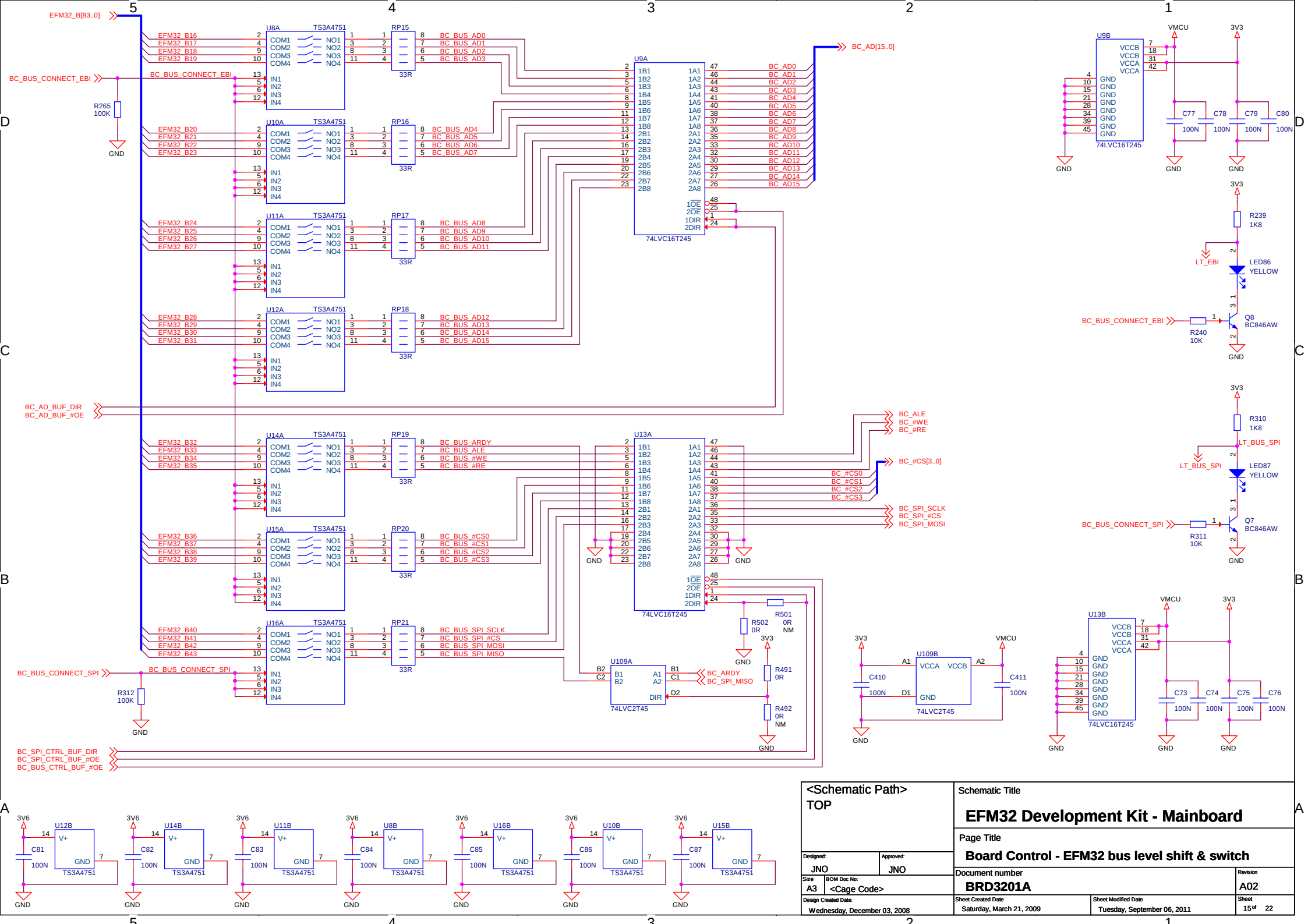
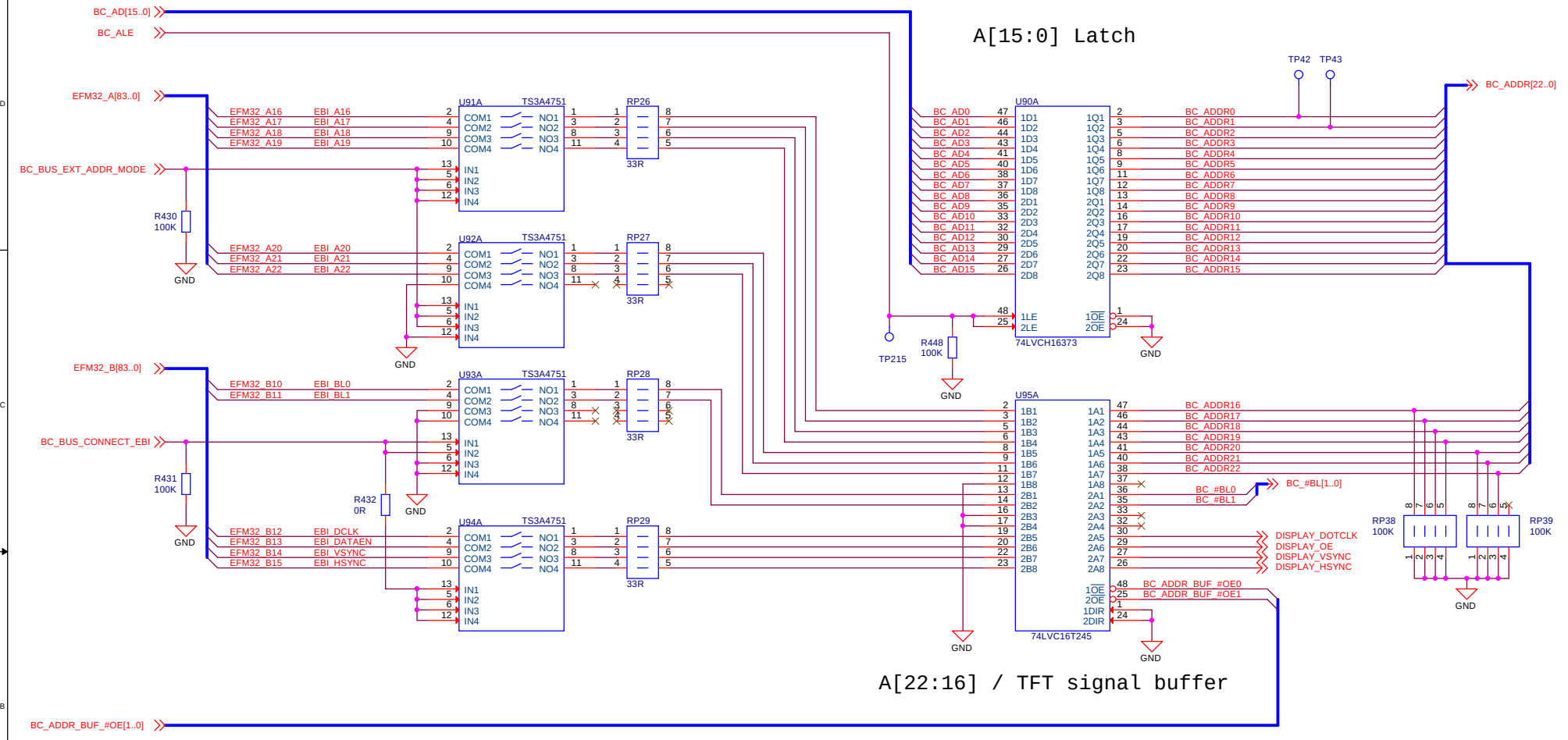
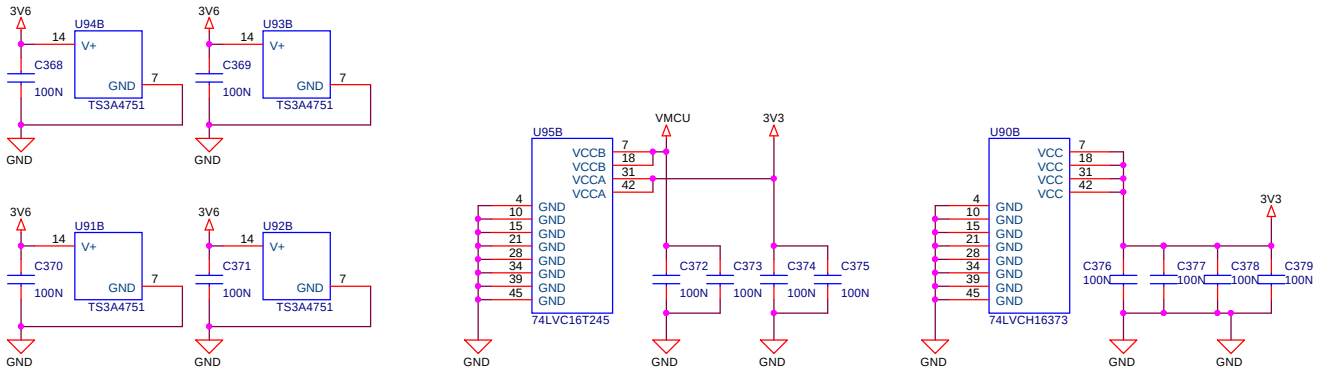


<Schematic Path> TOP	Schematic Title: **EFM32 Development Kit - Mainboard**
	Page Title: **Board Control - EFM32 bus level shift & switch**
Designed: JNO	Approved: JNO
Size: A3	BOM Doc No: <Cage Code>
Document number: **BRD3201A**	Revision: A02
Design Created Date: Wednesday, December 03, 2008	Sheet Created Date: Saturday, March 21, 2009
Sheet Modified Date: Tuesday, September 06, 2011	Sheet 15 of 22



Power & Decoupling



<Schematic Path>
TOP

Schematic Title	EFM32 Development Kit - Mainboard
Page Title	Board Control - EFM32 bus level shift & switch 2
Designed: JNO	Approved: JNO
Size: A3	BOM Doc No: <Cage Code>
Document number	BRD3201A
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Design Created Date	Wednesday, December 03, 2008
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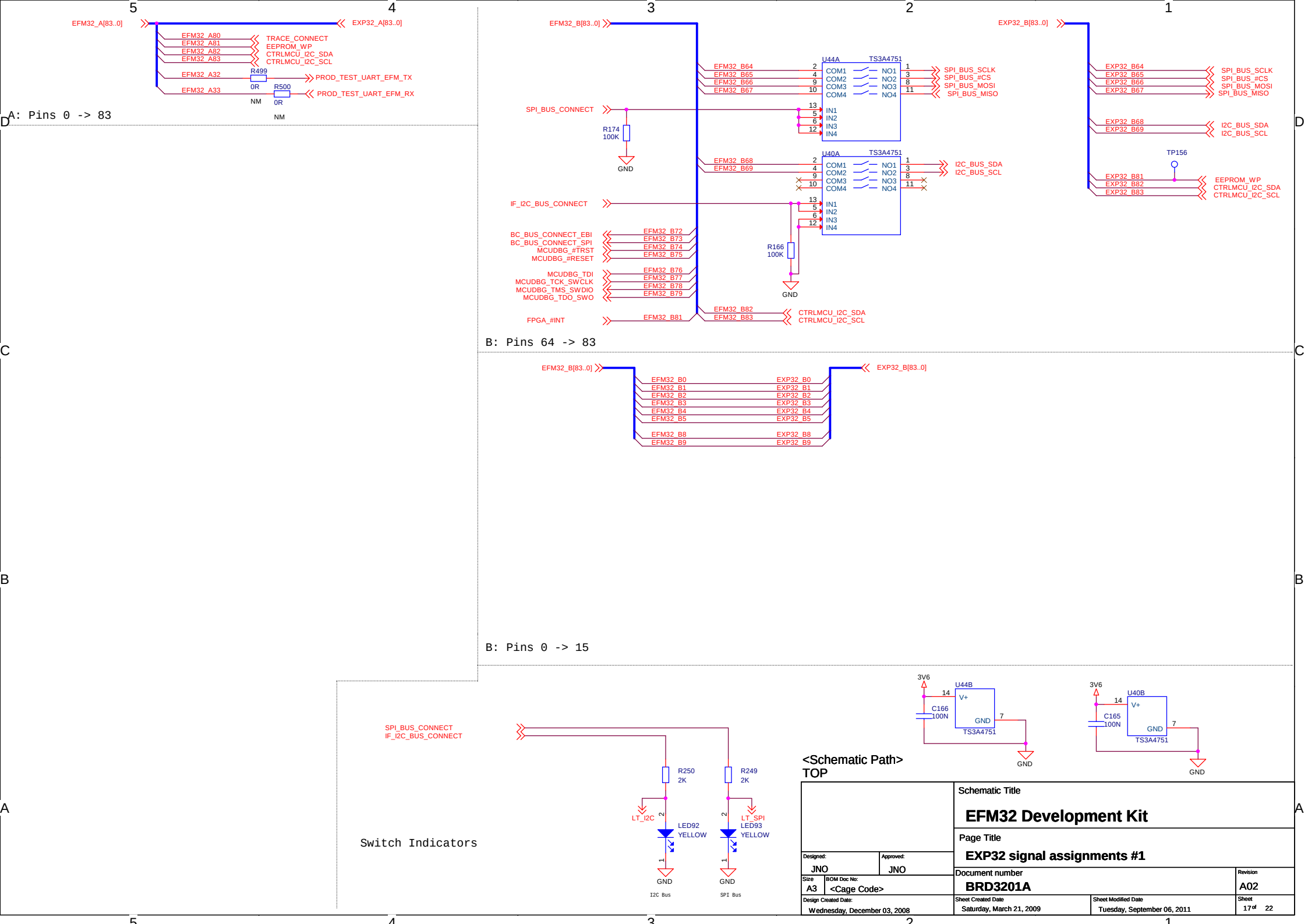
EFM32_A[83..0]
EXP32_A[83..0]
EFM32_A80
EFM32_A81
EFM32_A82
EFM32_A83
TRACE_CONNECT
EEPROM_WP
CTRLMCU_I2C_SDA
CTRLMCU_I2C_SCL
EFM32_A32
R499
0R
NM
PROD_TEST_UART_EFM_TX
EFM32_A33
R500
0R
NM
PROD_TEST_UART_EFM_RX
A: Pins 0 -> 83
EFM32_B[83..0]
EXP32_B[83..0]
U44A
TS3A4751
EFM32_B64
EFM32_B65
EFM32_B66
EFM32_B67
COM1
COM2
COM3
COM4
NO1
NO2
NO3
NO4
SPI_BUS_SCLK
SPI_BUS_#CS
SPI_BUS_MOSI
SPI_BUS_MISO
SPI_BUS_CONNECT
IN1
IN2
IN3
IN4
R174
100K
GND
U40A
EFM32_B68
EFM32_B69
I2C_BUS_SDA
I2C_BUS_SCL
IF_I2C_BUS_CONNECT
R166
100K
BC_BUS_CONNECT_EBI
BC_BUS_CONNECT_SPI
MCUDBG_#TRST
MCUDBG_#RESET
EFM32_B72
EFM32_B73
EFM32_B74
EFM32_B75
MCUDBG_TDI
MCUDBG_TCK_SWCLK
MCUDBG_TMS_SWDIO
MCUDBG_TDO_SWO
EFM32_B76
EFM32_B77
EFM32_B78
EFM32_B79
FPGA_#INT
EFM32_B81
EFM32_B82
EFM32_B83
CTRLMCU_I2C_SDA
CTRLMCU_I2C_SCL
B: Pins 64 -> 83
EXP32_B64
EXP32_B65
EXP32_B66
EXP32_B67
EXP32_B68
EXP32_B69
TP156
EXP32_B81
EXP32_B82
EXP32_B83
B: Pins 0 -> 15
EFM32_B0
EFM32_B1
EFM32_B2
EFM32_B3
EFM32_B4
EFM32_B5
EFM32_B8
EFM32_B9
EXP32_B0
EXP32_B1
EXP32_B2
EXP32_B3
EXP32_B4
EXP32_B5
EXP32_B8
EXP32_B9
SPI_BUS_CONNECT
IF_I2C_BUS_CONNECT
R250
2K
R249
2K
LT_I2C
LED92
YELLOW
LT_SPI
LED93
YELLOW
I2C Bus
SPI Bus
Switch Indicators
3V6
U44B
C166
100N
V+
GND
TS3A4751
U40B
C165
100N
<Schematic Path>
TOP
Schematic Title
EFM32 Development Kit
Page Title
EXP32 signal assignments #1
Designed:
JNO
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JNO
Size
A3
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<Cage Code>
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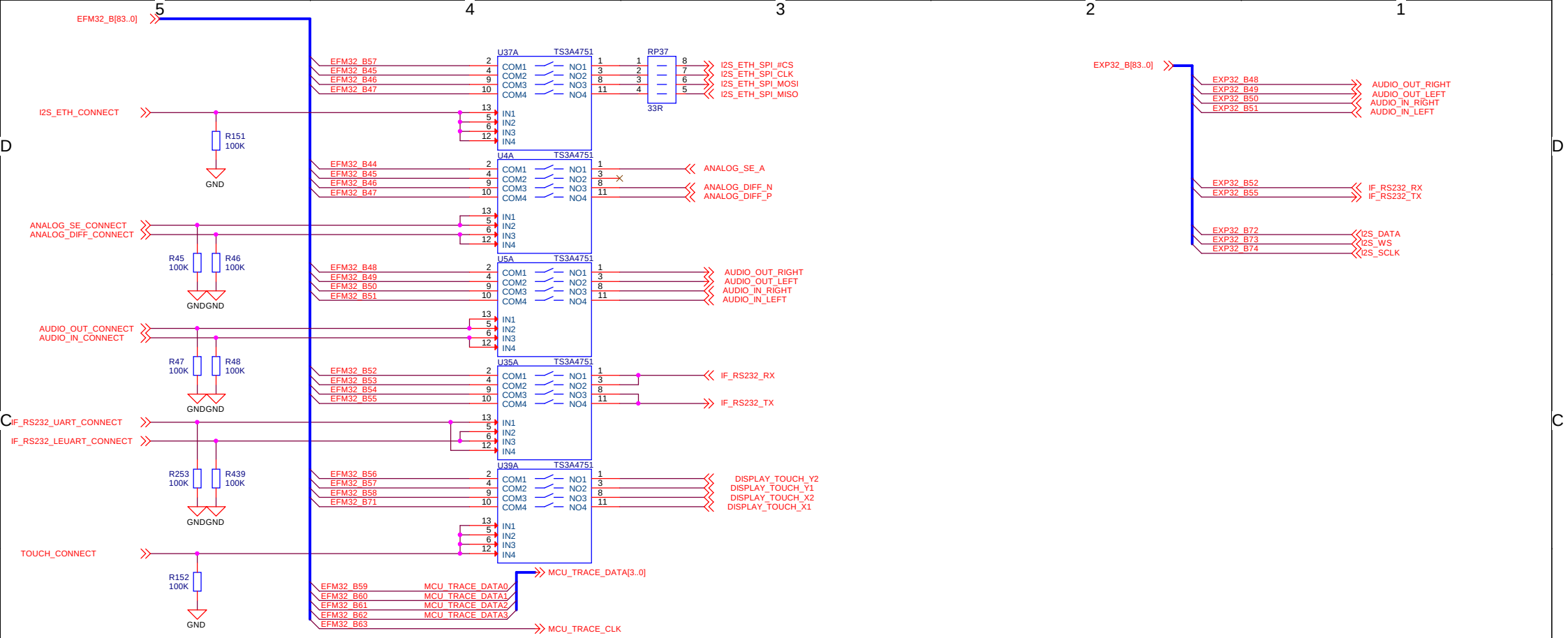
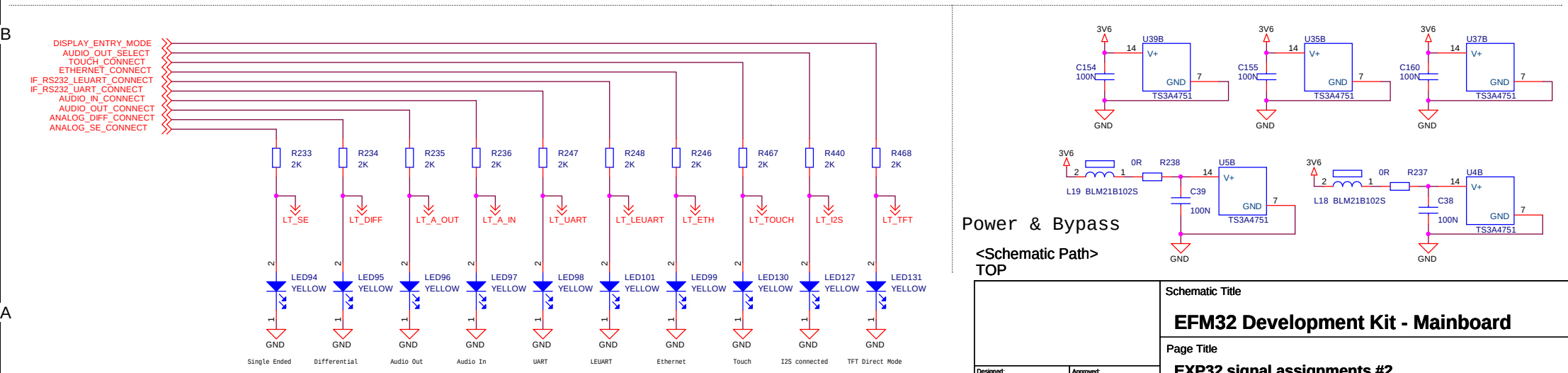


B: Pins 44 -> 63



Switch Indicators

Power & Bypass

<Schematic Path>
TOP

Schematic Title	EFM32 Development Kit - Mainboard
Page Title	EXP32 signal assignments #2
Designed: JNO	Approved: JNO
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Document number	BRD3201A
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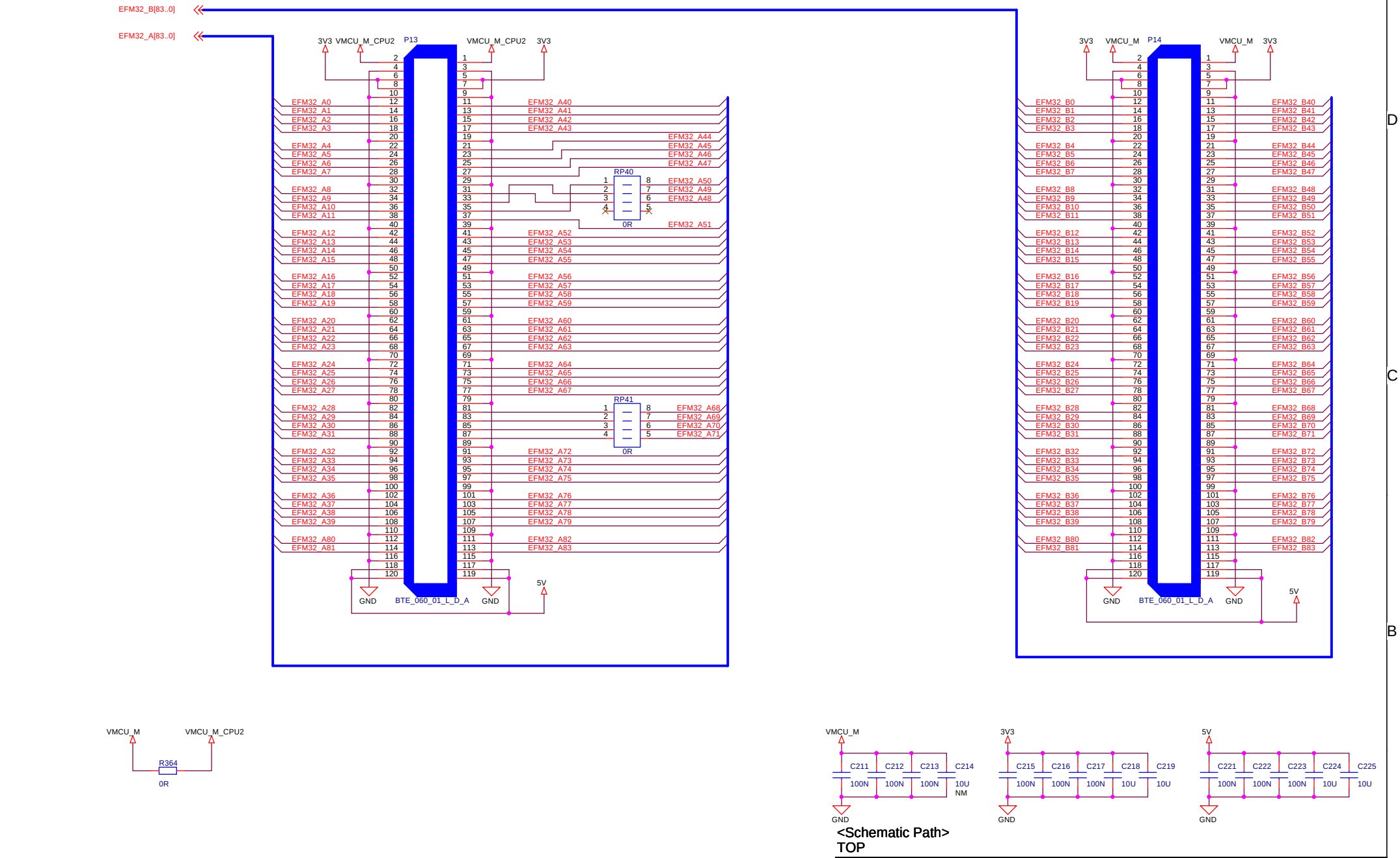

<Schematic Path>
TOP

Schematic Title	**EFM32 Development Kit - Mainboard**
Page Title	**EFM32 Board Connectors**
Designed: JNO	Approved: JNO
Size: A3	BOM Doc No: <Cage Code>
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Revision	A02
Design Created Date:	Wednesday, December 03, 2008
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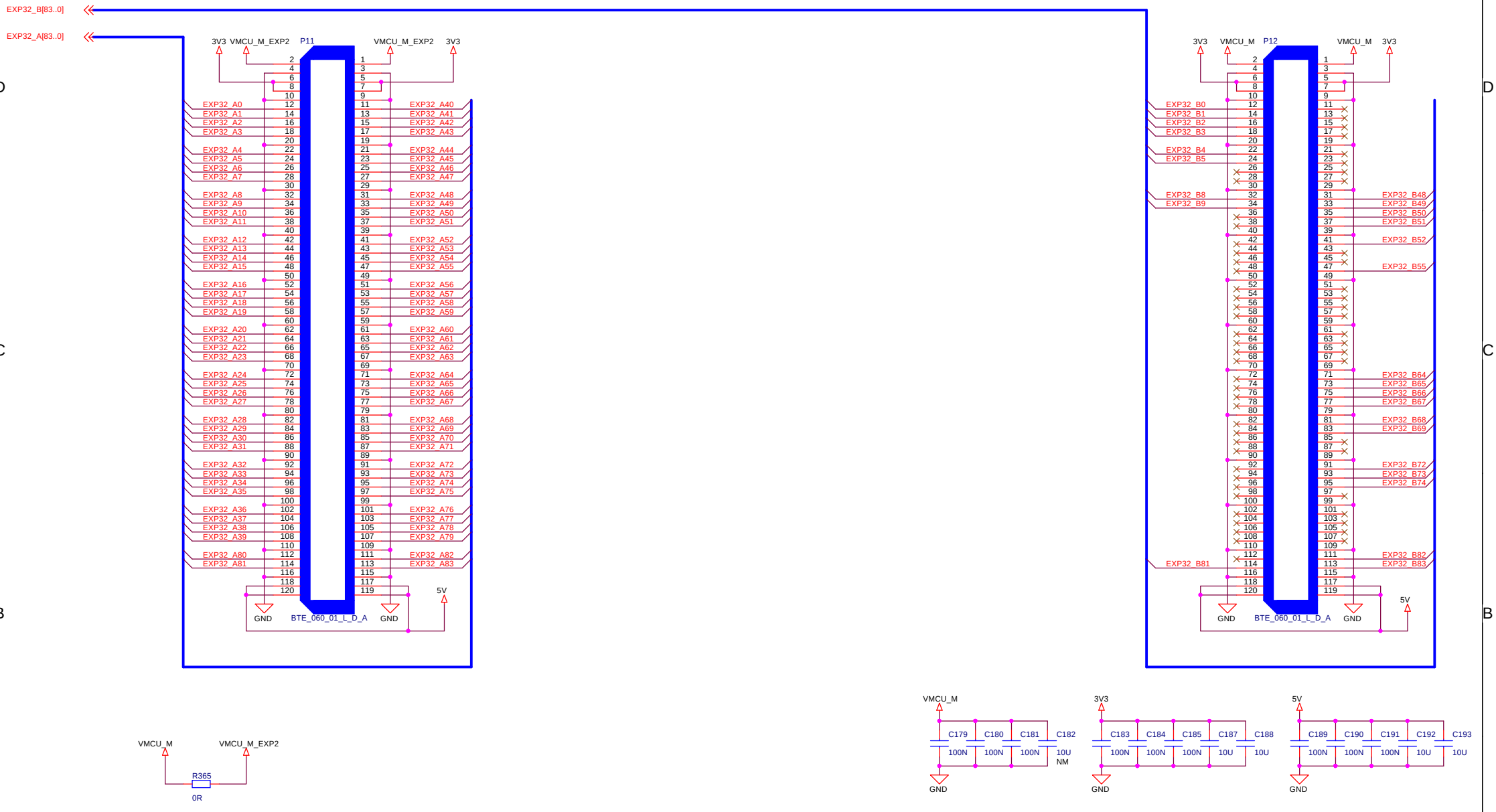

<Schematic Path>
TOP

Schematic Title	**EFM32 Development Kit - Mainboard**
Page Title	**EXP32 Board Connectors**
Designed: JNO	Approved: JNO
Size: A3	BOM Doc No: <Cage Code>
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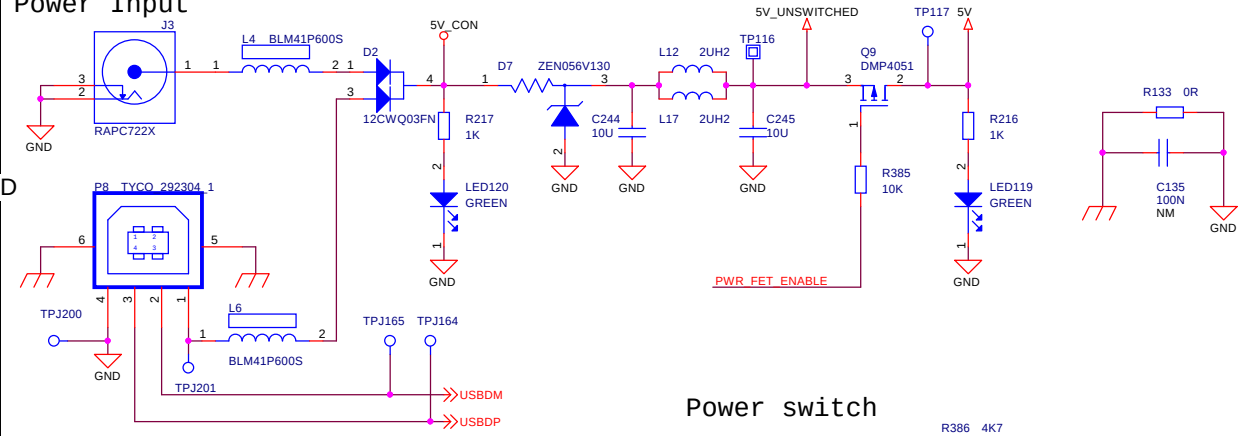
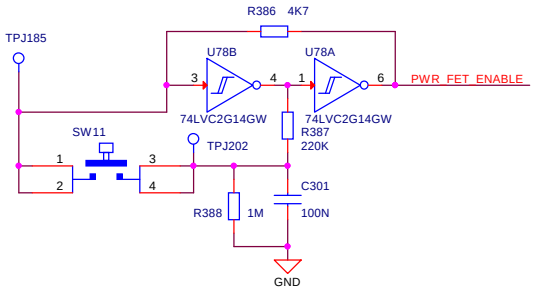
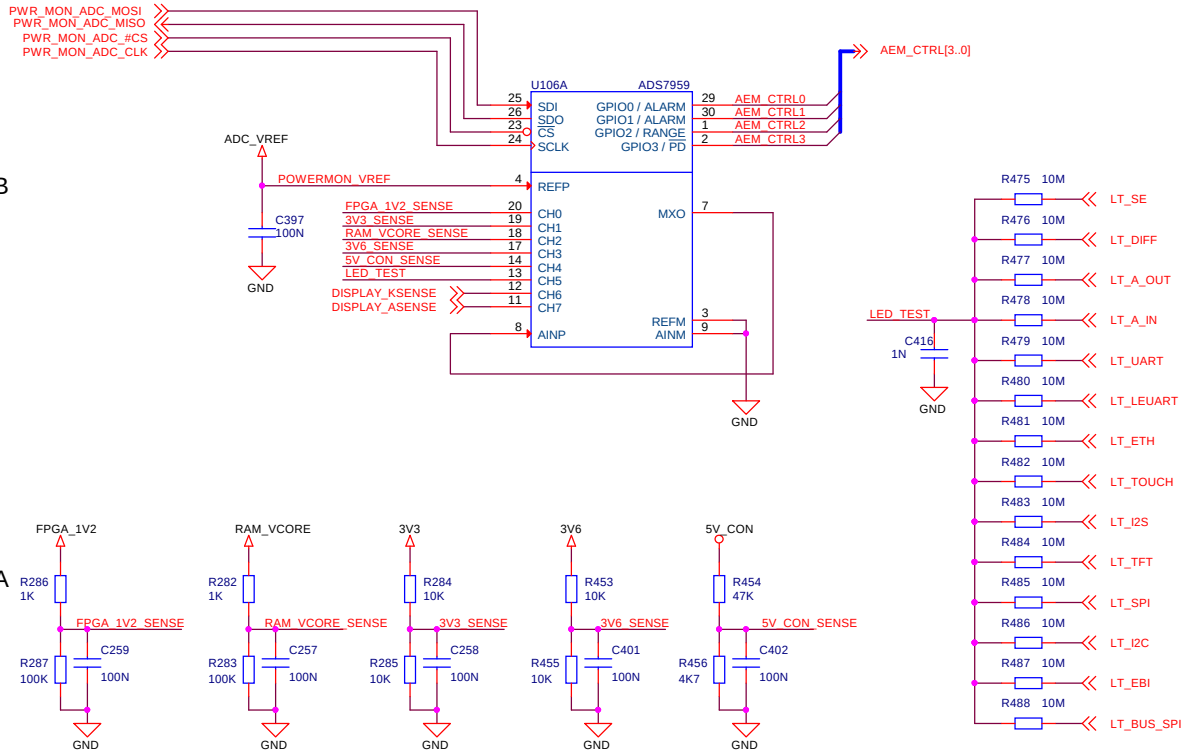
Power Input



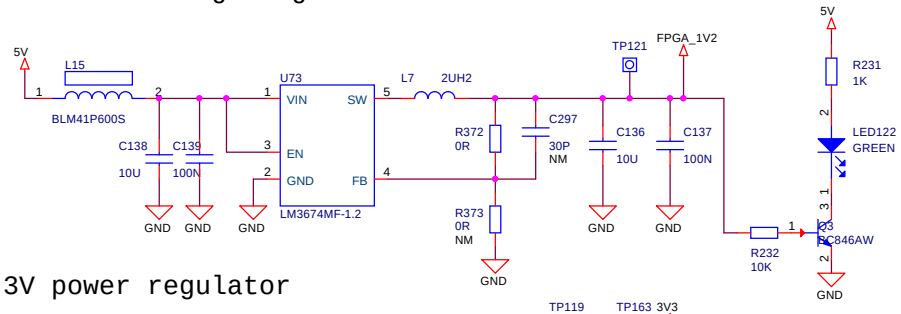
Power switch



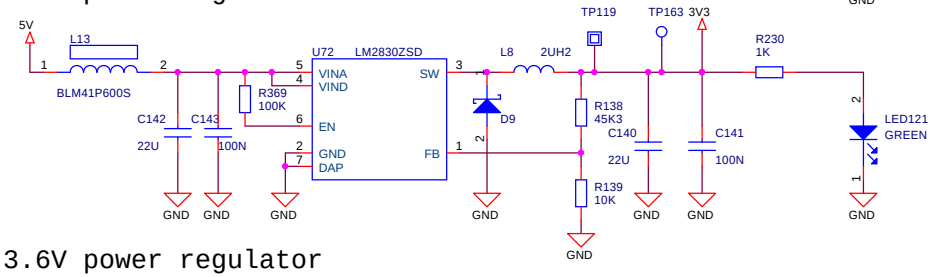
Power Monitoring



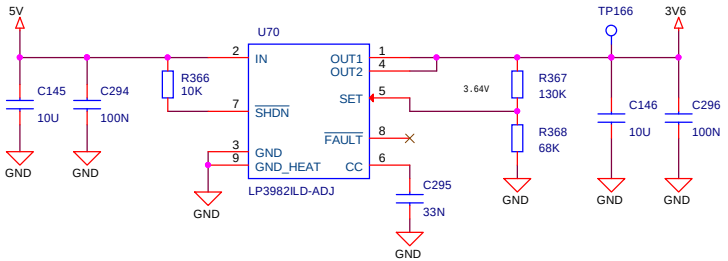
FPGA core voltage regulator



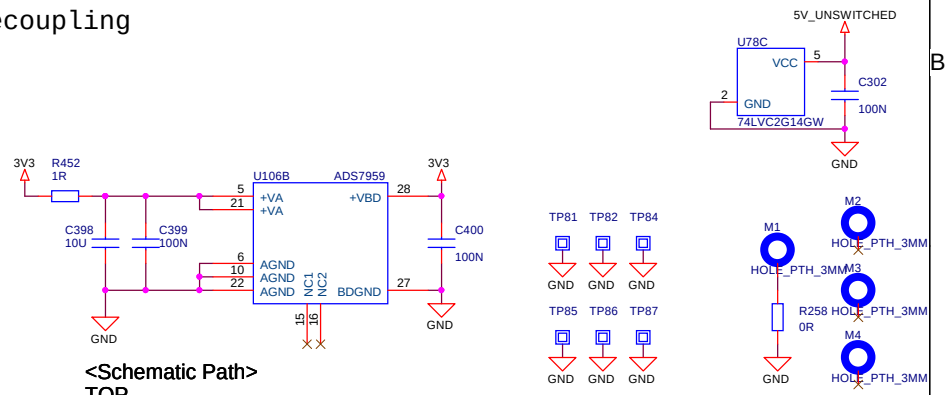
3.3V power regulator



3.6V power regulator



Decoupling



<Schematic Path>
TOP

Schematic Title	**EFM32 Development Kit - Mainboard**	
Page Title	**Main Power Regulators**	
Designed: JNO	Approved: JNO	
Size: A3	BOM Doc No: <Cage Code>	Document number: **BRD3201A** — Revision: A02
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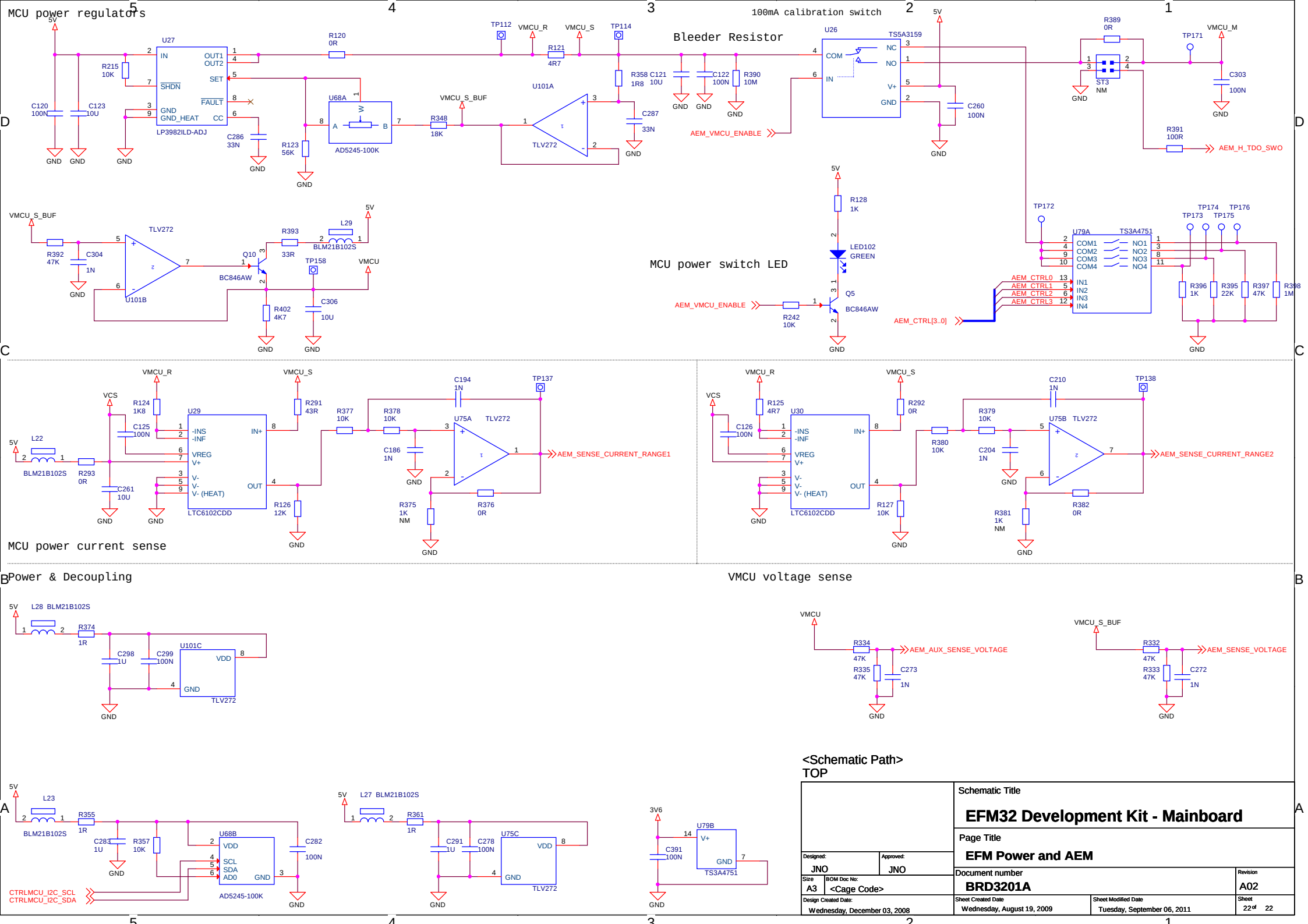
MCU power regulators
100mA calibration switch
Bleeder Resistor
U27
LP3982ILD-ADJ
U68A
AD5245-100K
U101A
TLV272
U26
TS5A3159
AEM_VMCU_ENABLE
AEM_H_TDO_SWO
VMCU_S_BUF
U101B
MCU power switch LED
LED102
GREEN
Q5
BC846AW
U79A
TS3A4751
AEM_CTRL[3..0]
MCU power current sense
U29
LTC6102CDD
U75A
AEM_SENSE_CURRENT_RANGE1
VMCU voltage sense
U30
U75B
AEM_SENSE_CURRENT_RANGE2
Power & Decoupling
U101C
AEM_AUX_SENSE_VOLTAGE
AEM_SENSE_VOLTAGE
CTRLMCU_I2C_SCL
CTRLMCU_I2C_SDA
U68B
U75C
U79B
Schematic Path
TOP
Schematic Title
EFM32 Development Kit - Mainboard
Page Title
EFM Power and AEM
Designed: JNO
Approved: JNO
Size A3
BOM Doc No: <Cage Code>
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