

EFM32 Leopard Gecko STK

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Revision History

Rev.	Description
A00	Initial version for series production
A01	Updated EFM32 to Leopard Gecko Rev.D
A02	Added test points for EFM USB. Fixed small error on PCB.

STK

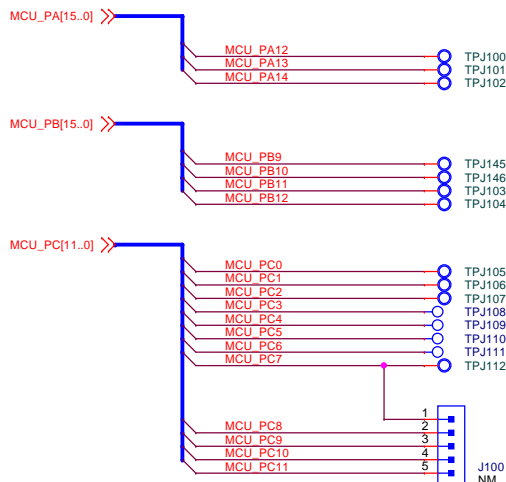
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		Page Title	
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Designed: DDB	Approved: JNO	Document number BRD2201A	Revision A02
Size A3	BOM Doc No:	Sheet Created Date Saturday, March 21, 2009	Sheet Modified Date Thursday, June 14, 2012
Design Created Date: Wednesday, December 03, 2008		Sheet 1 of 10	

Breakout Connections

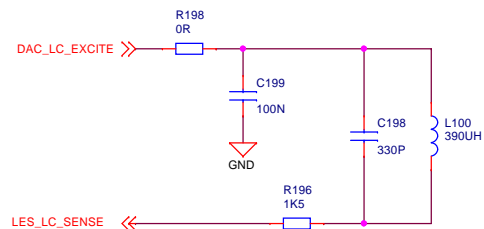
The diagram illustrates the breakout connections for three MCU pin groups: PA, PB, and PC. Each group is connected to a set of TPJ breakout boards.

- MCU_PA[15..0]** is connected to TPJ100, TPJ101, and TPJ102.
- MCU_PB[15..0]** is connected to TPJ145, TPJ146, TPJ103, and TPJ104.
- MCU_PC[11..0]** is connected to TPJ105, TPJ106, TPJ107, TPJ108, TPJ109, TPJ110, TPJ111, and TPJ112.

MCU_PC[11..0] is also connected to a J100 NM breakout board, which has pins 1 through 5 labeled.



LESENSE LC-Sensor



Power

TPJ133
TPJ134
TPJ135
TPJ136
TPJ137
TPJ138

GND

VMCU

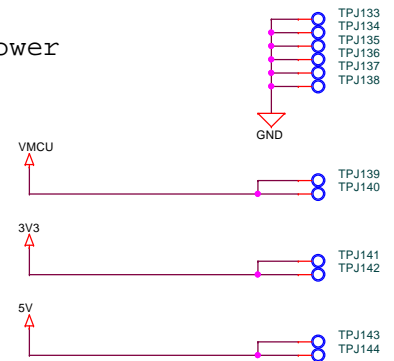
TPJ139
TPJ140

3V3

TPJ141
TPJ142

5V

TPJ143
TPJ144

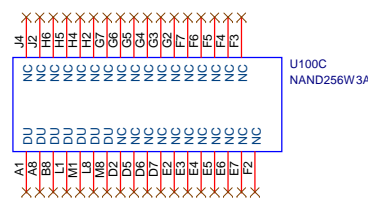
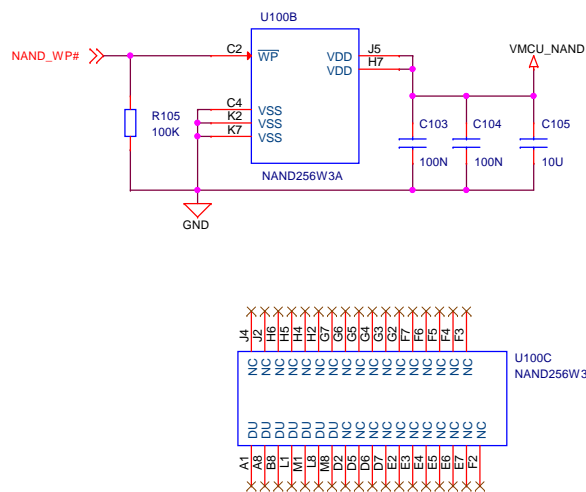
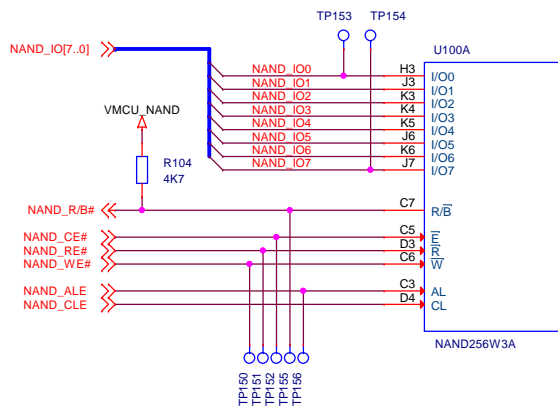


32MB NAND Flash

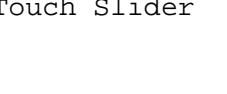
The diagram illustrates the connection of a 32MB NAND Flash to a U100A microcontroller. The U100A is shown as a blue box with pins for I/O, address, and control signals. The NAND flash is represented by a stack of eight chips (NAND IO0 to NAND IO7) connected to a VMCU NAND block. The VMCU NAND block is connected to the NAND flash chips via a 4K7 resistor (R104). The NAND flash chips are connected to the U100A pins via jumpers (TP150 to TP156).

U100A Pin	Signal	Connection
H3	I/O0	NAND IO0
J3	I/O1	NAND IO1
K3	I/O2	NAND IO2
K4	I/O3	NAND IO3
K5	I/O4	NAND IO4
J6	I/O5	NAND IO5
K6	I/O6	NAND IO6
J7	I/O7	NAND IO7
C7	R/B	NAND_R/B#
C5	TE	NAND_CE#
D3	TR	NAND_RE#
C6	W	NAND_WE#
C3	AL	NAND_ALE
D4	CL	NAND_CLE

Additional components and connections shown include a 4K7 resistor (R104) connected to the VMCU NAND block, and jumpers TP150 through TP156 connecting the NAND flash chips to the U100A pins.



3 Touch Slider



The diagram illustrates the Touch Slider component. It features a blue block labeled "TOUCH SLIDER" with a "T1" input on the left. Four red lines represent the output signals: "UIF TOUCH0", "UIF TOUCH1", "UIF TOUCH2", and "UIF TOUCH3". These signals are connected to a blue bus labeled "UIF_TOUCH[3..0]" on the left, which has a double arrow pointing towards the bus.

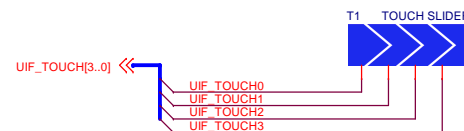
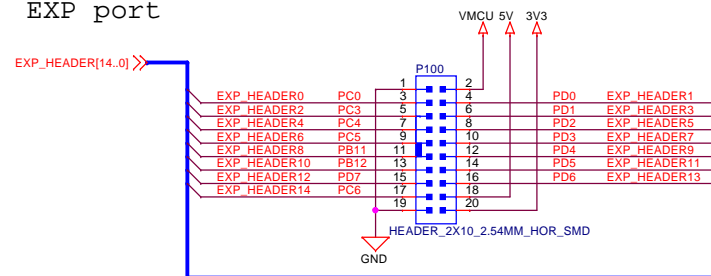


Diagram illustrating the EXP port connections. The EXP_HEADER[14..0] bus is connected to a 20-pin connector labeled P100. The connections are as follows:

Header Pin	Header Label	Connector Pin	Connector Label
0	EXP HEADER0	1	PC0
2	EXP HEADER2	3	PC3
4	EXP HEADER4	5	PC4
6	EXP HEADER6	7	PC5
8	EXP HEADER8	11	PB11
10	EXP HEADER10	13	PB12
12	EXP HEADER12	15	PD7
14	EXP HEADER14	17	PC6
-	GND	19	GND

Additional connections shown on the right side of the connector:

- Pin 2: VMCU 5V
- Pin 3: 3V3
- Pin 4: 3V3
- Pin 20: HEADER_ZX10_2.54MM_HOR



Q100
TEMT6200FX01

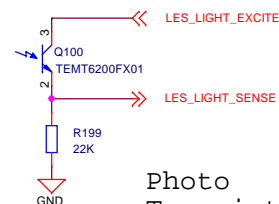
LES_LIGHT_EXCITE

LES_LIGHT_SENSE

R199
22K

GND

Photo Transistor



User pushbuttons

VMCU

R101 1M

R102 1M

SW100

SW101

R100 100R

R103 100R

C100 1N

C101 1N

UIF_PB0

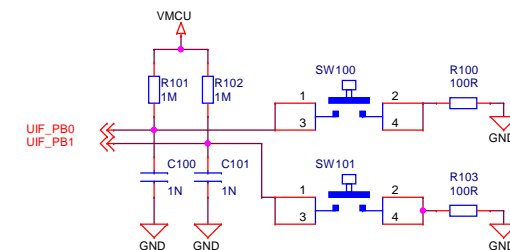
UIF_PB1

GND

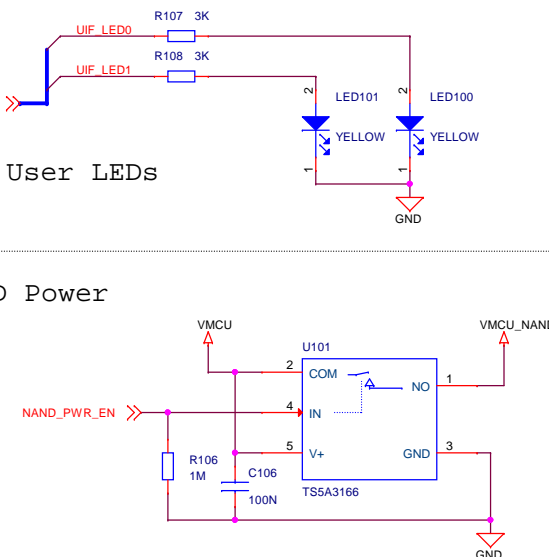
GND

GND

GND



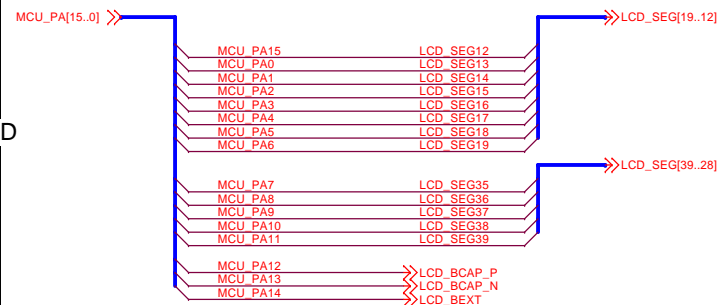
EXP Communication	
PD0 EXP HEADER1 PD1 EXP HEADER3 PD2 EXP HEADER5 PD3 EXP HEADER7 PD4 EXP HEADER9 PD5 EXP HEADER11 PD6 EXP HEADER13	MOSI-PD0 MISO-PD1 CLK-PD2 CS-PD3
	I2C1 SDA-PC4 SCL-PC5
	UART TX-PD0 RX-PD1
	LEUART TX-PD4 RX-PD5



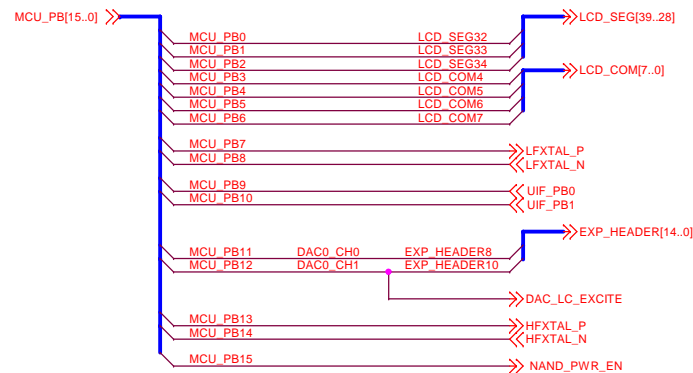
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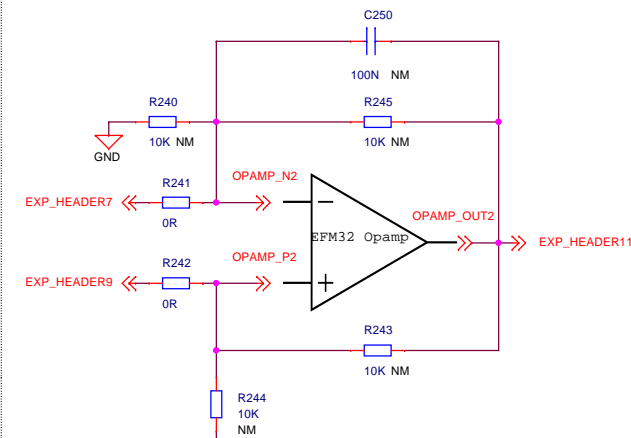
PA Connections



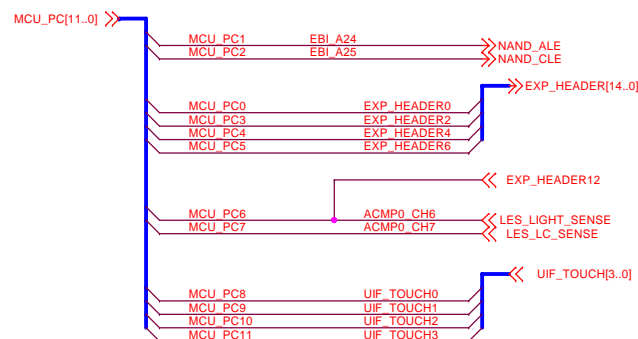
PB Connections



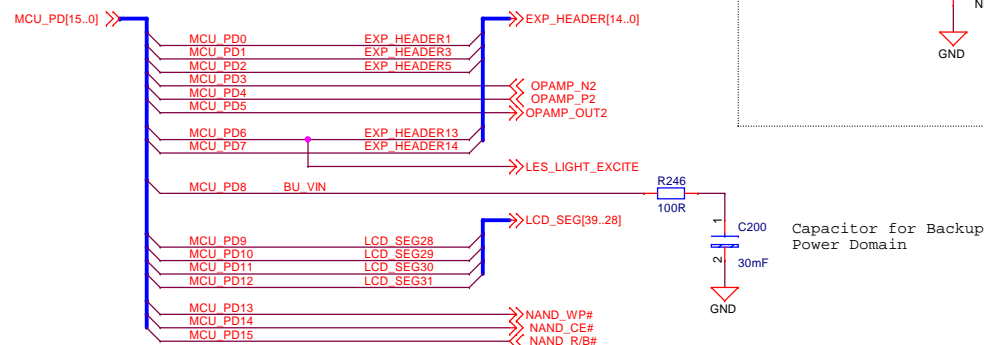
OPAMP Connection Footprint



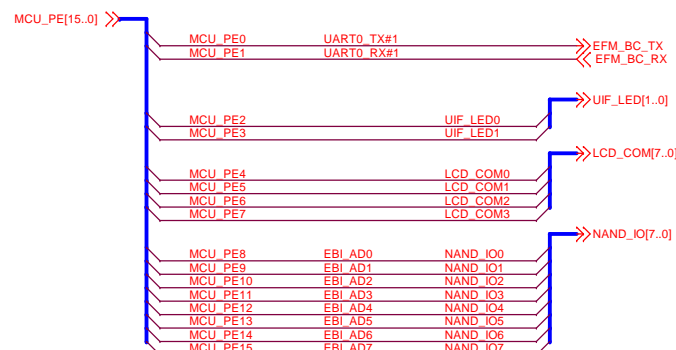
PC Connections



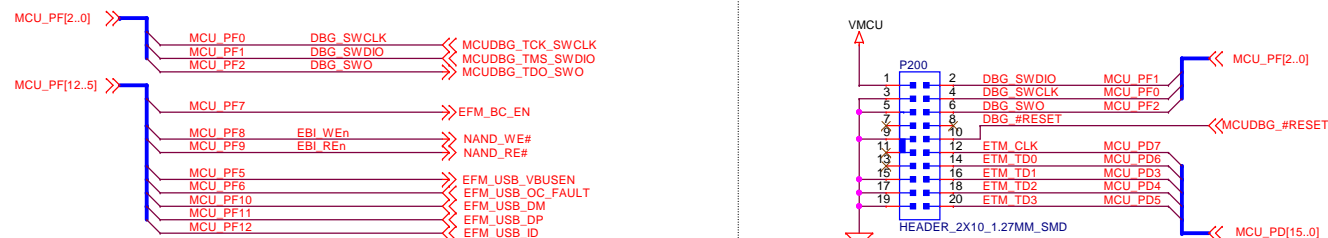
PD Connections



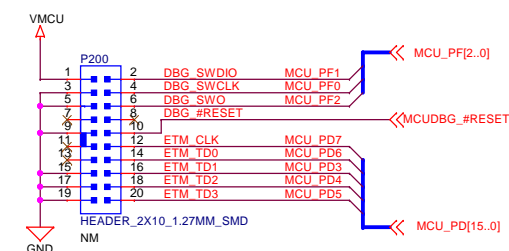
PE Connections



PF Connections

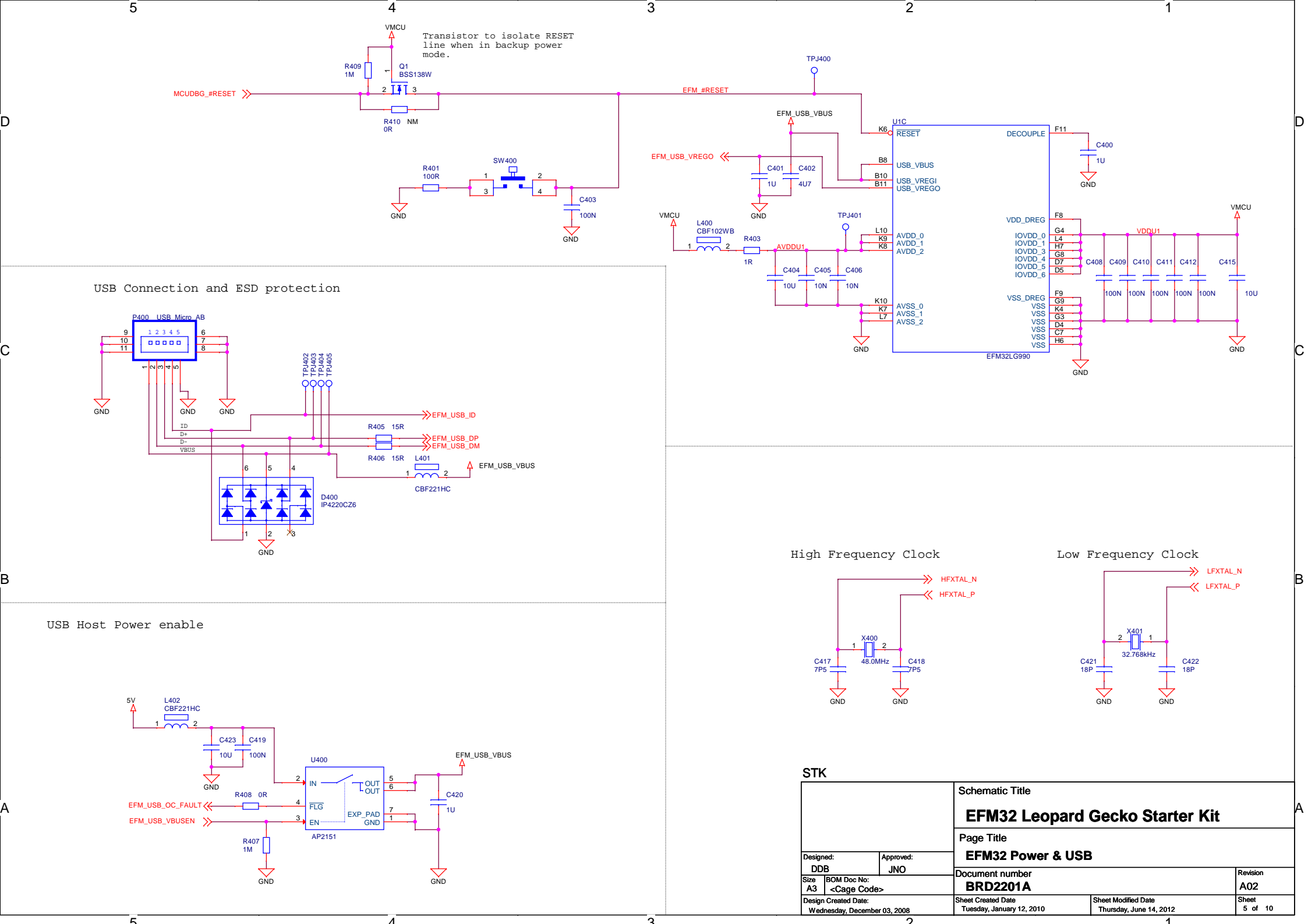


19-pin JTAG/SWD and Trace connector footprint
(reverse side)

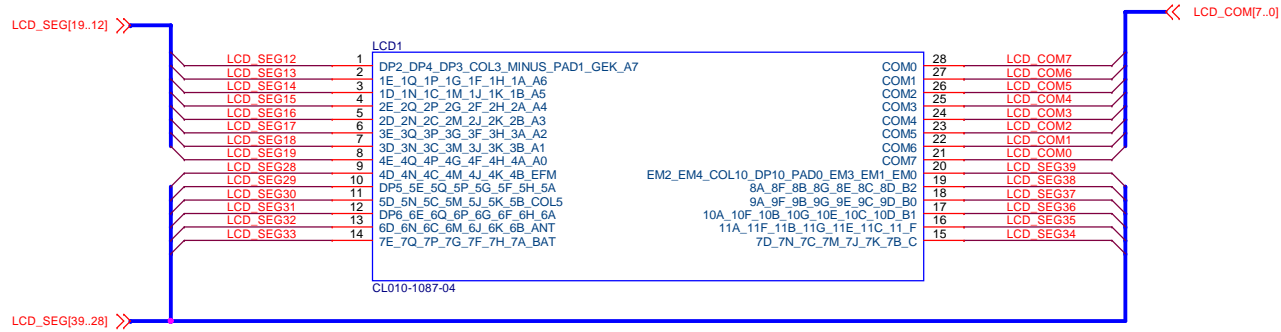


STK

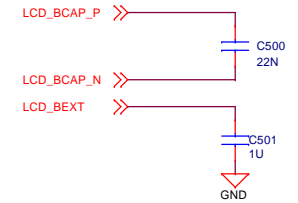
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Signal Assignments			
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LCD signal connections



LCD Boost

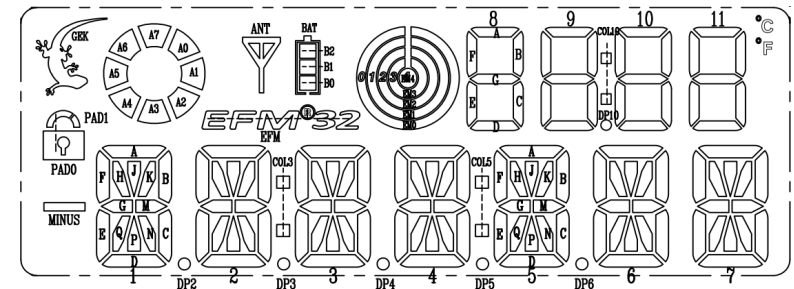


Segment names

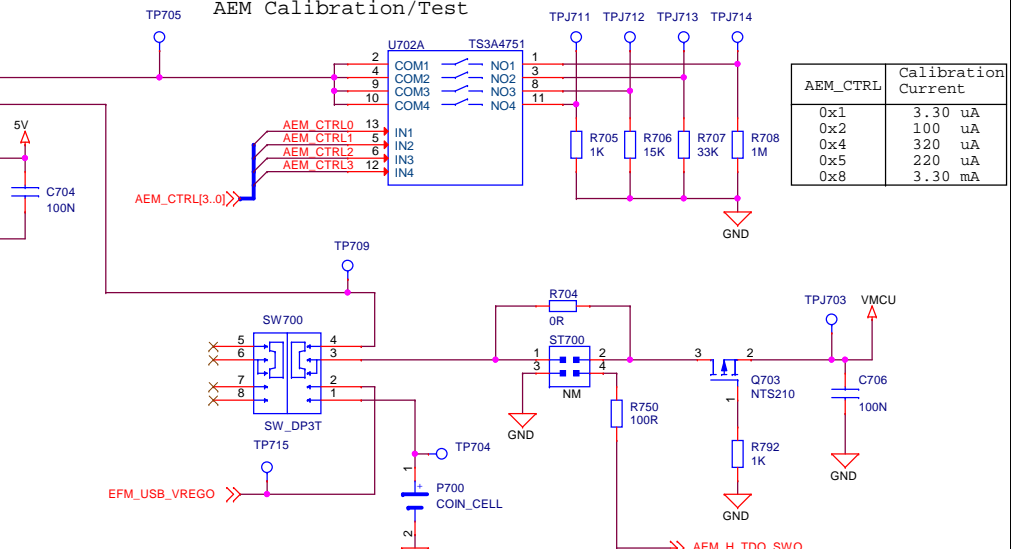
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COM0	DP2	1 E	1 D	2 E	2 D	3 E	3 D	4 E	4 D	DP5	5 D	DP6	6 D	7 E
COM1	DP4	1 Q	1 N	2 Q	2 N	3 Q	3 N	4 Q	4 N	5 E	5 N	6 E	6 N	7 Q
COM2	DP3	1 P	1 C	2 P	2 C	3 P	3 C	4 P	4 C	5 Q	5 C	6 Q	6 C	7 P
COM3	COL3	1 G	1 M	2 G	2 M	3 G	3 M	4 G	4 M	5 P	5 M	6 P	6 M	7 G
COM4	MINUS	1 F	1 J	2 F	2 J	3 F	3 J	4 F	4 J	5 G	5 J	6 G	6 J	7 F
COM5	PAD1	1 H	1 K	2 H	2 K	3 H	3 K	4 H	4 K	5 F	5 K	6 F	6 K	7 H
COM6	GEK	1 A	1 B	2 A	2 B	3 A	3 B	4 A	4 B	5 H	5 B	6 H	6 B	7 A
COM7	A7	A6	A5	A4	A3	A2	A1	A0	EFM	5 A	COL5	6 A	ANT	BAT

PIN	15	16	17	18	19	20	21	22	23	24	25	26	27	28
---	S14	S15	S16	S17	S18	S19	COM7	COM6	COM5	COM4	COM3	COM2	COM1	COM0
COM0	7 D	11 A	10 A	9 A	8 A	EM2								COM0
COM1	7 N	11 F	10 F	9 F	8 F	EM4							COM1	
COM2	7 C	11 B	10 B	9 B	8 B	COL10						COM2		
COM3	7 M	11 G	10 G	9 G	8 G	DP10					COM3			
COM4	7 J	11 E	10 E	9 E	8 E	PAD0				COM4				
COM5	7 K	11 C	10 C	9 C	8 C	EM3		COM5						
COM6	7 B	11 D	10 D	9 D	8 D	EM1		COM6						
COM7	°C	°F	B1	B0	B2	EM0	COM7							

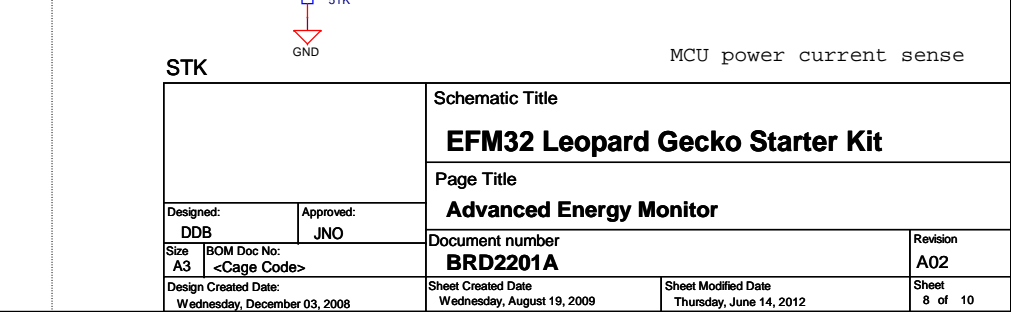
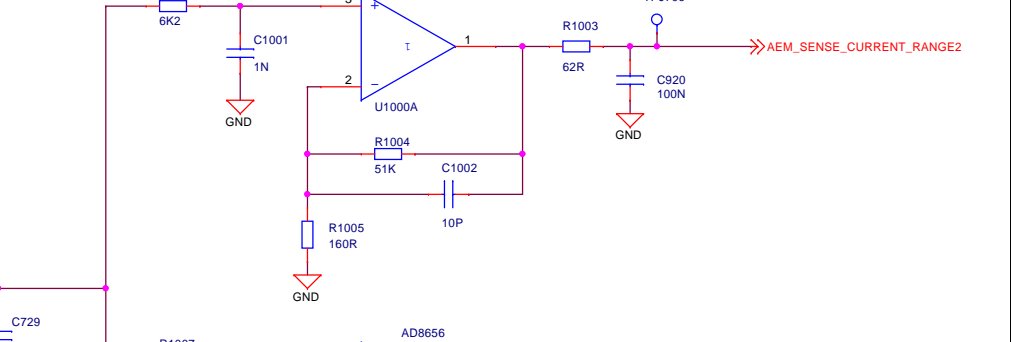
Segment placement



1



AEM_CTRL	Calibration Current
0x1	3.30 uA
0x2	100 uA
0x4	320 uA
0x5	220 uA
0x8	3.30 mA

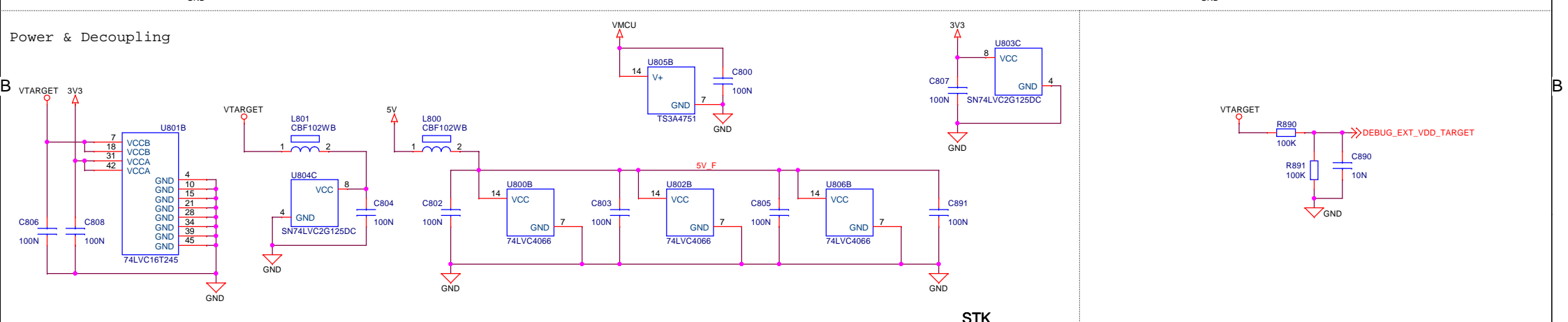
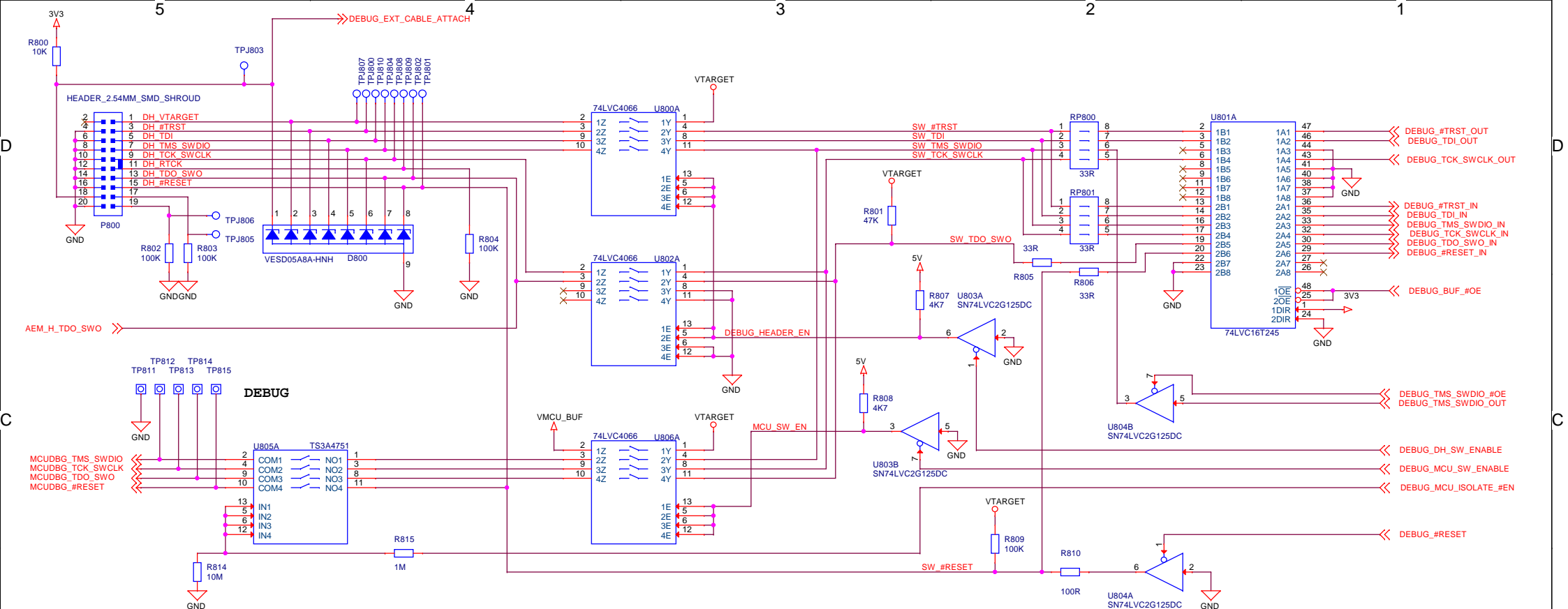


STK

GND

MCU power current sense

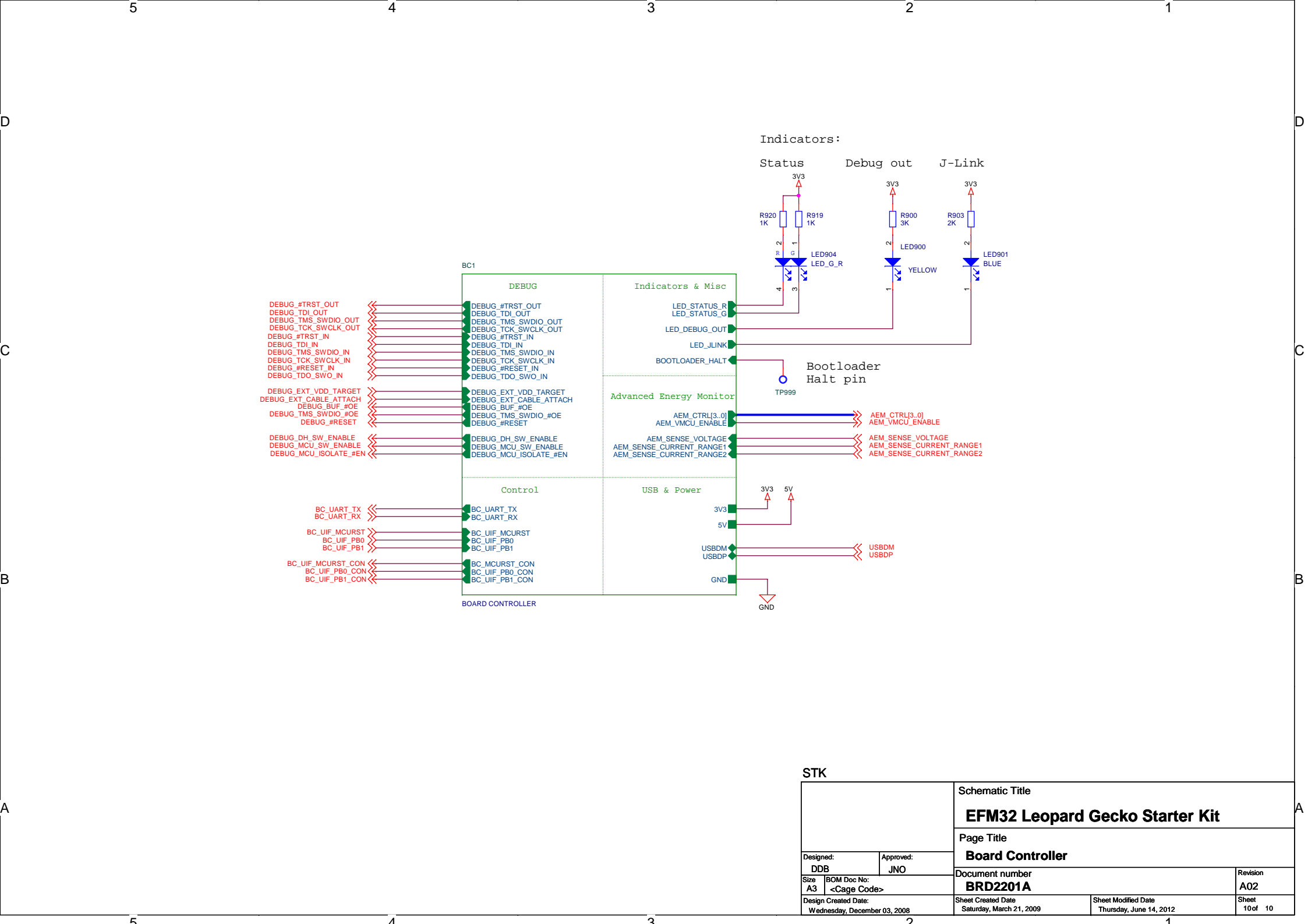
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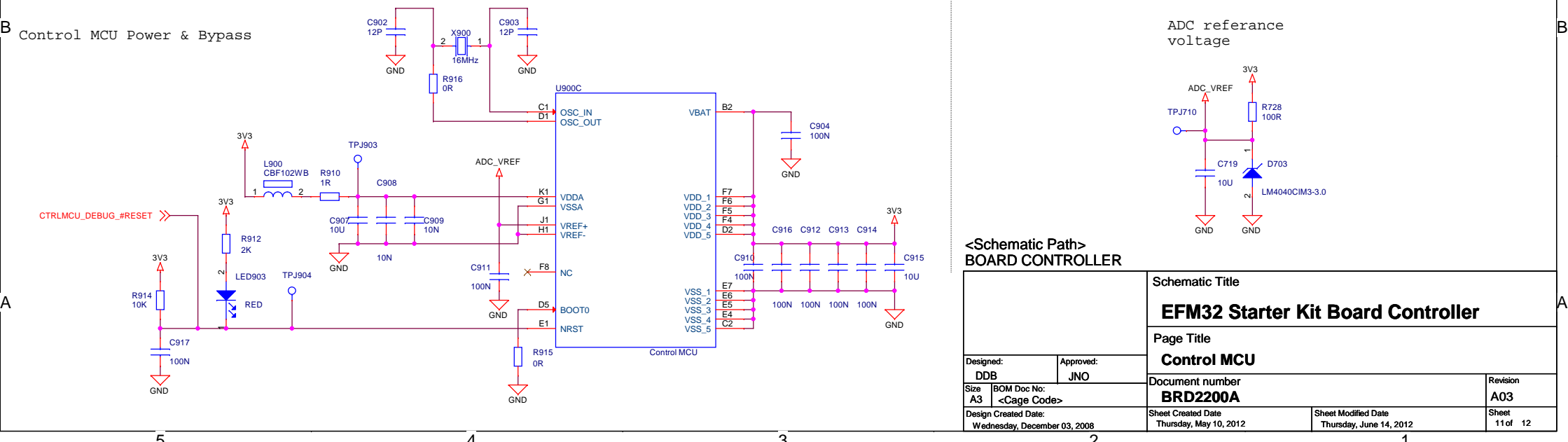
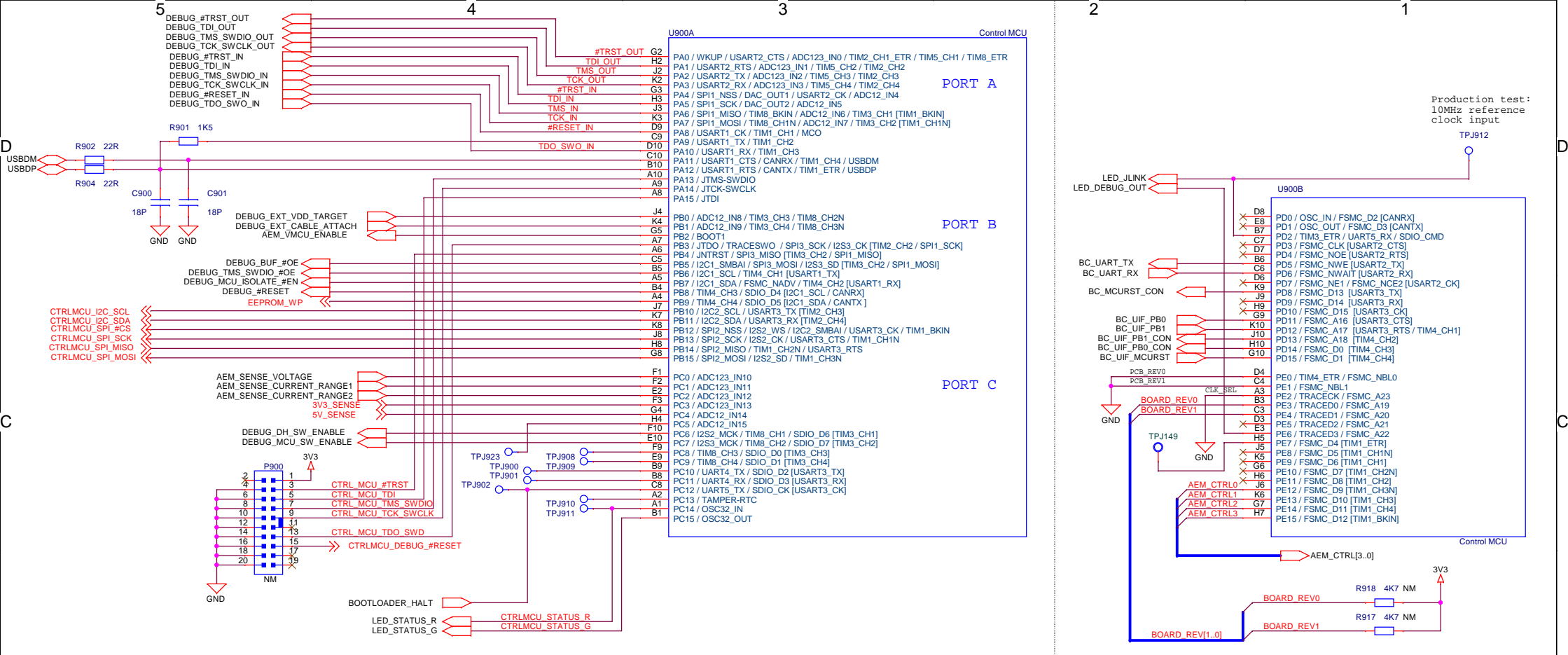


Mode						
Mode	DEBUG_MCU_SW_ENABLE	DEBUG_DH_SW_ENABLE	DEBUG_BUF_#OE	ISOLATE_#EN	DH_VTARGET	VTARGET
Debug Out	0	1	0	0	External voltage	External voltage
MCU Debug	1	0	0	1	Disconnected	VMCU
Debug In	1	1	1	1	VMCU	VMCU
Debug Off	1	1	1	0	-	-

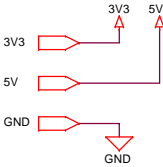
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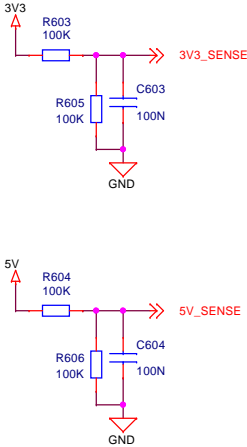




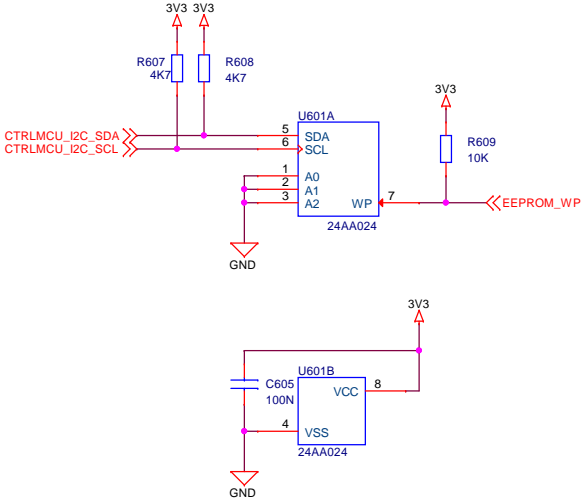
POWER INPUTS



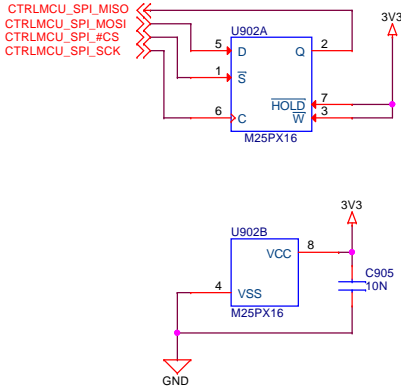
POWER SENSE



CTRLMCU EEPROM



CTRLMCU SERIAL FLASH



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BOARD CONTROLLER

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