*** PCB SPECIFICATION FOR CIRCUIT BOARD MANUFACTURING ***

PRODUCT OWNER : Energy Micro AS
DOCUMENT/BOARD : PCB2201 REV. A00
DATE : 2012-03-30
REVISION : A00

PREPARED BY : Ole Jacob Bryhni Frostad
BOARDS pr PANEL: 4 (1 X 4)
PANEL SIZE : 126.0 x 260.0 mm
BOARD SIZE : 110.0 x 55.0 mm
BOARD THICKNESS: 1.6 mm +/- 10 %
NO OF LAYERS : 6
MATERIAL(S) : Glass Epoxy FR-4, NEMA Class 2, UL 94V-0, Tg min 150 C
Materials in compliance with the RoHS and WEEE directives
MARKINGS: Logo, Week/Year, UL
(Avoid areas reserved for DataMatrix, Barcodes or Lables)
QUALITY REQ. : IPC-A-600 (current revisions) Class 2, and IPC specifications
refered to by IPC-A-600
GENERAL REQ. : If applicable, the following requirements are valid:
- If Build-Up (Stack-Up) is specified, follow Build-Up,
otherwise use (board manufacturer) standard Build-Up.
- Copper balancing may be applied on break-away-tabs,
or otherwise outside board outline(s), but must have
a minimum 1.5 mm clearance to possible fiducials.
- Break-away areas may be used for patterns, holes etc
by manufacturer for QA purposes.
- Inner radius (contour) 1.2 mm, unless stated otherwise.
- Manufacturer may plug tented via holes to improve yield.
COPPER THK. : SEE BUILD UP
COPPER PASSIV. : ENIG to meet IPC-4552 requirements, except Nickel thickness
must be minimum 4 um. (Electroless Nickel/Immersion Gold)
RESIST MASK : Photo Polymer Wet film, BLACK NB!
to IPC-SM-840 Class T requirements (current revision)
VIA HOLES : TENTED (OVERPRINTED, NOT PLUGGED) IPC-4761 Type I
UNLESS OPTIONALLY: EXPLICIT OTHER VIA TREATMENT REQUESTED
LEGEND COLOUR : WHITE
LEGEND LAYER(S): BOTH SIDES
CONTROLLED IMP : Design has Controlled impedances. Follow Build up strictly!
Unless explicitly stated otherwise, controlled impedance
has been designed into the board. Use of test strip is
hence normally not required.
NOMINAL VALUES for Width, Spacing and VIA Diameter:
Cu TRACK(TRACE): Minimum conductor width : 0.10 mm (4 mils)
Cu SPACING : Minimum conductor spacing: 0.10 mm (4 mils)
MINIMUM VIA : Minimum via pad diameter : 0.48 mm (19 mils)
Min via hole (SEE HOLE INFORMATION FURTHER DOWN)
Min via hole may have more than one pad diameter.

(SPECIFICATION CONTINUED ON NEXT PAGE)

BUILD UP :

```
L1  ============================   35 um Cu (1.0 Oz)
    /////////// C O R E ///////////  100 um
L2  ============================   18 um Cu (0.5 Oz)
    - - - - P R E P R E G - - - -  128 um
L3  ============================   18 um Cu
- - /////////// C O R E /////////// 1000 um  - - CENTER - -
L4  ============================   18 um Cu
    - - - - P R E P R E G - - - -  128 um
L5  ============================   18 um Cu
    /////////// C O R E ///////////  100 um
L6  ============================   35 um Cu
```

TEST : 100% Electrical Test
Optical test, AOI (with automatic scanner)
Visual inspection
(Generate netlist from Gerber and Drill files)

NC DRILL - HOLE INFORMATION:

WARNING: Drill dimensions must be taken from the Excellon (.exc) file(s).
NON-PLATED holes may have a small center marker in the Gerber files.
Under no circumstance must these Gerber flashes be mistaken for the
hole drill dimensions!

The drill file may contain slots. See drill information below.
The Gerber file mb2201.gex may also contain slot information.
Dimensions for the finished board (after plating).
Tolerances +/- 0.1 mm, unless specified otherwise below.
Via Holes +0.1 mm/-Via Size, unless specified otherwise below.

PLATED HOLES:
T01 VH DIA = 0.25 mm QTY = 2384 (VIA-HOLES)
T02 VH DIA = 0.3 mm QTY = 1216 (VIA-HOLES)
T03 PTH DIA = 0.8 mm QTY = 112
T04 PTH DIA = 0.9 mm QTY = 32
T05 PTH DIA = 1.0 mm QTY = 228
T06 PTH DIA = 3.0 mm QTY = 4

NON-PLATED HOLES:
T07 NP DIA = 0.5 mm QTY = 40
T08 NP DIA = 0.9 mm QTY = 8
T09 NP DIA = 1.6 mm QTY = 8
T10 NP DIA = 3.0 mm QTY = 8

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+++ YOUR CIRCUIT BOARD DESIGN PARTNER +++

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