



EFM8SB10 Sleepy Bee STK


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Revision History

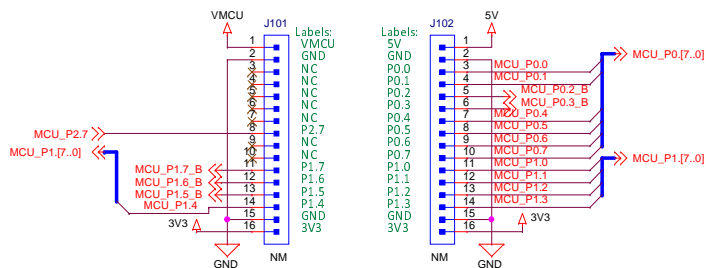
Rev.	Description
A00	Initial version released for production.
A01	Minor updates to design after prototype series. Updated PCB.
A02	Updated PCB revision.



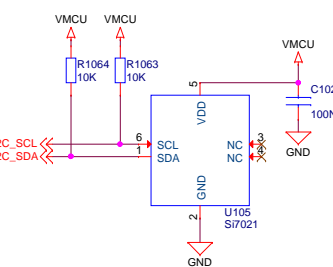
STK

 SILICON LABS®		Schematic Title EFM8SB1 Sleepy Bee Starter Kit	
Designed: MRW		Page Title Title Page	
Size A3	BOM Doc No:	Document number BRD5101A	Revision A02
Design Created Date: Wednesday, December 03, 2008		Sheet Created Date Thursday, May 15, 2014	Sheet Modified Date Monday, March 23, 2015
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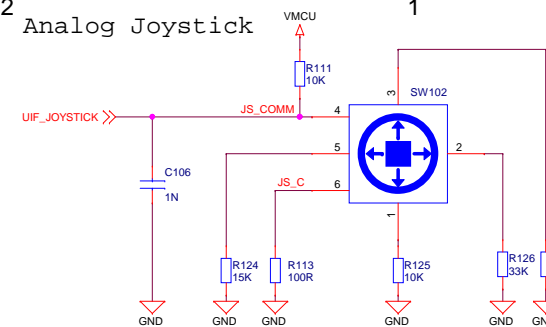
Breakout Connections



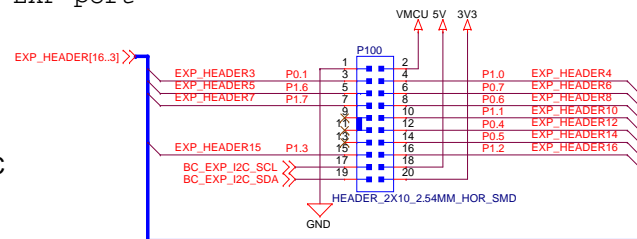
Temperature & Relative Humidity Sensor



Analog Joystick



EXP port



EXP-Header Functionality

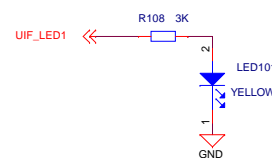
** Indicates potential STK hardware conflicts

1	GND		ADC0.1
3	P0.1		
5	P1.6		
7	P1.7		
9			
11			
13			
15	P1.3	I2C0_SCL	ADC0.11
17			Reserved for EXP Board Identification
19			

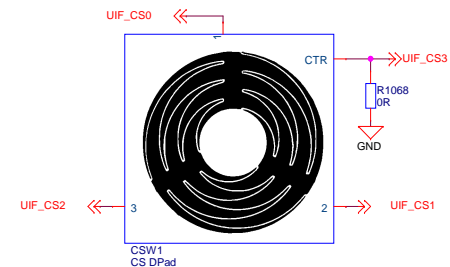
2	VMCU		
4	P1.0	SPI0_MOSI	CMP0P
6	P0.7	SPI0_MISO	ADC0.7
8	P0.6	SPI0_SCK	ADC0.6
10	P1.1	SPI0_NSS	CMP0N
12	P0.4	UART0_TX	ADC0.4
14	P0.5	UART0_RX	ADC0.5
16	P1.2	I2C0_SDA	ADC0.10
18	5V		
20	3V3		

** STK LED0

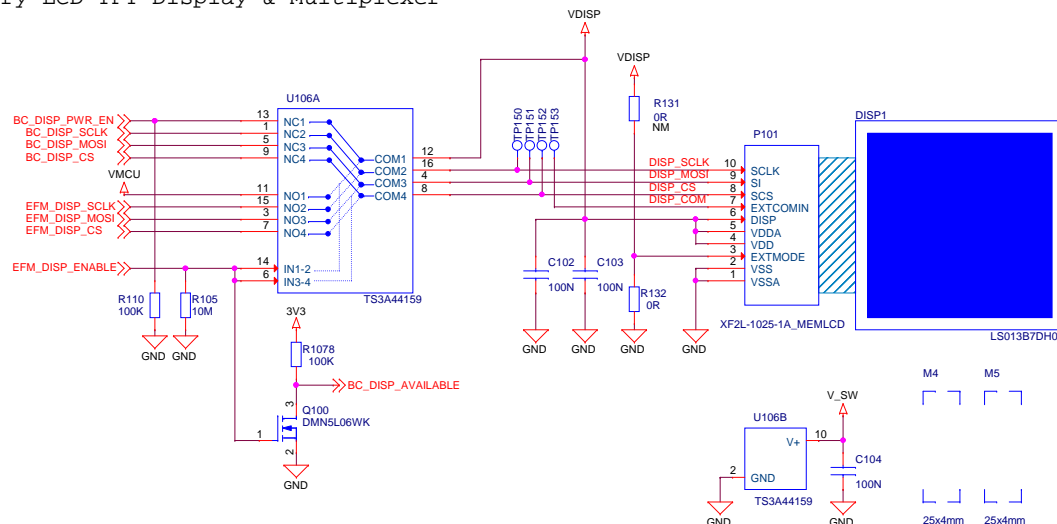
LED



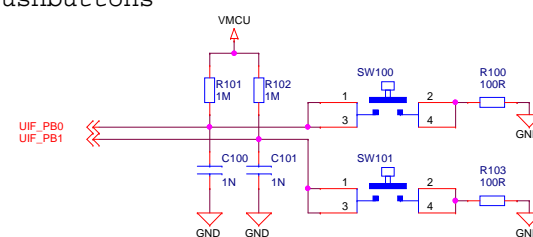
Capsense Rotor



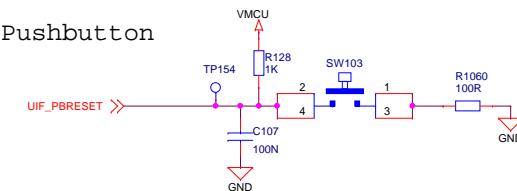
Memory LCD-TFT Display & Multiplexer



User pushbuttons



RESET Pushbutton

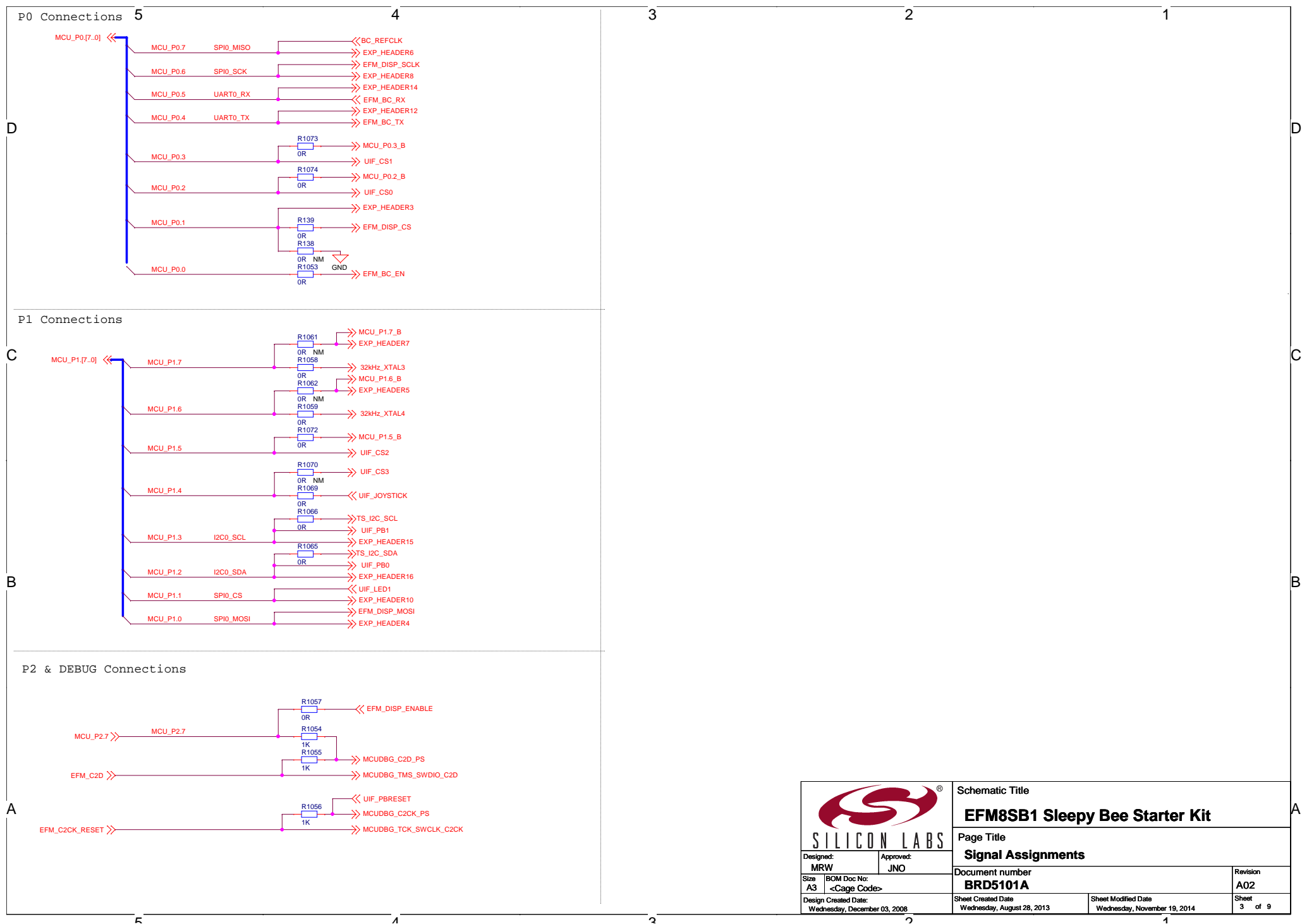



STK

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		EFM8SB1 Sleepy Bee Starter Kit	
Designed: MRW Size: A3 Design Created Date: Wednesday, December 03, 2008		Page Title	
		User Interfaces	
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A The EFM8 always controls ownership of the display using the EFM_DISP_ENABLE signal.

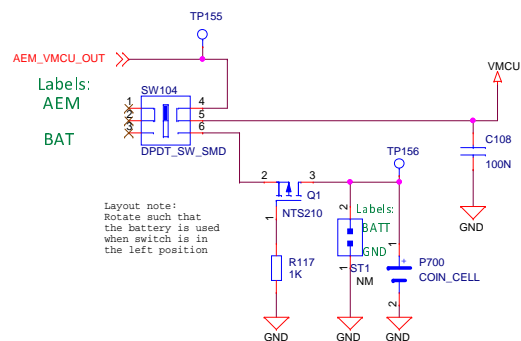
EFM_DISP_ENABLE	DISP_CTRL	VDISP
0	BC	BC_DISP_PWR_EN
1	EFM	VMCU



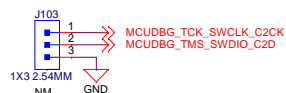
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Designed: MRW		Page Title	
Approved: JNO		Signal Assignments	
Size A3 BOM Doc No: <Cage Code>		Document number	
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Power Switch

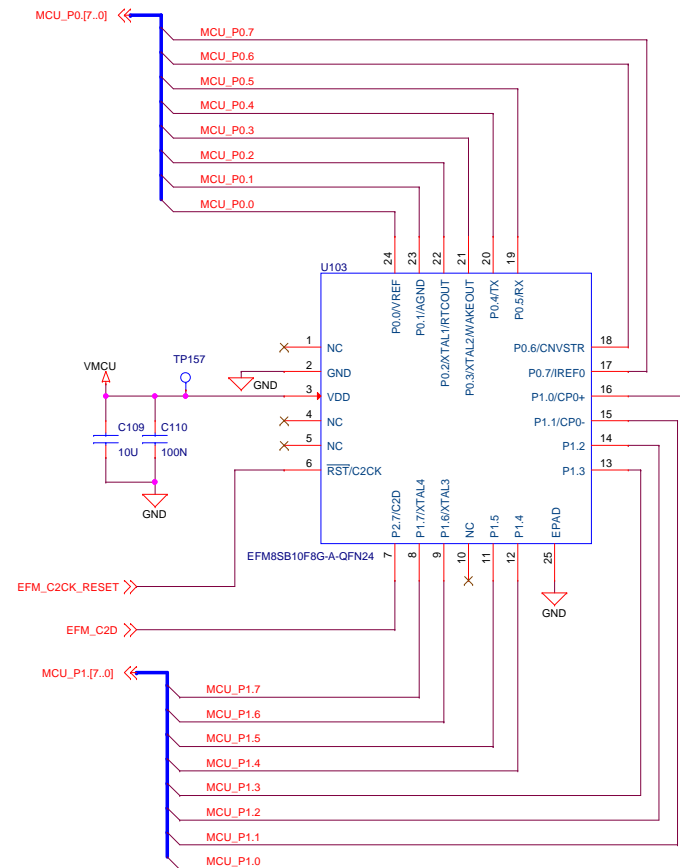
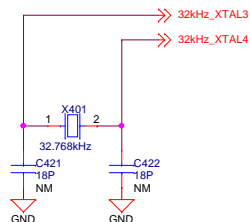
SWITCH POS	MODE DESCRIPTION
AEM	AEM Enabled, VMCU sourced from external 3.3V LDO powered by BC USB 5V supply
BAT	AEM Disabled, VMCU sourced from external coin-cell battery or external power supply




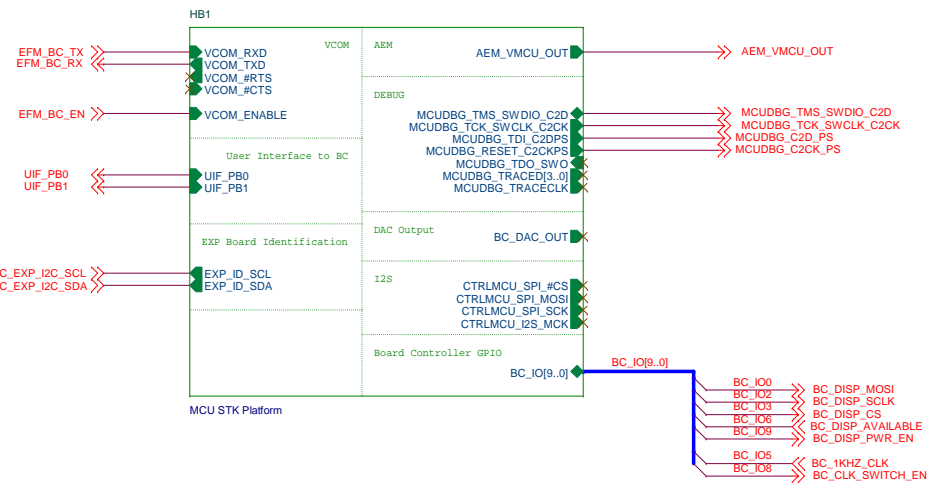
C2 Debug Header



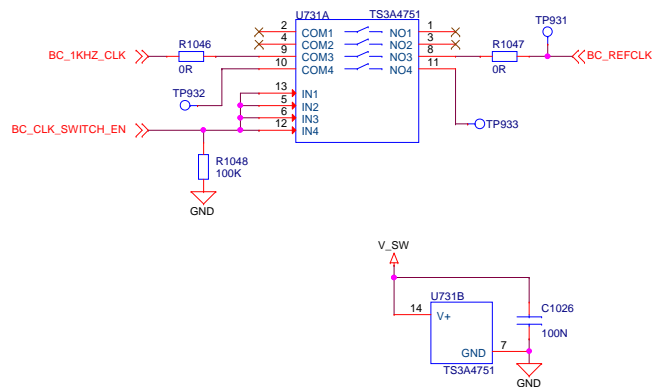
Low Frequency Clock




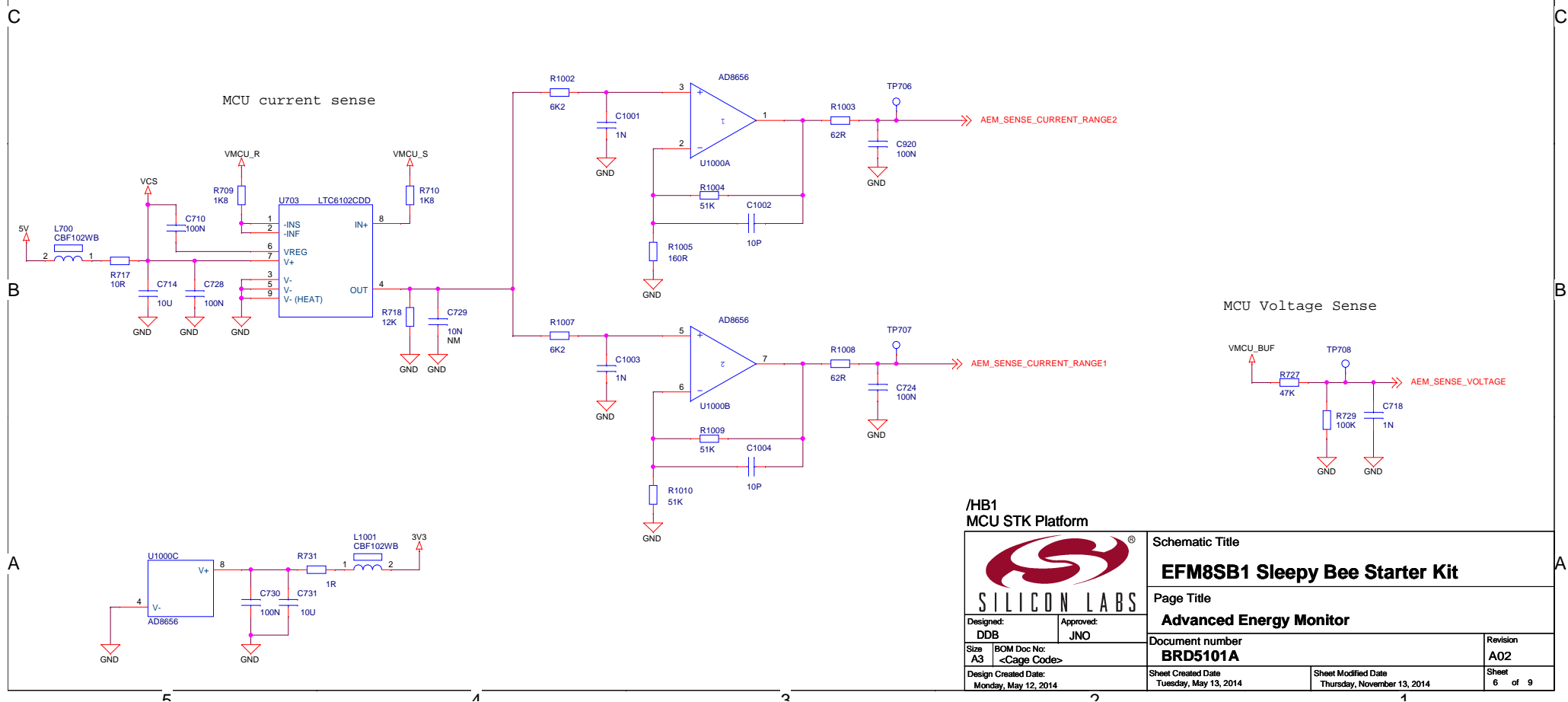
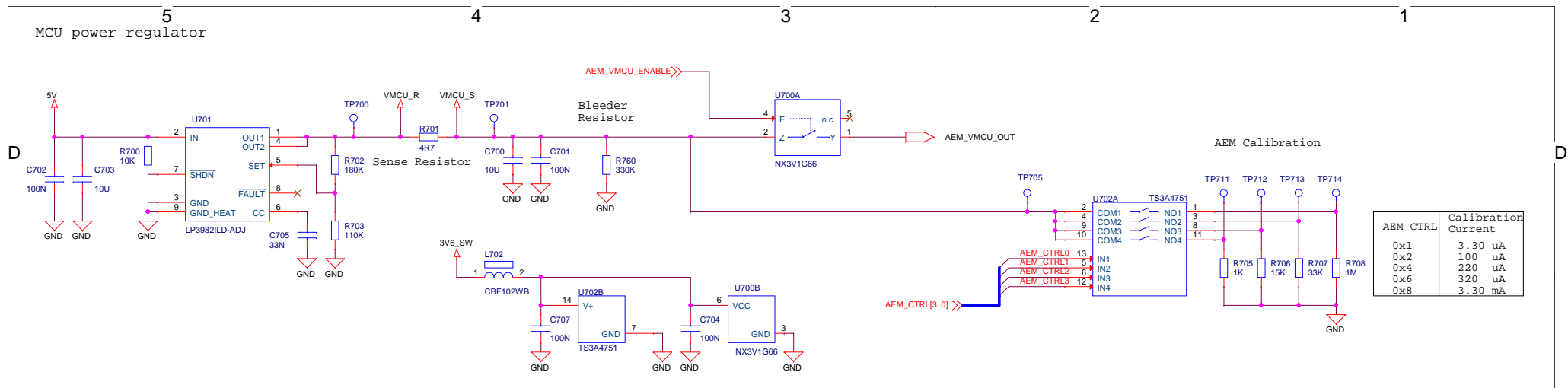
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Designed: MRW		Page Title	
Approved: JNO		EFM8 I/O	
Size A3	BOM Doc No: <Cage Code>	Document number BRD5101A	Revision A02
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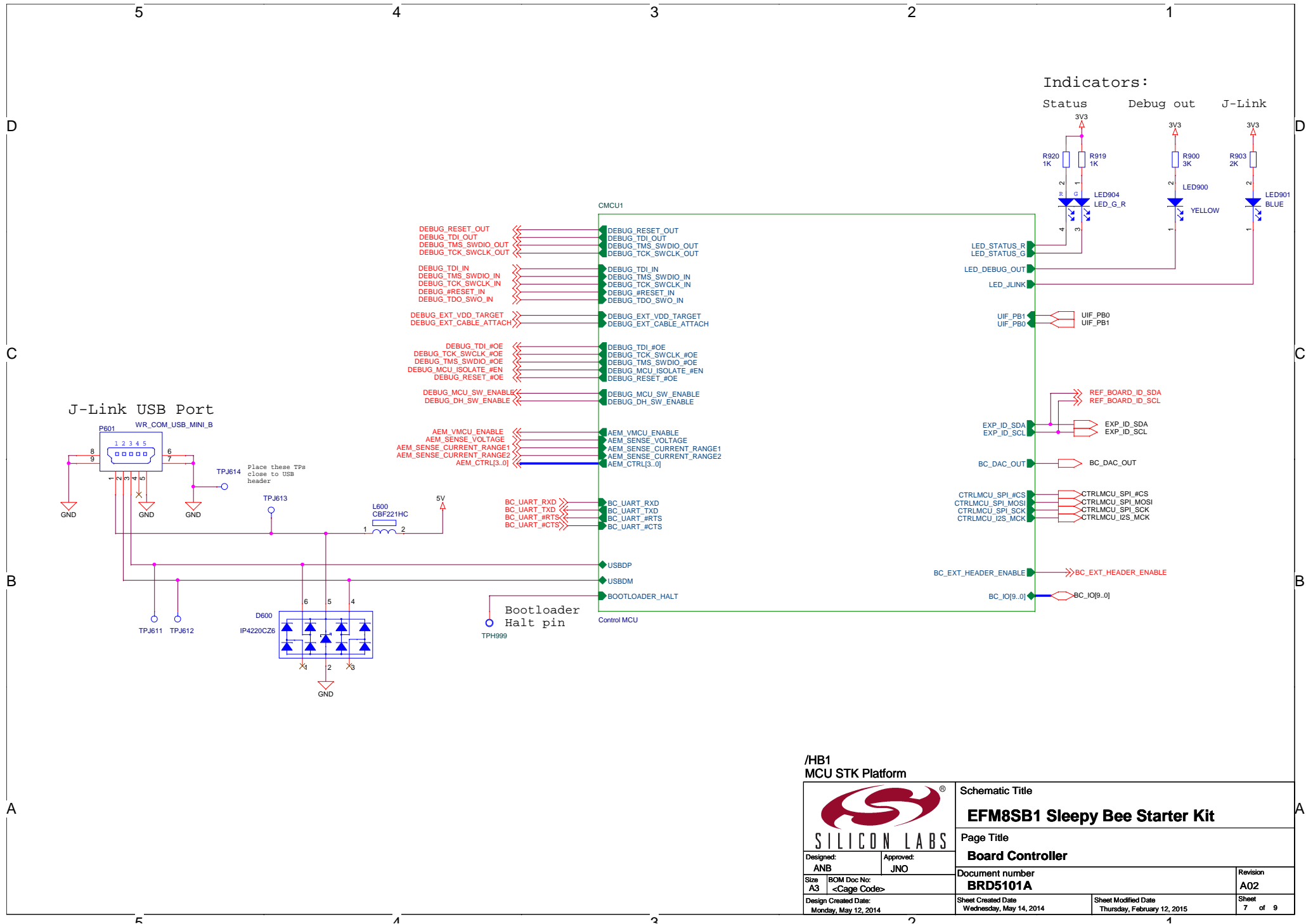


Analog Switch



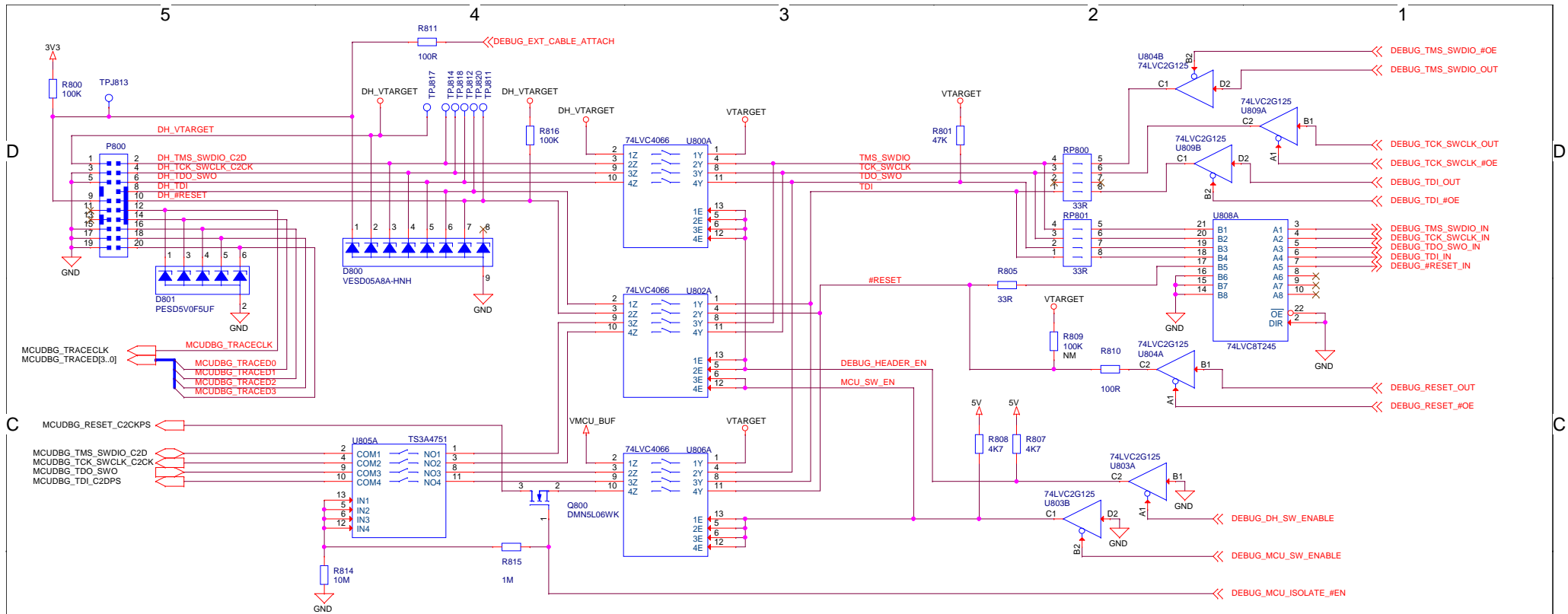
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Designed: MRW Size: A3 BOM Doc No: <Cage Code> Design Created Date: Wednesday, December 03, 2008		Page Title	
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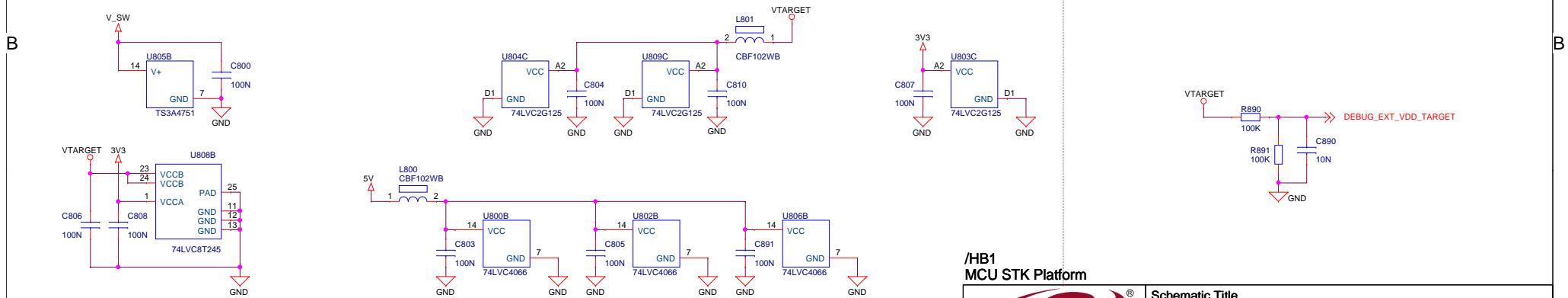


/HB1
MCU STK Platform

 SILICON LABS		Schematic Title	
		EFM8SB1 Sleepy Bee Starter Kit	
Designed: ANB		Page Title	
Size A3		Board Controller	
BOM Doc No: <Cage Code>		Document number	
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Power & Decoupling



Mode	DEBUG_MCU_SW_ENABLE	DEBUG_DH_SW_ENABLE	DEBUG_BUF_#OE	ISOLATE_#EN	DH_VTARGET	VTARGET
Debug Out	0	1	0	0	External voltage	External voltage
MCU Debug	1	0	0	1	Disconnected	VMCU
Debug In	1	1	1	1	VMCU	VMCU
Debug Off	1	1	1	0	-	-

/HB1
MCU STK Platform

		Schematic Title	
		EFM8SB1 Sleepy Bee Starter Kit	
Designed: DDB		Page Title	
Approved: JNO		Debug Interface	
Size A3		Document number	
<Cage Code>		BRD5101A	
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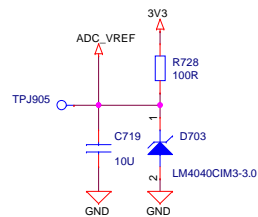


B

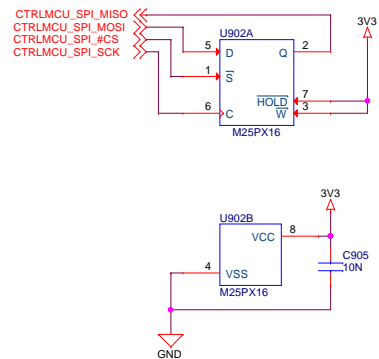
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A

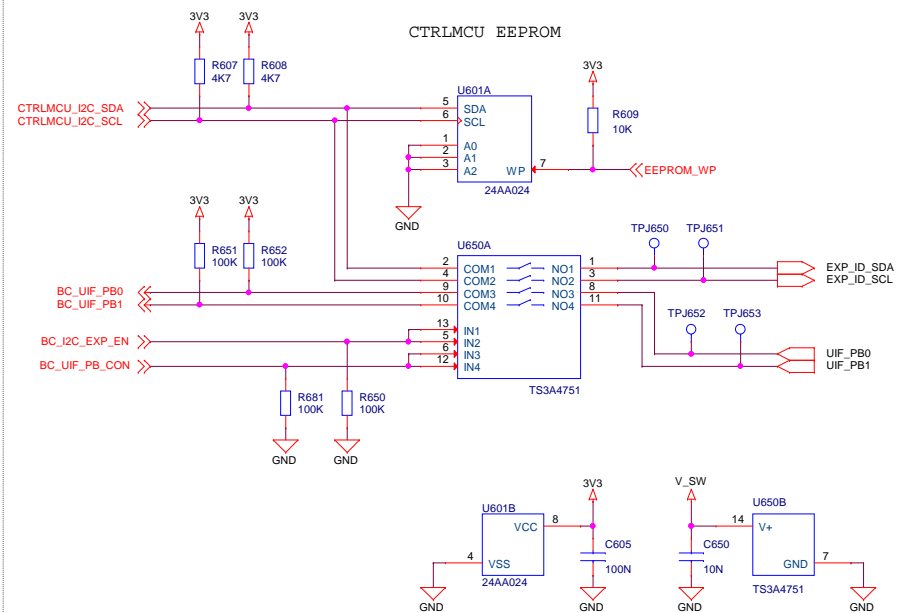
ADC reference voltage



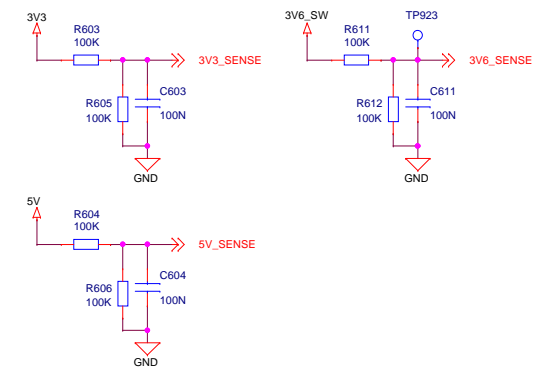
CTRLMCU SERIAL FLASH




CTRLMCU EEPROM



POWER SENSE



/HB1/CMCU1
Control MCU

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Designed: ANB		Page Title	
Approved: JNO		Control MCU Misc	
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