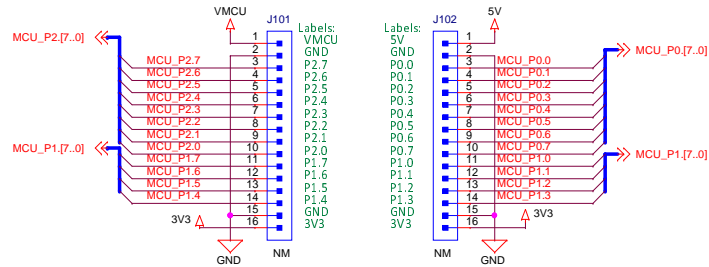


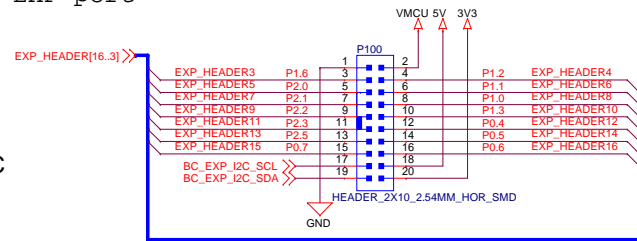




## Breakout Connections



## EXP port

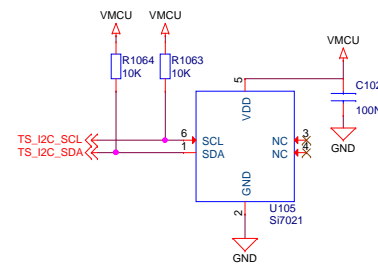


### EXP-Header Functionality

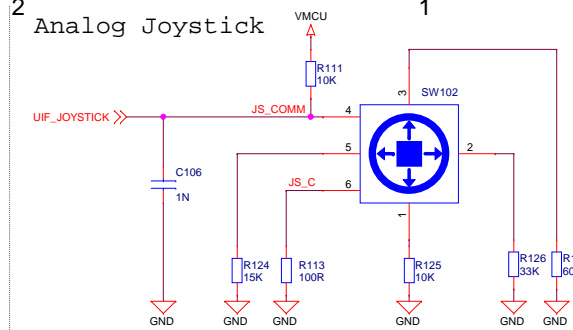
\*\* Indicates potential STK hardware conflicts

1	GND				
3	P1.6				
5	P2.0				
7	P2.1				
9	P2.2				
11	P2.3				
13	P2.5				
15	P0.7				
17					
19					
2	VMCU				
4	P1.2	SPI0_MOSI	CMPP.5/ADC0.10		
6	P1.1	SPI0_MISO	CMPP.4/ADC0.9		
8	P1.0	SPI0_SCK	CMPP.4/ADC0.8		
10	P1.3	SPI0_NSS	CMPP.5/ADC0.11		
12	P0.4	UART0_TX	CMPP.2/ADC0.4		
14	P0.5	UART0_RX	CMPP.2/ADC0.5		
16	P0.6	I2C0_SDA	CMPP.3/ADC0.6		
18	5V				
20	3V3				

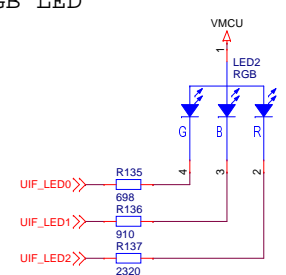
## Temperature & Relative Humidity Sensor



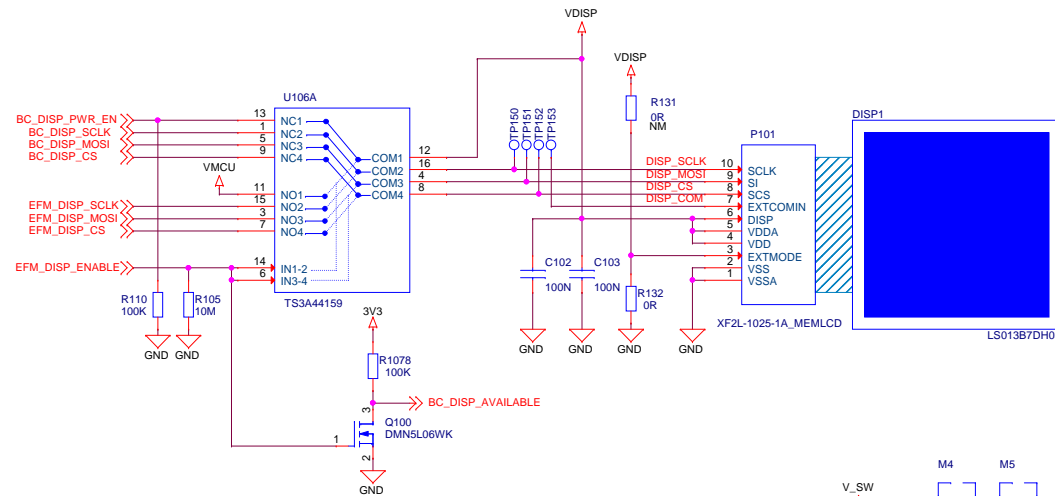
## Analog Joystick



## RGB LED



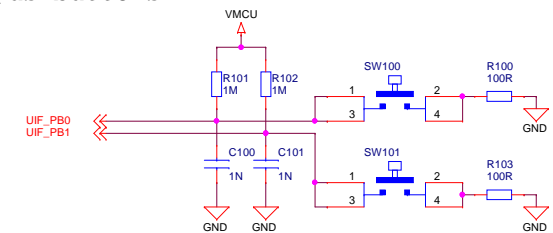
## Memory LCD-TFT Display & Multiplexer



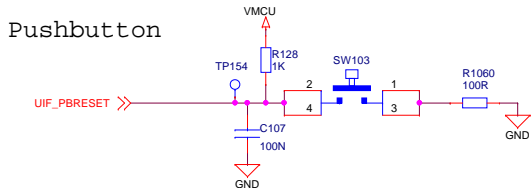
The EFM8 always controls ownership of the display using the EFM\_DISP\_ENABLE signal.

EFM_DISP_ENABLE	DISP_CTRL	VDISP
0	BC	BC_DISP_PWR_EN
1	EFM	VMCU

## User pushbuttons



## RESET Pushbutton



## STK

		Schematic Title	
		EFM8SB2 Sleepy Bee Starter Kit	
Designed: MRW		Page Title	
Size A3		User Interfaces	
BOM Doc No:		Document number	
Design Created Date:		BRD5100A	
Wednesday, December 03, 2008		Sheet Created Date	Revision
		Wednesday, August 28, 2013	A01
		Sheet Modified Date	Sheet
		Friday, November 21, 2014	2 of 10



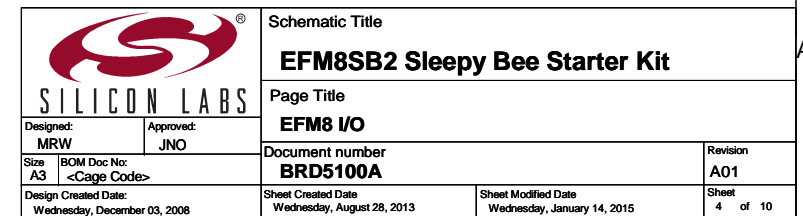




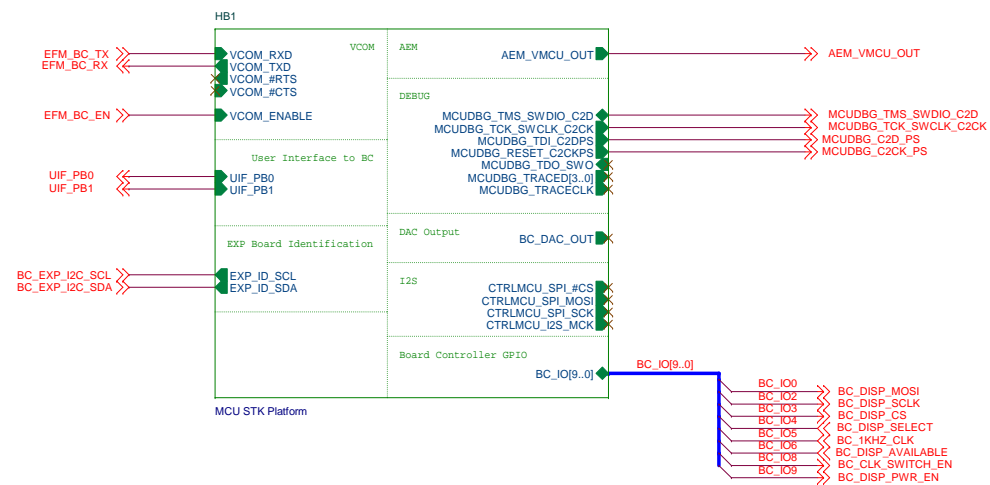
## D

C

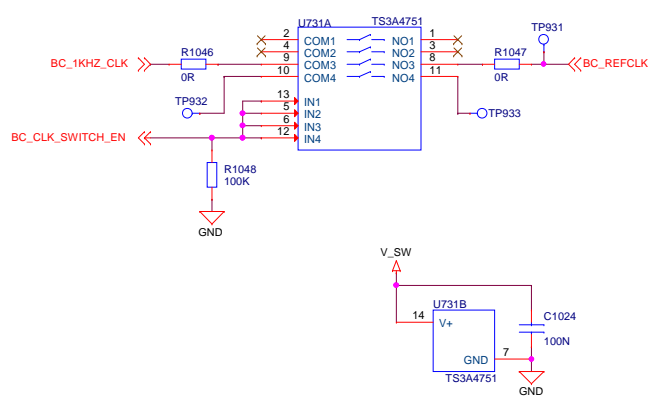
## A








Analog Switch

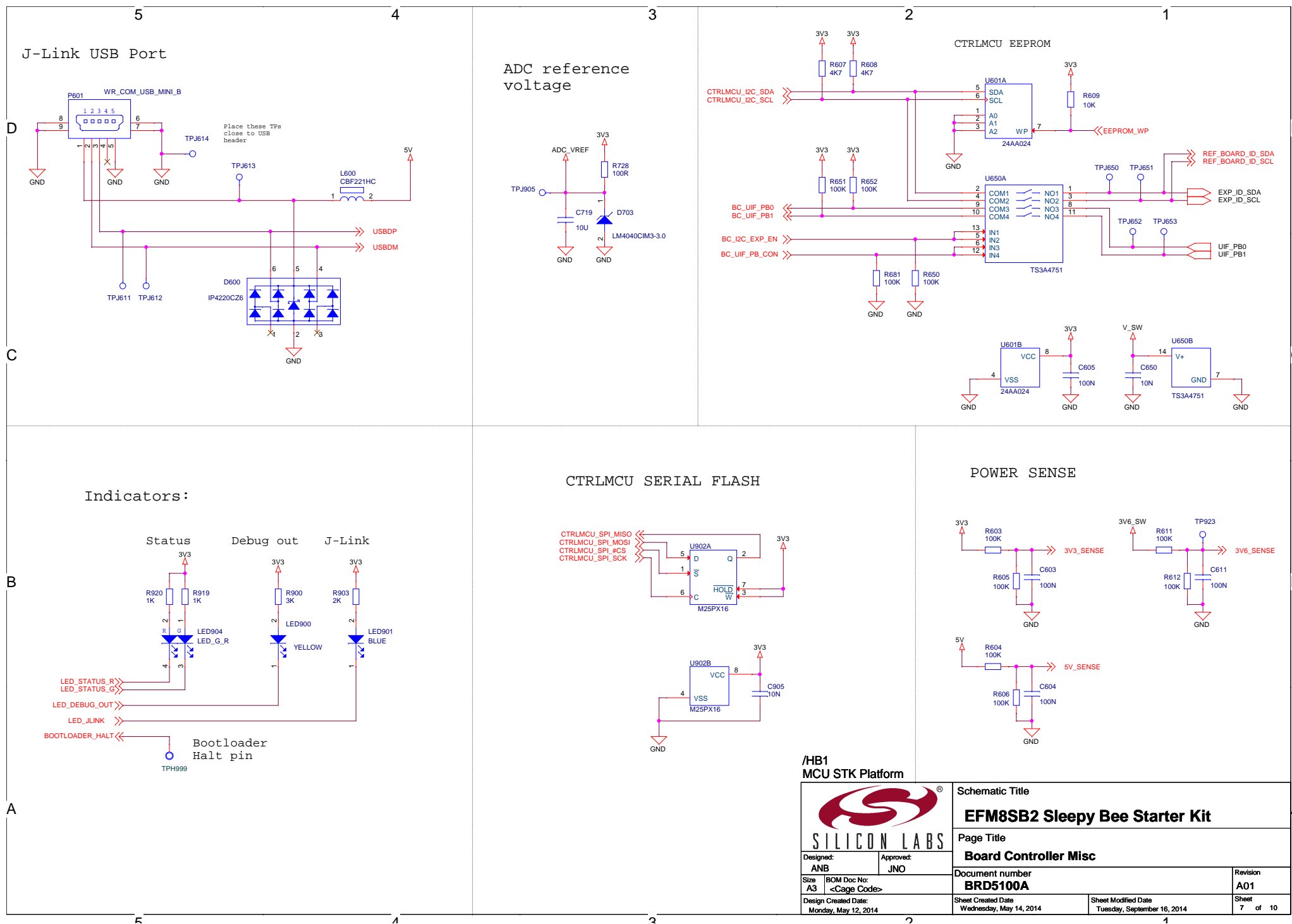


 SILICON LABS®		Schematic Title	
		EFM8SB2 Sleepy Bee Starter Kit	
Designed: MRW		Page Title	
Approved: JNO		Functional Blocks	
Size A3		Document number BRD5100A	
BOM Doc No: <Cage Code>		Revision A01	
Design Created Date: Wednesday, December 03, 2008		Sheet Created Date Thursday, May 15, 2014	Sheet Modified Date Friday, November 21, 2014
		Sheet 5 of 10	










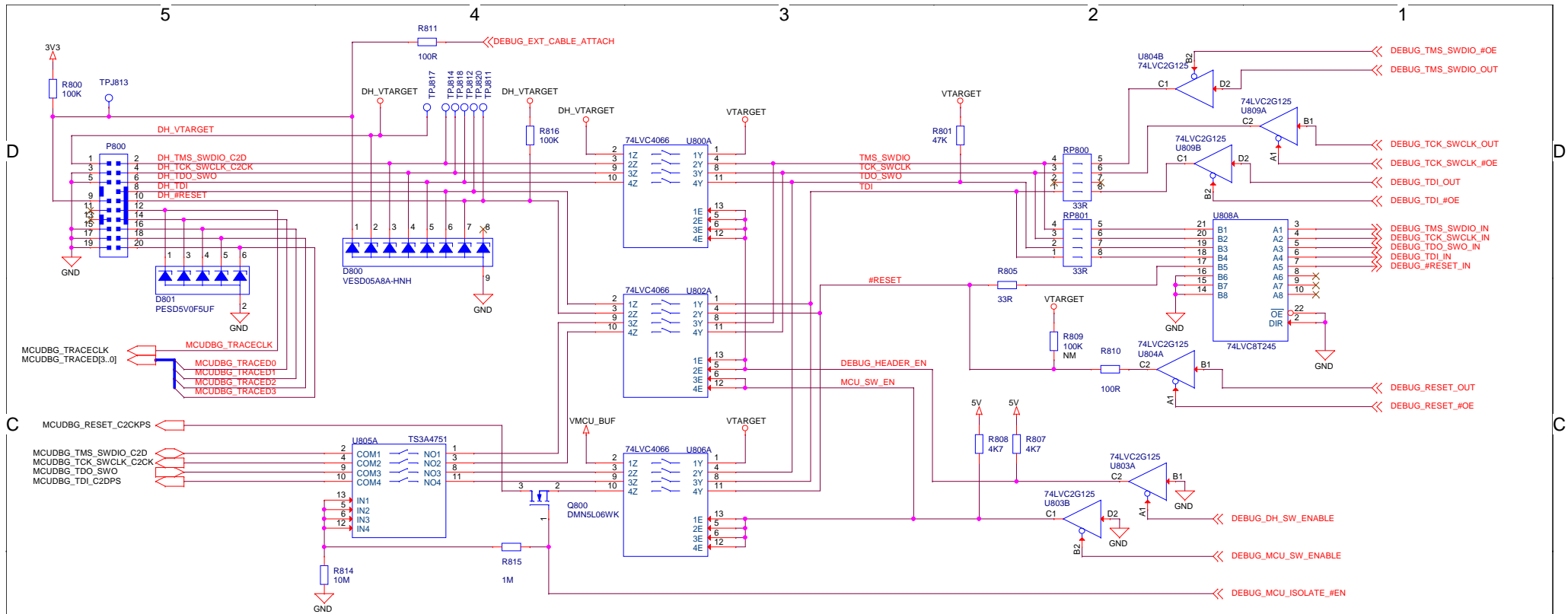
/HB1  
MCU STK Platform

 SILICON LABS®		Schematic Title	
		EFM8SB2 Sleepy Bee Starter Kit	
Designed: ANB		Page Title	
Approved: JNO		Board Controller Misc	
Size A3		Document number	
BOM Doc No: <Cage Code>		BRD5100A	
Design Created Date: Monday, May 12, 2014		Sheet Created Date Wednesday, May 14, 2014	Revision A01
		Sheet Modified Date Tuesday, September 16, 2014	Sheet 7 of 10

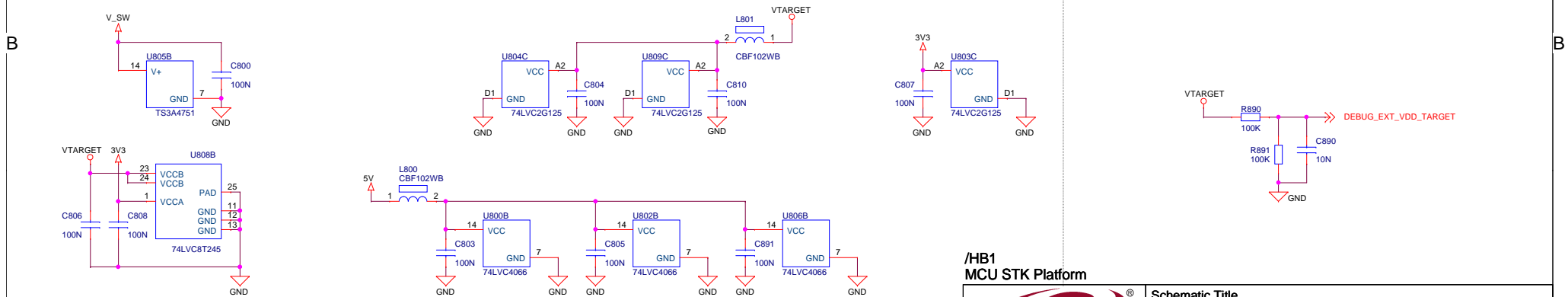








## Power & Decoupling



Mode	DEBUG_MCU_SW_ENABLE	DEBUG_DH_SW_ENABLE	DEBUG_BUF_#OE	ISOLATE_#EN	DH_VTARGET	VTARGET
Debug Out	0	1	0	0	External voltage	External voltage
MCU Debug	1	0	0	1	Disconnected	VMCU
Debug In	1	1	1	1	VMCU	VMCU
Debug Off	1	1	1	0	-	-

/HB1  
MCU STK Platform

		Schematic Title	
		<b>EFM8SB2 Sleepy Bee Starter Kit</b>	
Designed: DDB		Page Title	
Approved: JNO		<b>Debug Interface</b>	
Size: A3	BOM Doc No: <Cage Code>	Document number	
Design Created Date: Monday, May 12, 2014		<b>BRD5100A</b>	
Sheet Created Date: Monday, May 12, 2014		Sheet Modified Date: Wednesday, October 22, 2014	Revision: A01
Sheet 9 of 10			



## D



## B



J-Link USB Cable	PMOS State	NMOS State	V_SW	VMCU_SENSE
Connected	Off	ON	3.6V	VMCU
Disconnected	ON	OFF	VMCU	Isolated



SILICON LABS

Sheet Created Date Monday, May 12, 2014	Sheet Modified Date Tuesday, September 16, 2014	Sheet 10 of 10
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Revision	A01
Sheet	10 of 10