



EFM8SB2 Sleepy Bee STK

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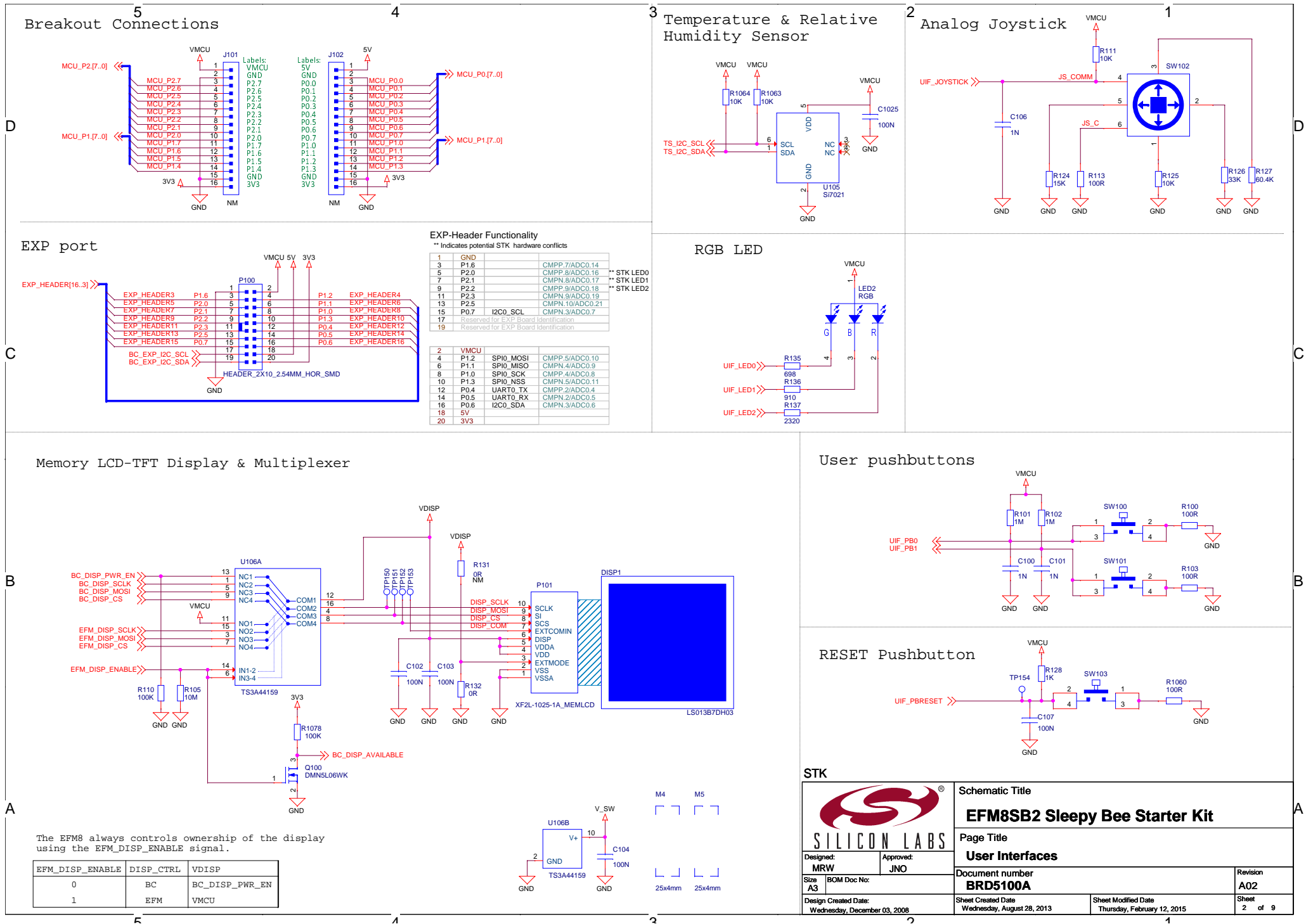
Revision History

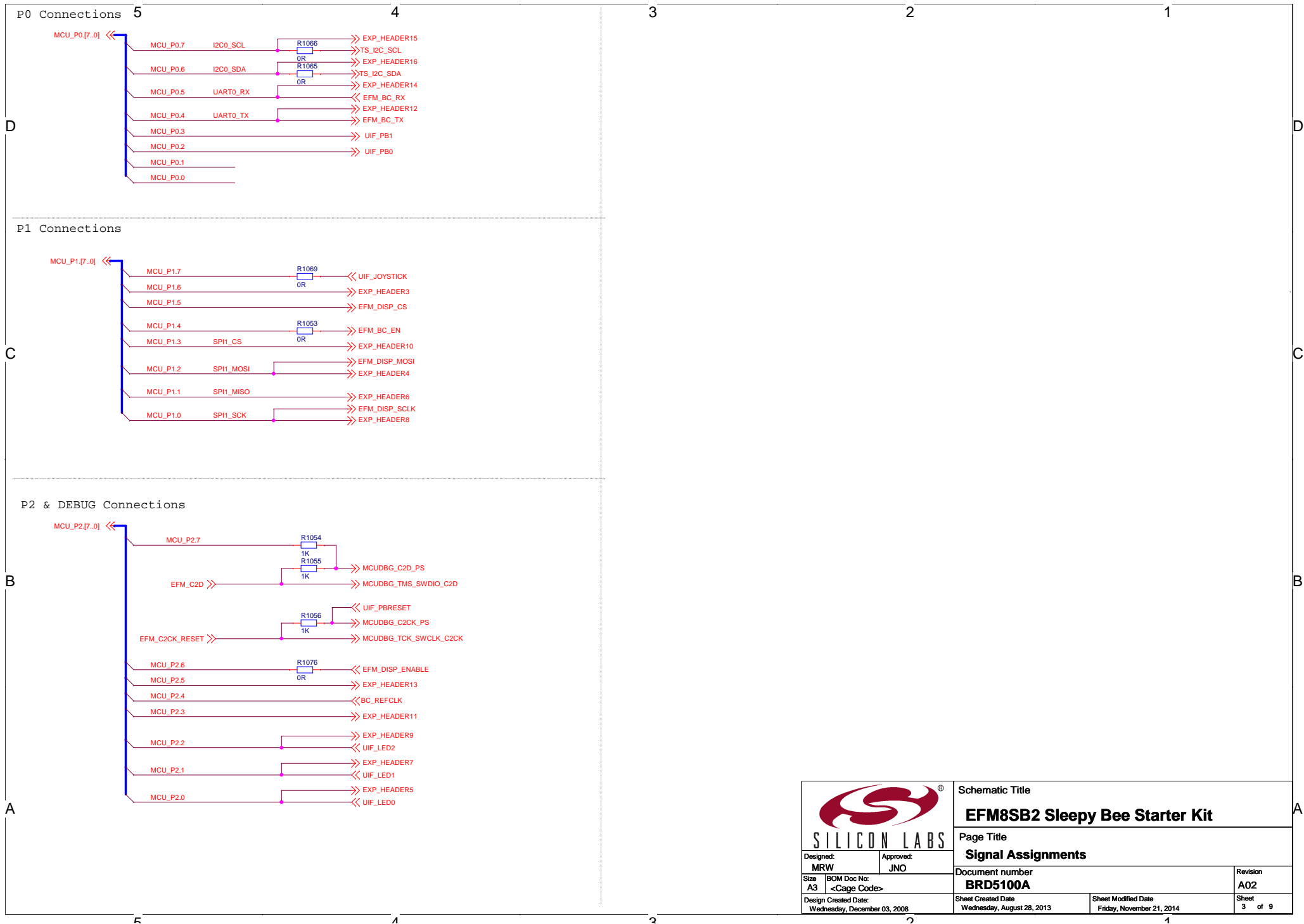
Rev.	Description
A00	Initial release for production.
A01	Removed ST1 and J103 from the BOM.
A02	Updated PCB revision.




STK

		Schematic Title	
		EFM8SB2 Sleepy Bee Starter Kit	
Page Title		Title Page	
Designed: MRW	Approved: JNO	Document number BRD5100A	Revision A02
Size A3	BOM Doc No:	Sheet Created Date Thursday, May 15, 2014	Sheet Modified Date Monday, March 23, 2015
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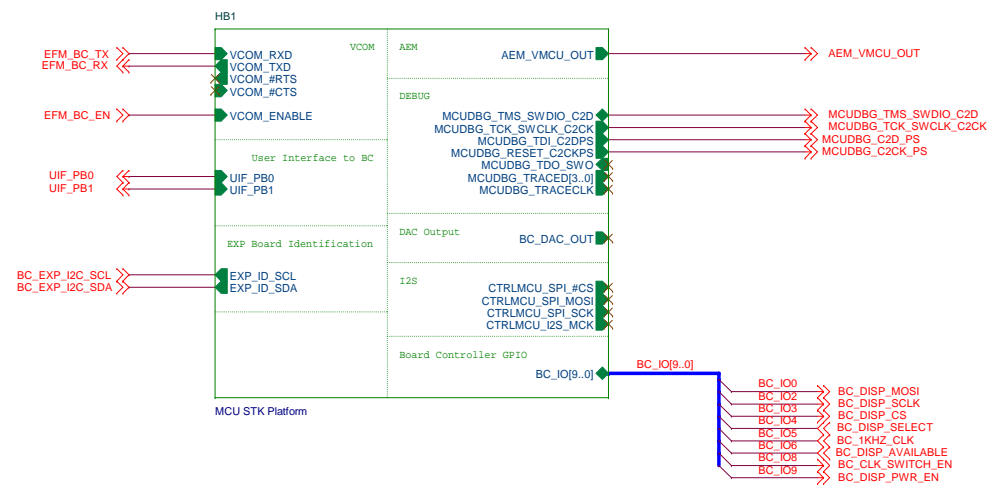
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Design Created Date: Wednesday, December 03, 2008		Sheet Created Date: Wednesday, August 28, 2013		Document number
		Sheet Modified Date: Friday, November 21, 2014		Revision
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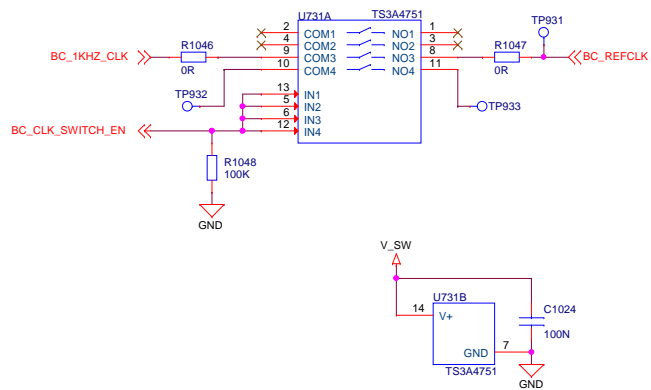
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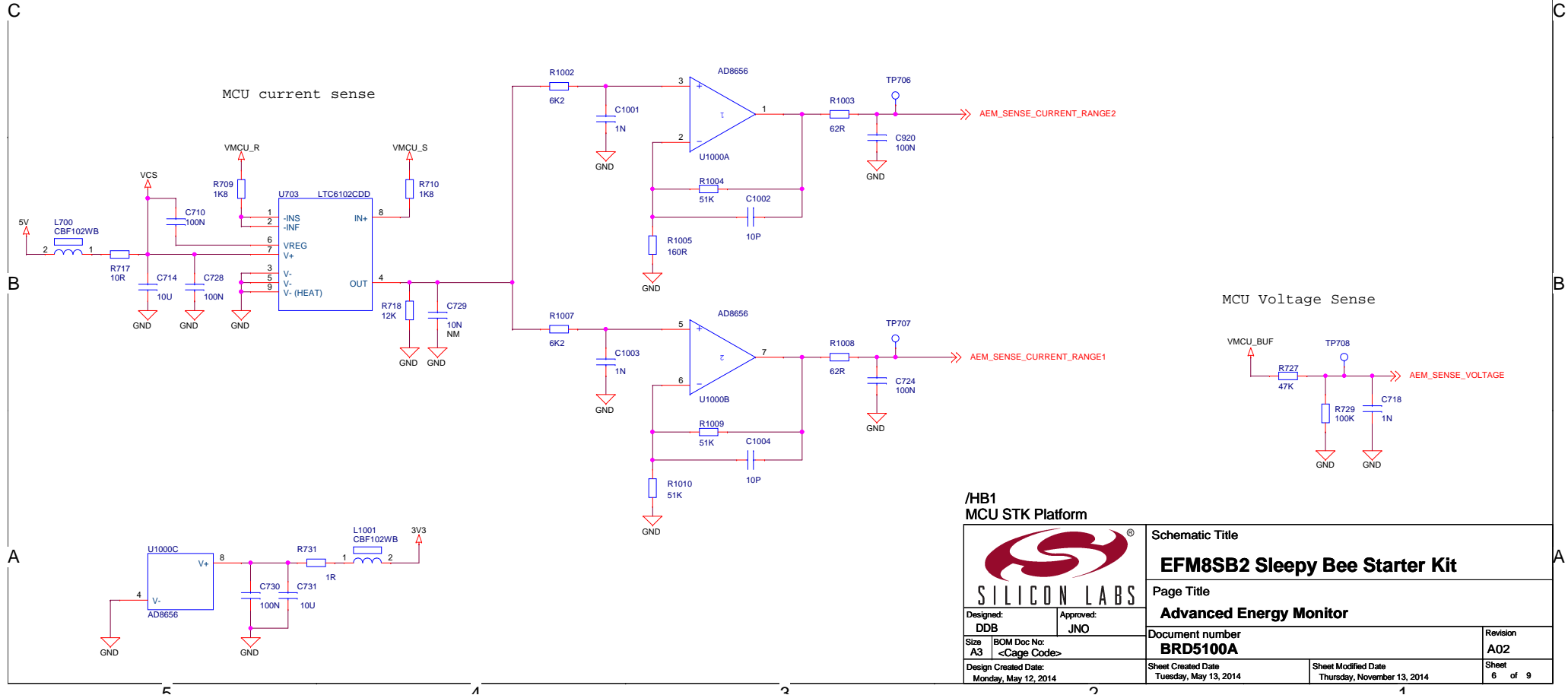
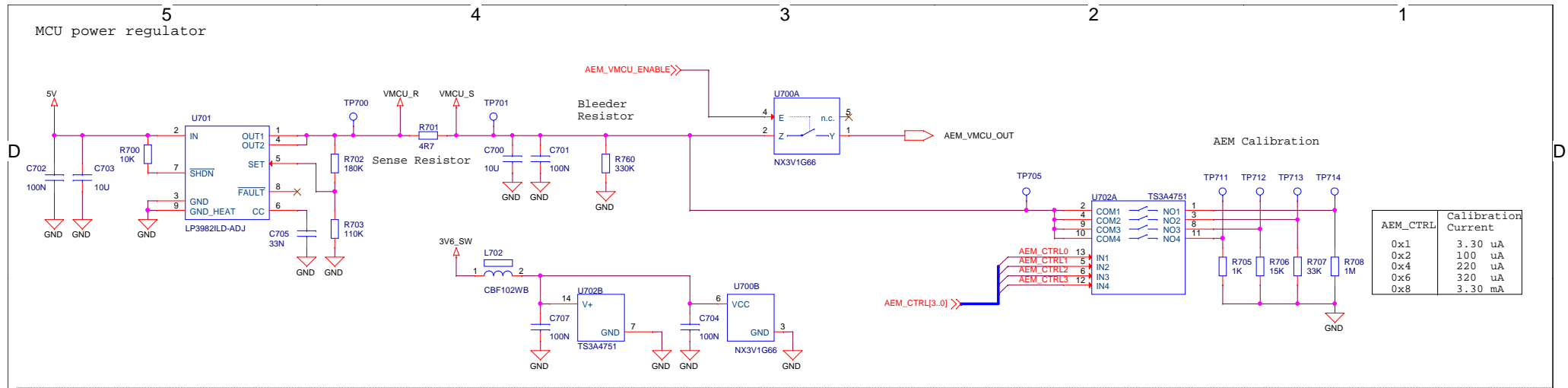


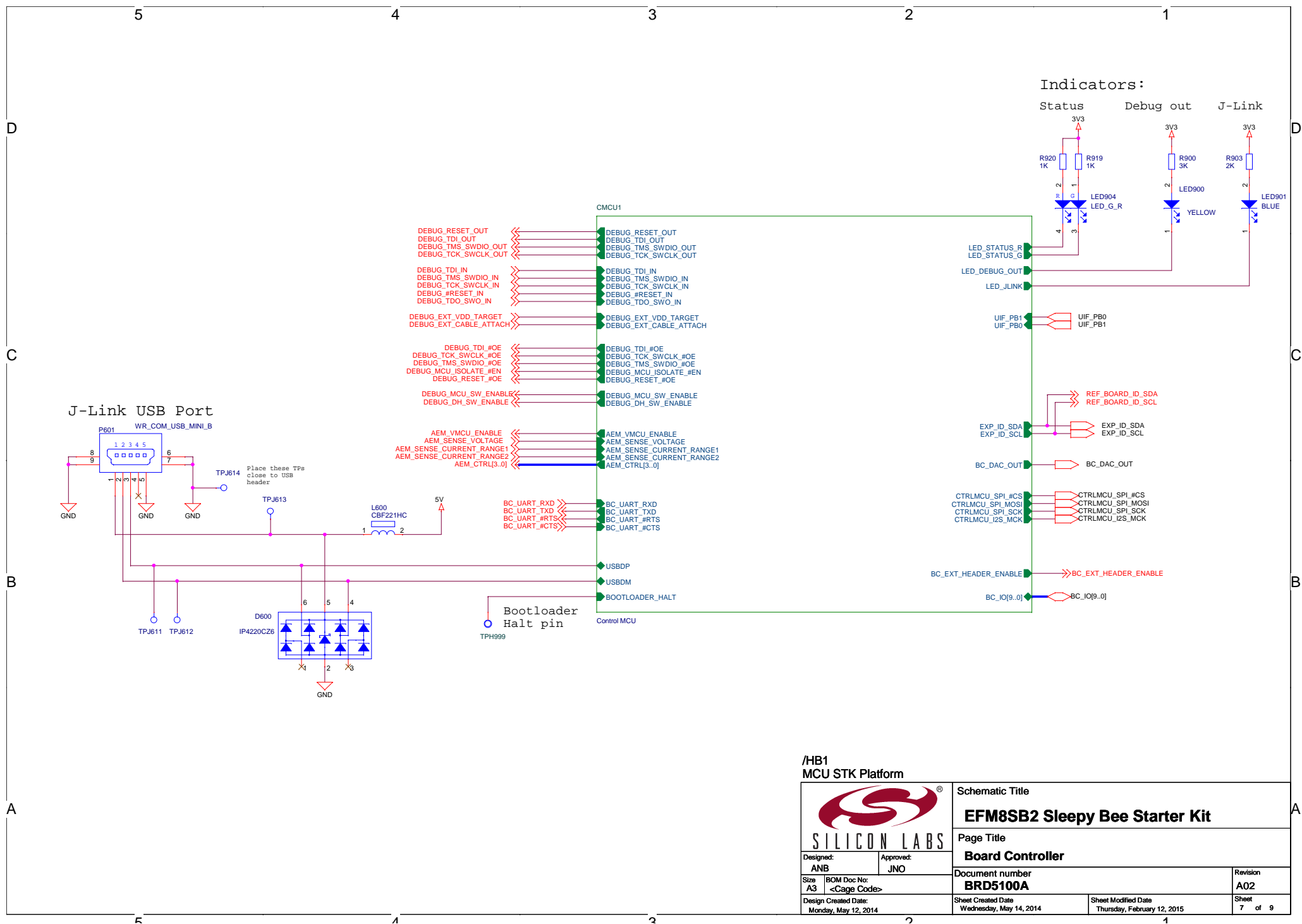


Analog Switch




 SILICON LABS®		Schematic Title	
		EFM8SB2 Sleepy Bee Starter Kit	
Designed: MRW		Page Title	
Approved: JNO		STK Common Platform	
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/HB1
MCU STK Platform

 SILICON LABS		Schematic Title	
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BOM Doc No: <Cage Code>		Document number	
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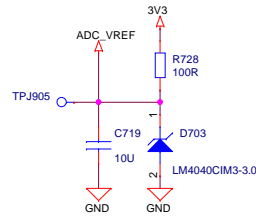


J-Link USB Cable	PMOS State	NMOS State	V_SW	VMCU_SENSE
Connected	Off	ON	3.6V	VMCU
Disconnected	ON	OFF	VMCU	Isolated

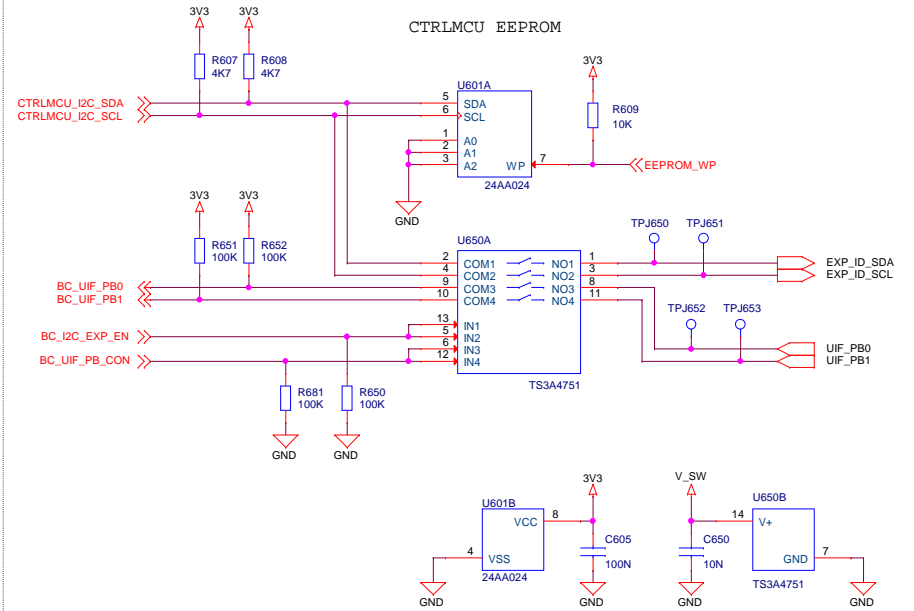
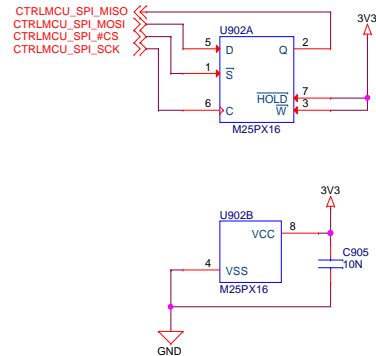


Schematic Title		
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Page Title		
Power & Misc		
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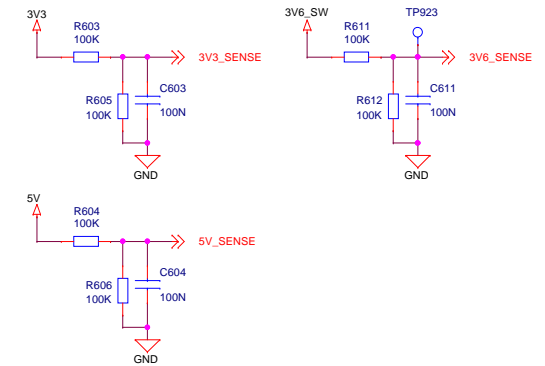
ADC reference voltage




CTRLMCU SERIAL FLASH



POWER SENSE



/HB1/CMCU1
Control MCU

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