*** PCB SPECIFICATION FOR BARE BOARD MANUFACTURING ***

PRODUCT OWNER : Silicon Labs
DOCUMENT/BOARD : '.BoardName'

DATE : 8/12/2020
REVISION : '.BoardRevision'

PREPARED BY : Allan
BOARDS pr PANEL : 12 (4 x 3)
PANEL SIZE : 210.2 x 205.4 mm
BOARD SIZE : 30.0 x 45.0 mm
BOARD THICKNESS : 1.6 mm +/-10%
NO OF LAYERS : 4
MATERIAL(S) : Glass Epoxy FR-4, NEMA Class 2, UL 94V-0, Tg min 150 C
Materials in compliance with the RoHS and WEEE directives
MARKINGS : Logo, Week/Year, UL (ON SECONDARY SIDE (BOT))
(Avoid areas reserved for DataMatrix, Barcodes or Lables)
All PCB manufacturerí»s markings (Logo, Week/Year, UL)
shall be put in the PCB frame. No marking on the boards
is allowed
QUALITY REQ. : IPC-A-600 (current revisions) Class 2, and IPC specifications
refered to by IPC-A-600
GENERAL REQ. : - Copper must not be added or removed from inside the board
outline(s), without written consent/approval.
Use the balancing of the panel that comes with the
Gerber files (without alterations)
If applicable, the following requirements are valid:
- If Build-Up (Stack-Up) is specified, follow Build-Up,
otherwise use (board manufacturer) standard Build-Up.
- Break-away areas may be used for patterns, holes etc.
by manufacturer for QA purposes.
- If V-CUT, use angle 30 +/- 5 degrees.
V-CUT minimum remaining thickness 0.5 +/- 0.1 mm.
Use of V-CUT test pads is allowed.
- Inner radius (contour/outline) 1.2 mm, unless stated
otherwise.
COPPER THK. : SEE BUILD-UP
COPPER PASSIV. : ENIG to meet IPC-4552 requirements (current revision)
(Electroless Nickel/Immersion Gold)
RESIST MASK : Solder Mask Color: BLACK (NB! NON-STANDARD)
Photo Polymer Wet film
to IPC-SM-840 Class T requirements (current revision)
Thickness minimum 8 um, maximum 20 um
VIA HOLES : PLUGGED/FILLED, IPC-4761 (current revision) Type IV-b
Plugged and Covered Both Sides, Low CTE Plugging Paste
If Type IV-b is not available as a process, then Type IV-a
for the Top Side, and Overprinted (Tented) Bot Side is OK
LEGEND/SILKSCR. : WHITE, BOTH SIDES (TOP + BOT)
CONTROLLED IMP : Design has Controlled impedances. FOLLOW BUILD-UP STRICTLY!
Unless explicitly stated otherwise, controlled impedance
has been designed into the board. Use of test strip is
hence normally not required.

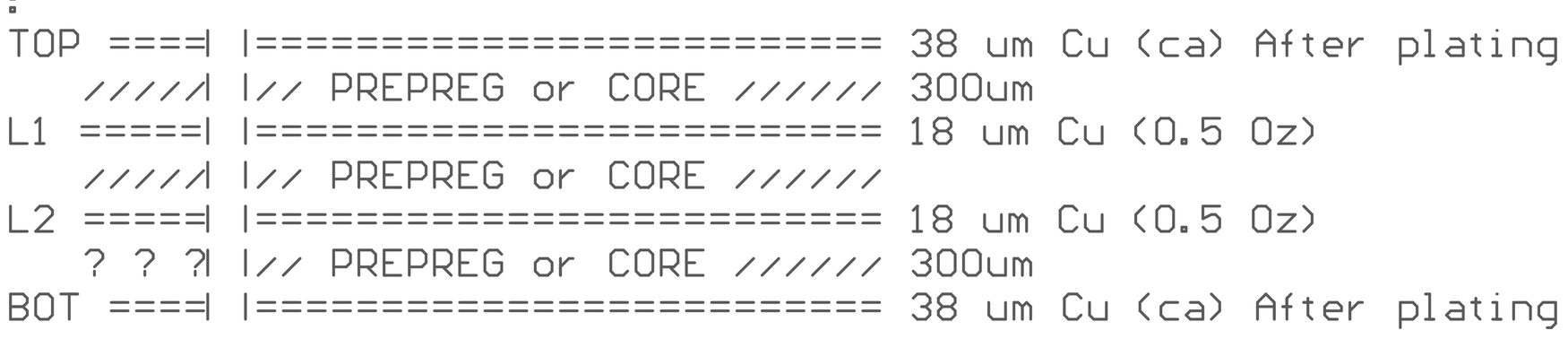
NOMINAL VALUES for Width, Spacing and VIA Diameter:

Cu TRACK(TRACE) :	Minimum conductor width	: 0.10 mm (4 mils)
Cu TRACK(TRACE) :	Minimum conductor spacing	: 0.10 mm (4 mils)
MINIMUM VIA :	Minimum via pad diameter	: 0.51 mm (20 mils)
	Minimum via hole diameter	: 0.25 mm (9.8 mils)

Min via hole may have more than one pad diameter.

(SPECIFICATION CONTINUED ON NEXT PAGE)

BUILD UP :



*)
The distance between Top-L1 and Bottom-L2 should be
as close to 300 um as possible!

**)
Select Center Prepreg thickness in order to reach specified
board thickness

TEST : 100% Electrical Test
Optical test, AOI (with automatic scanner)
Visual inspection
(Generate netlist from Gerber and Drill files)

Avoid use of 2125 Prepreg

If NB! is used in this specification, it means:
abbreviation for nota bene!, a Latin expression meaning
note well!

NC DRILL - HOLE INFORMATION:
WARNING : Drill dimensions must be taken from the Excellon (.DRL) file(s), and
the drill report file(s) (.DRR).
NON-PLATED holes may have a small center marker in the Gerber files.
Under no circumstance must these Gerber flashes be mistaken for the
hole drill dimensions!
The drill data may contain slots (in a separate file).
Dimensions for the finished board (after plating).
Tolerances +/- 0.1 mm, unless specified differently.
Via Holes +0.05 mm/-Via Size, unless specified differently.

