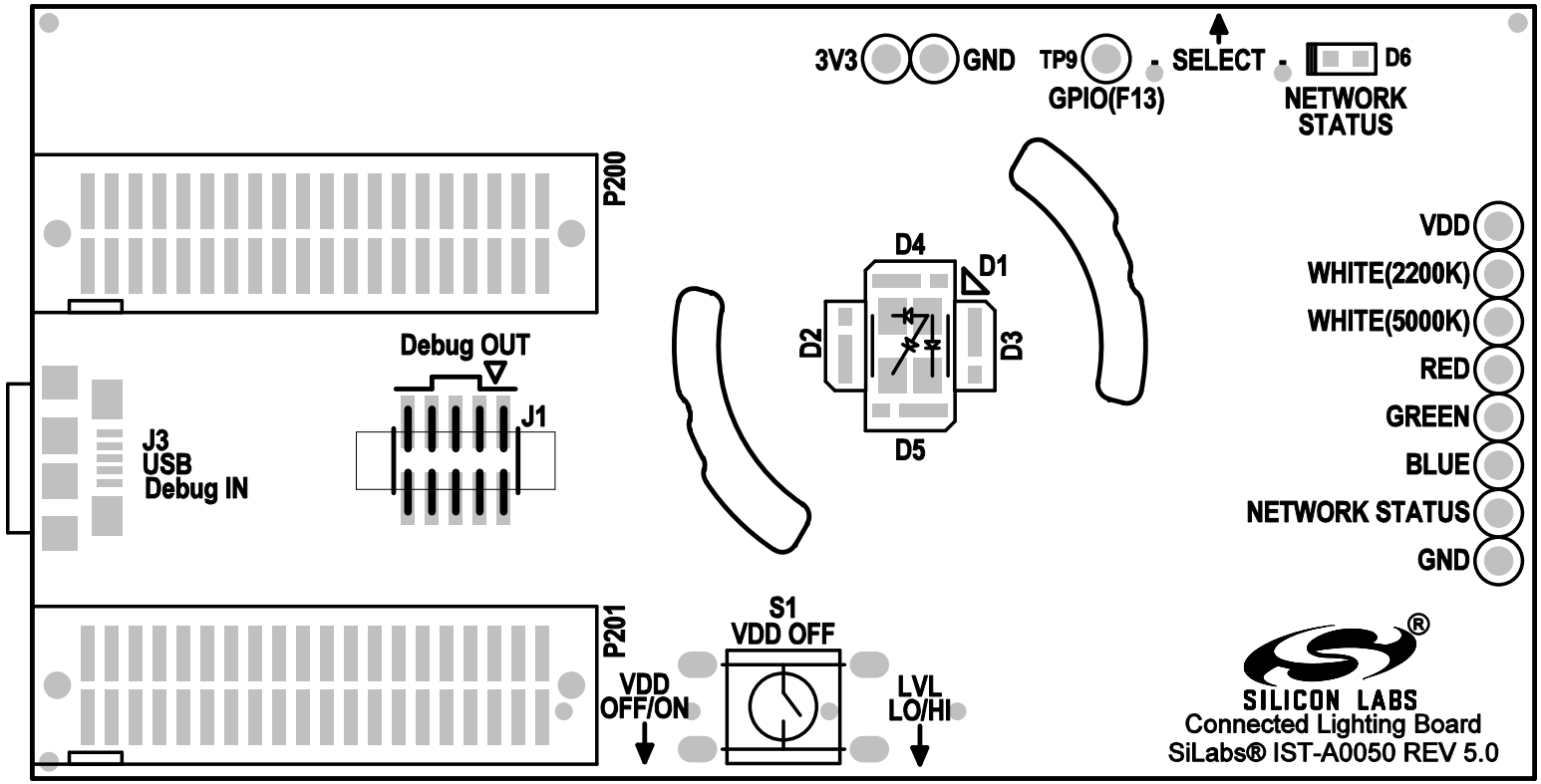
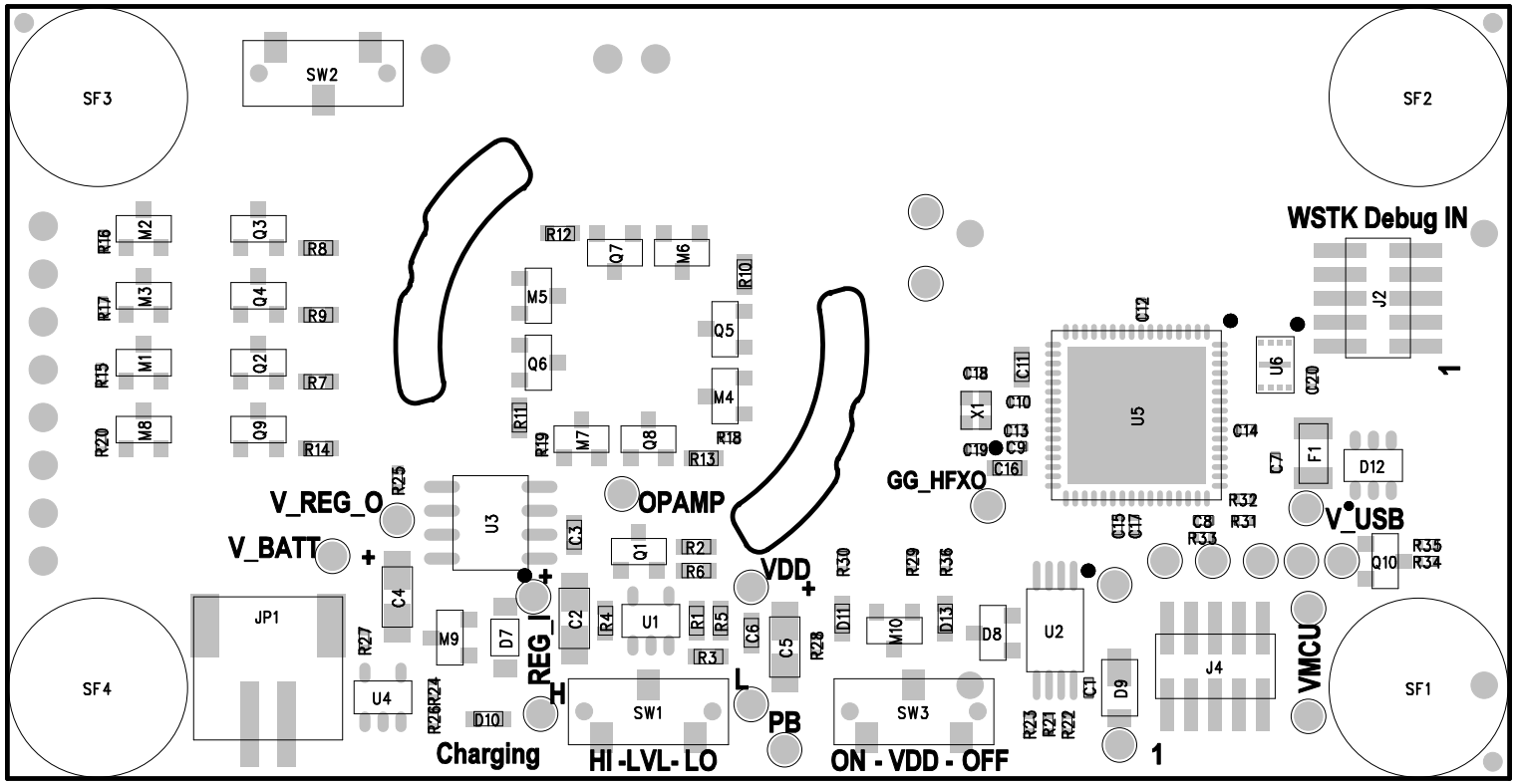
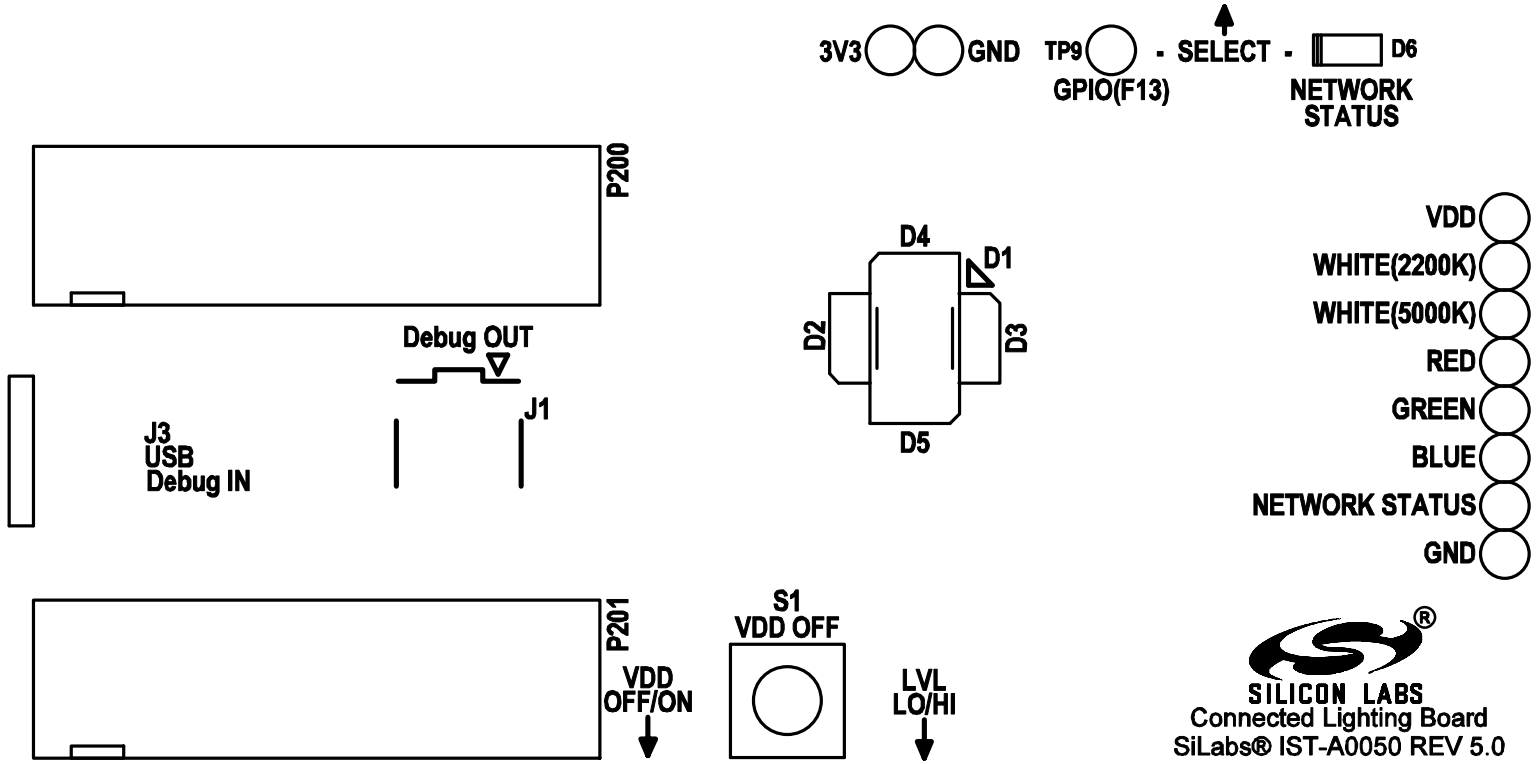
PRIMARY SILKSCREEN



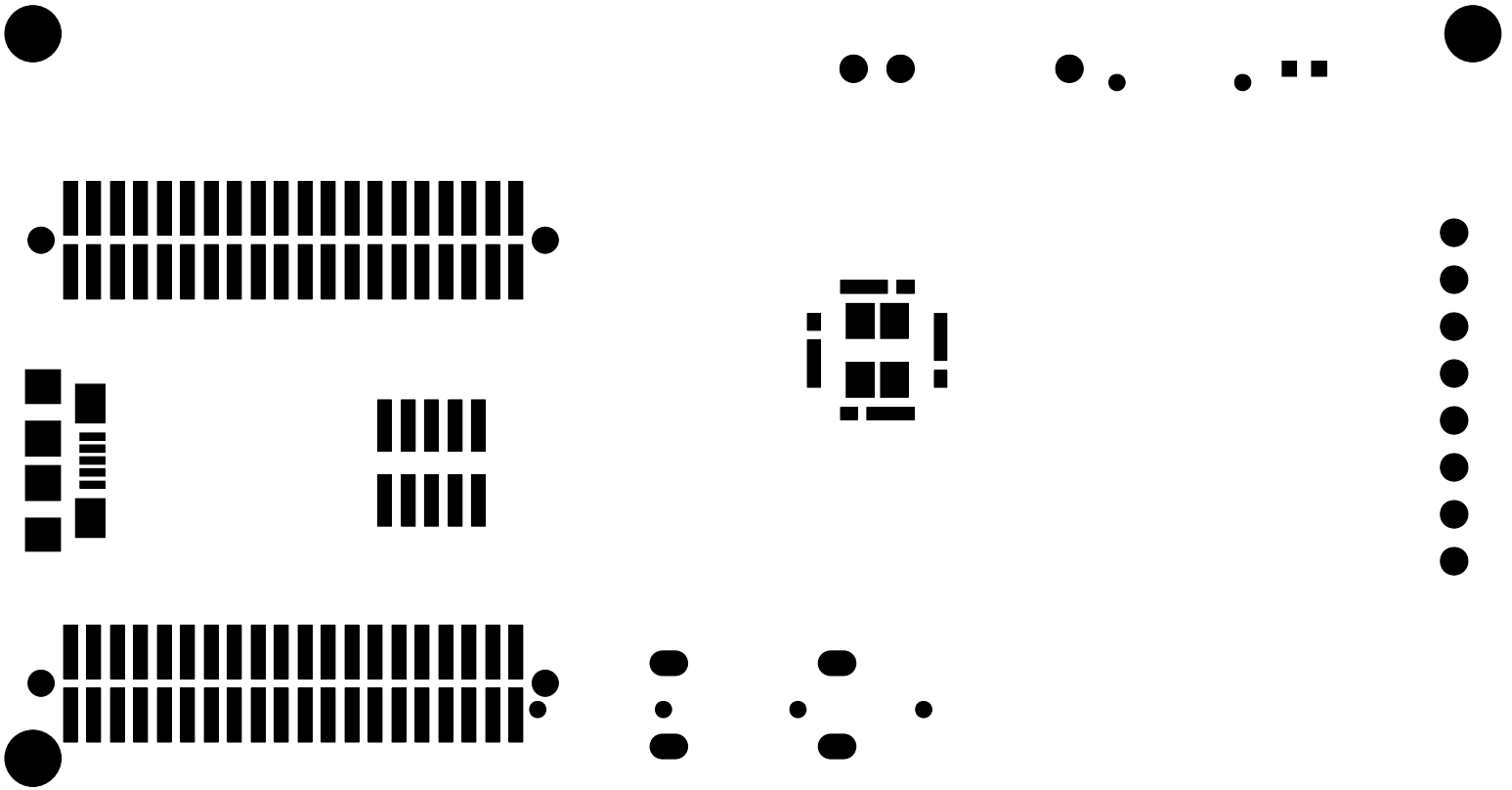
SECONDARY SILKSCREEN



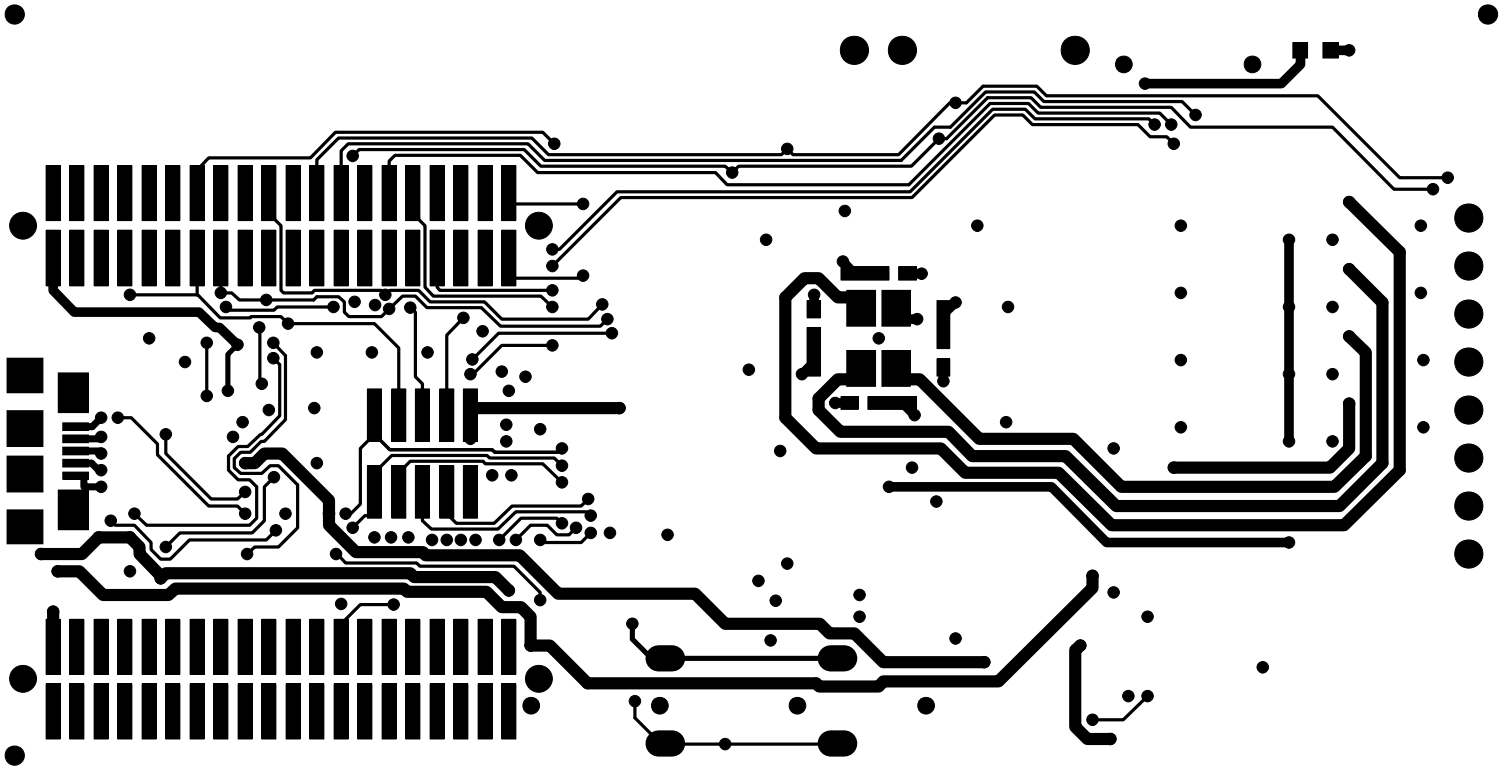
PRIMARY SILKSCREEN



PRIMARY SOLDER MASK

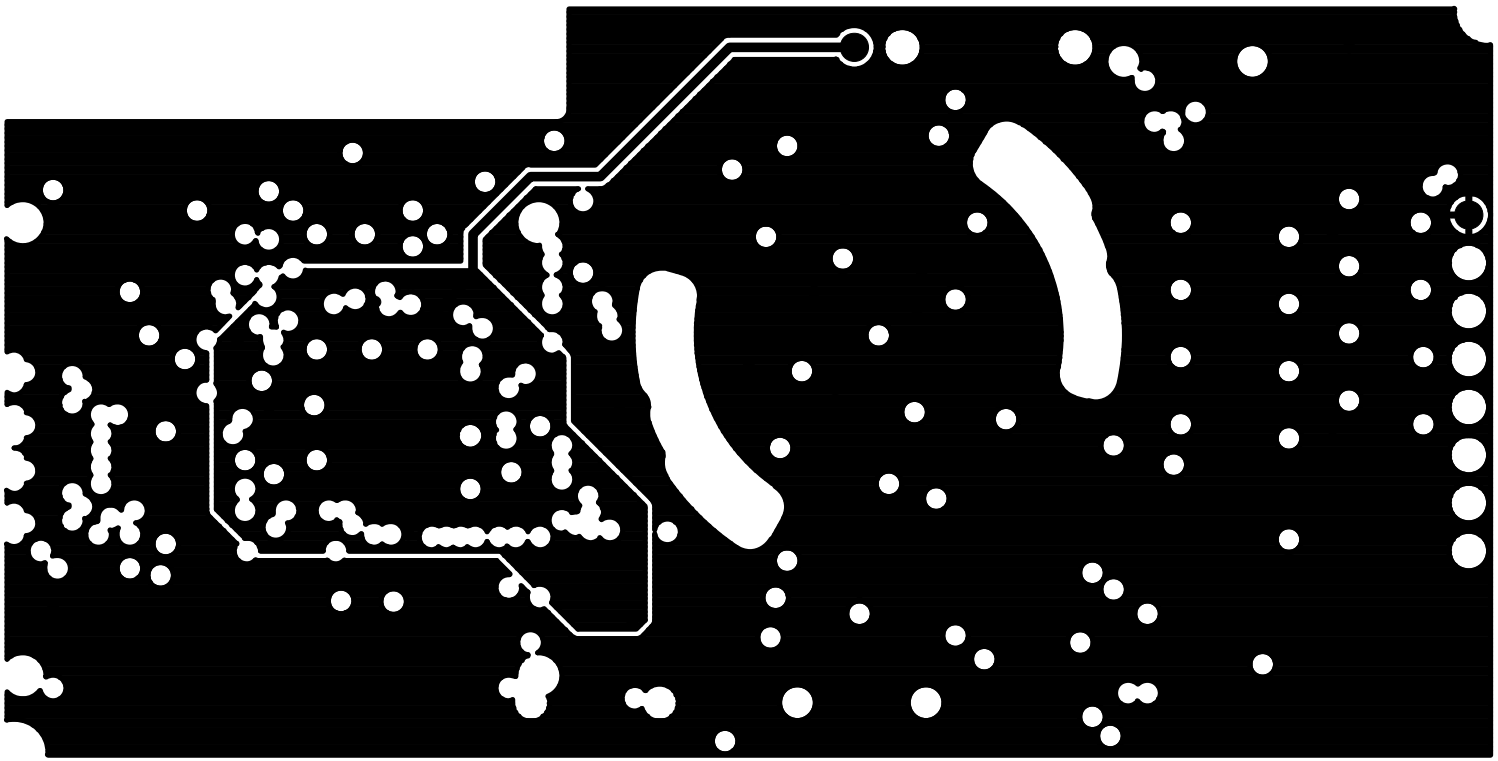


PRIMARY SIDE

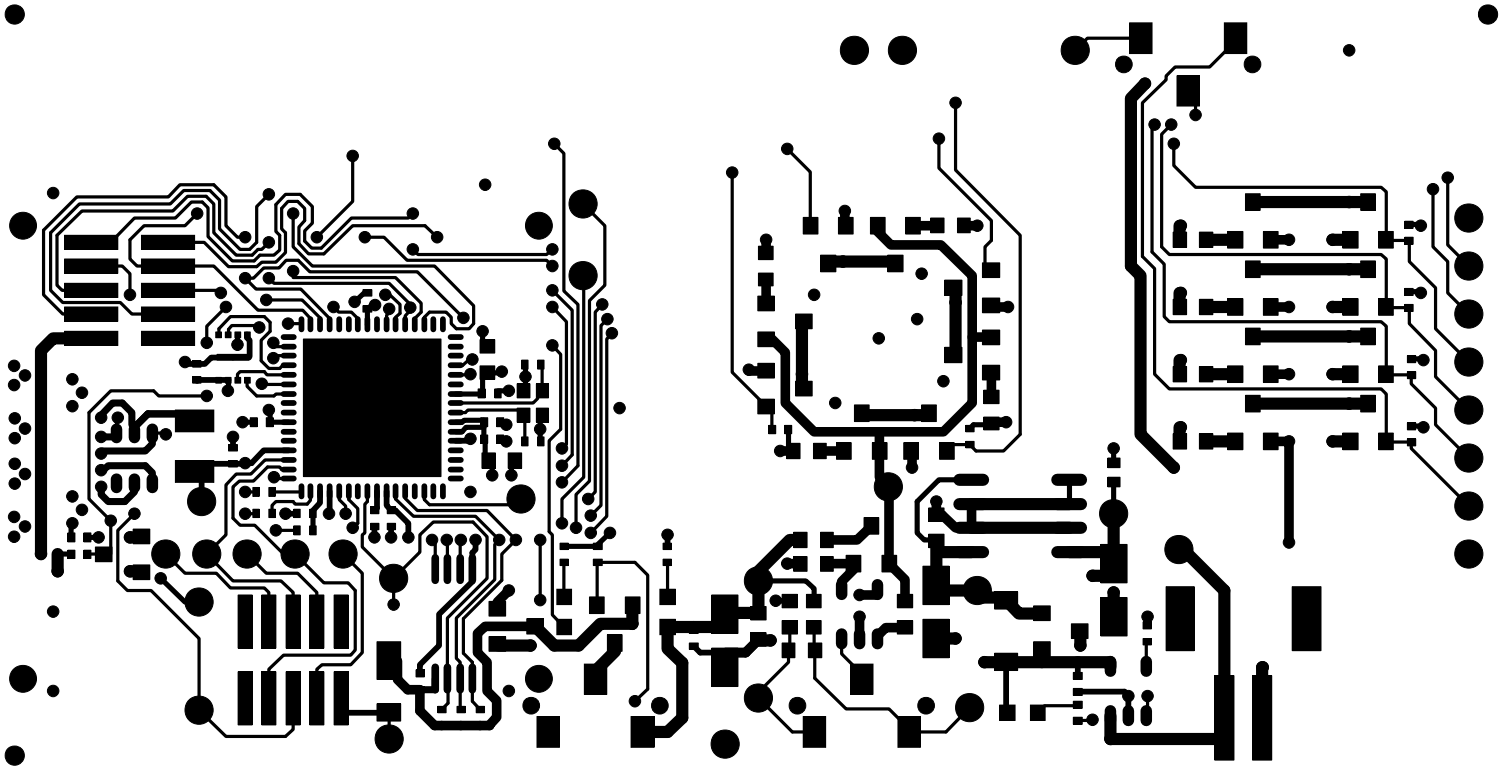


GROUND PLANE

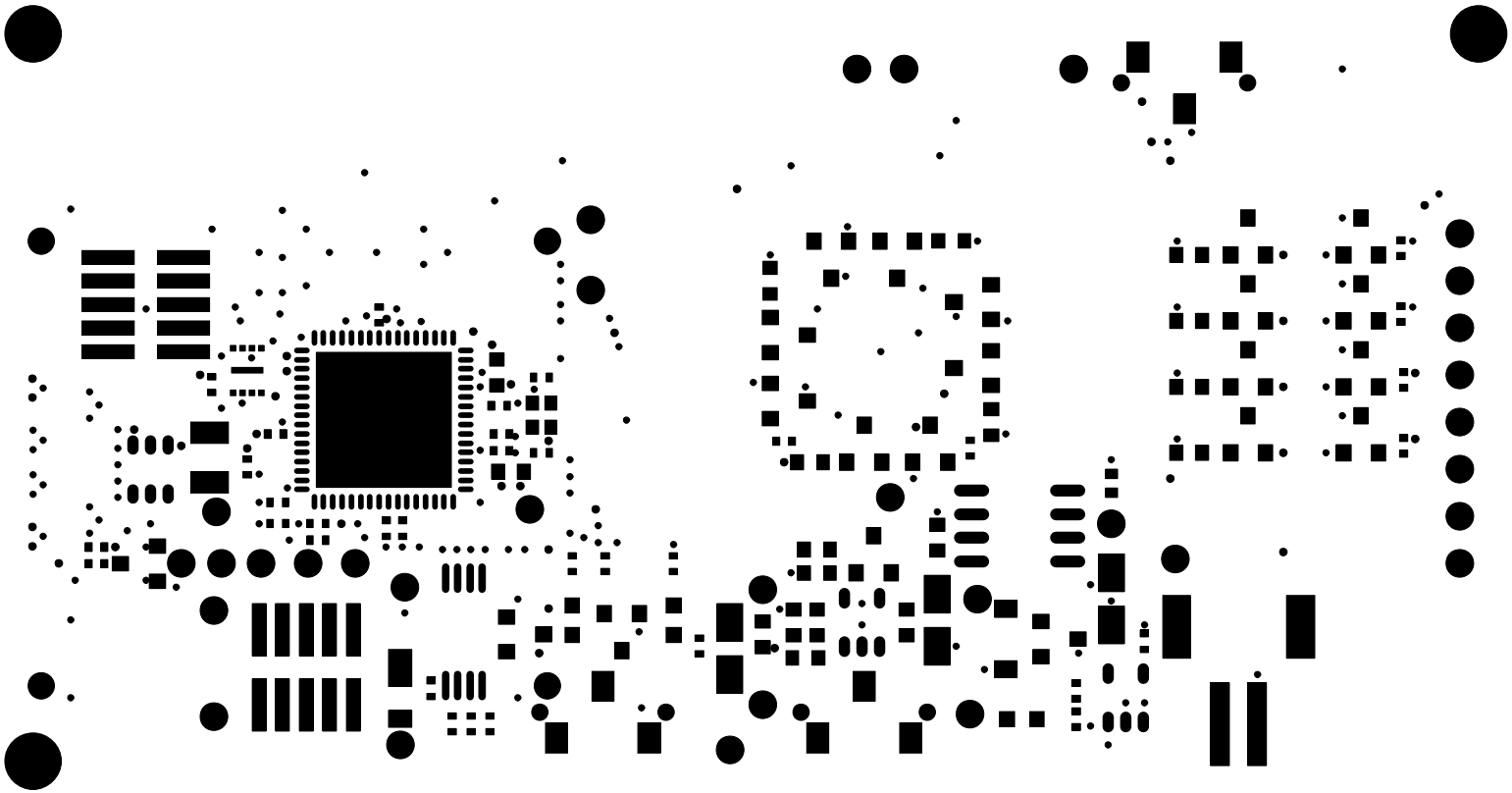
POWER PLANE



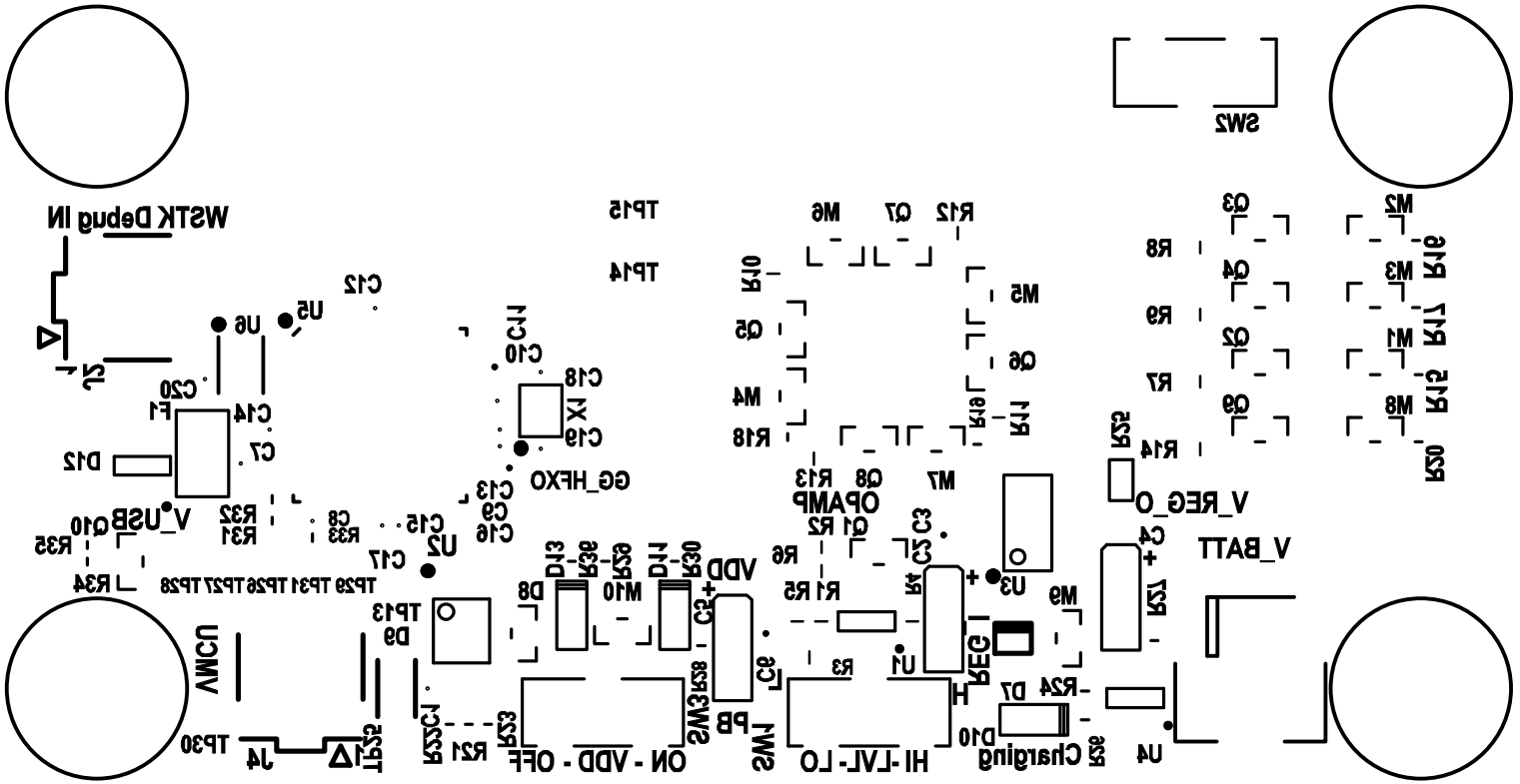
SECONDARY SIDE



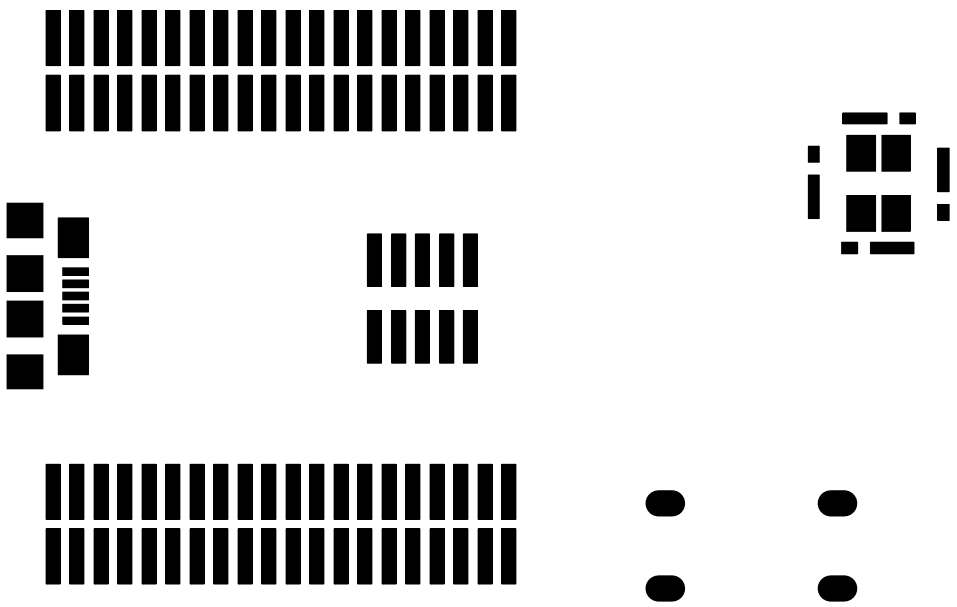
SECONDARY SOLDER MASK



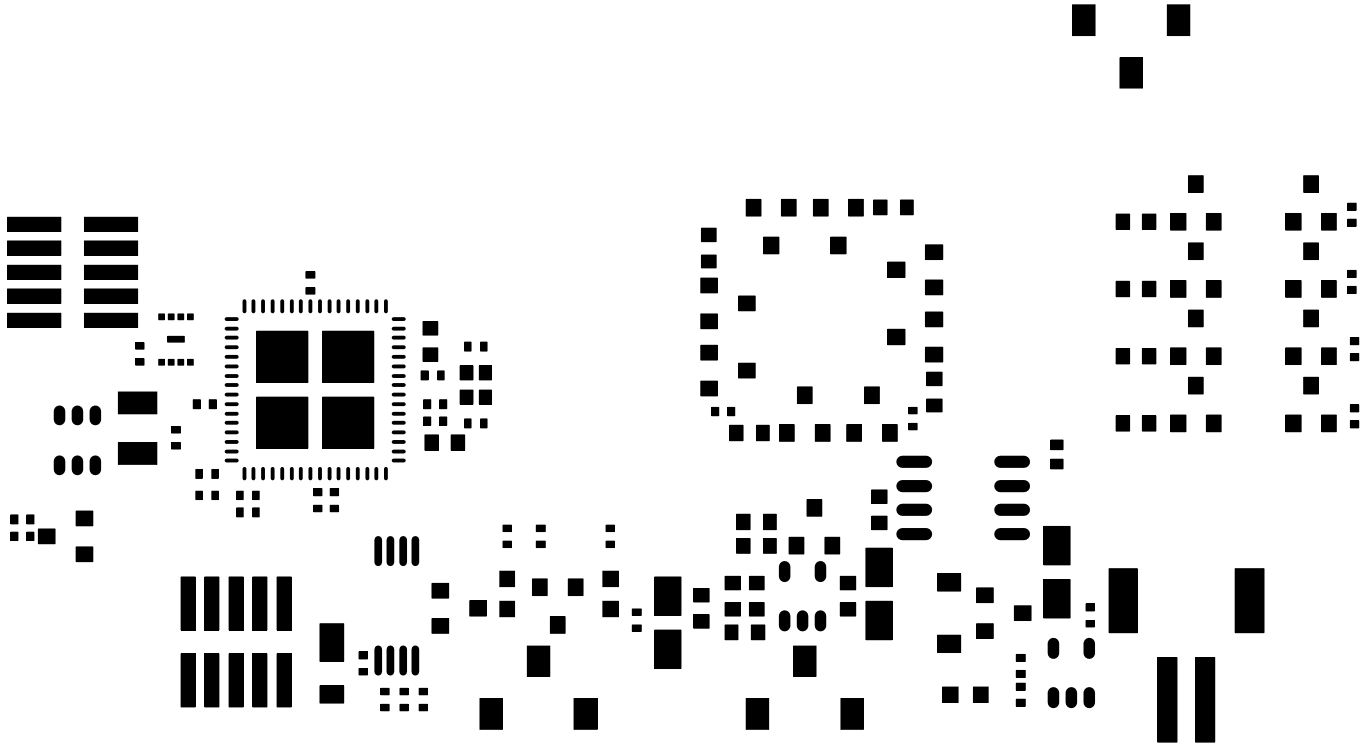
SECONDARY SILKSCREEN

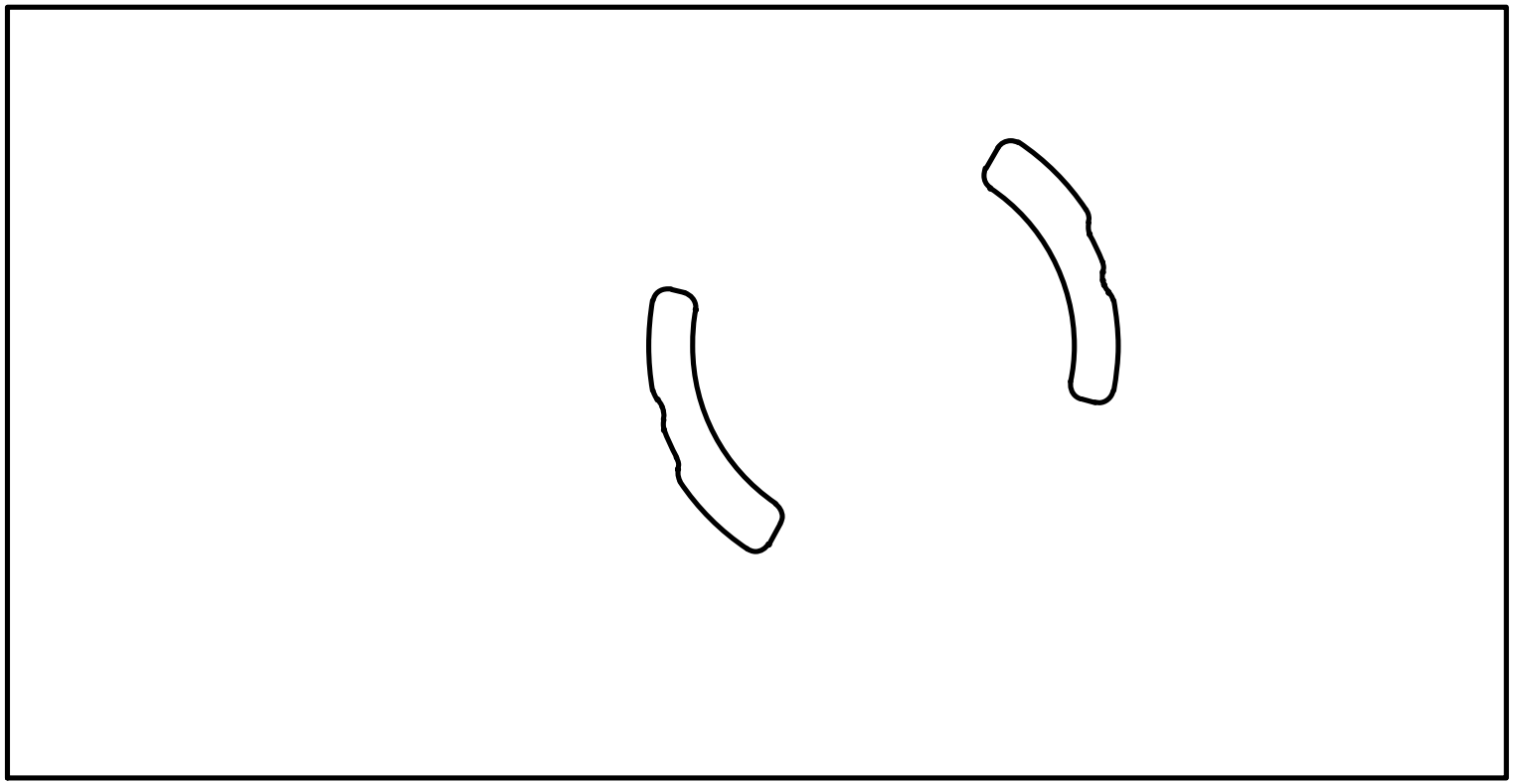


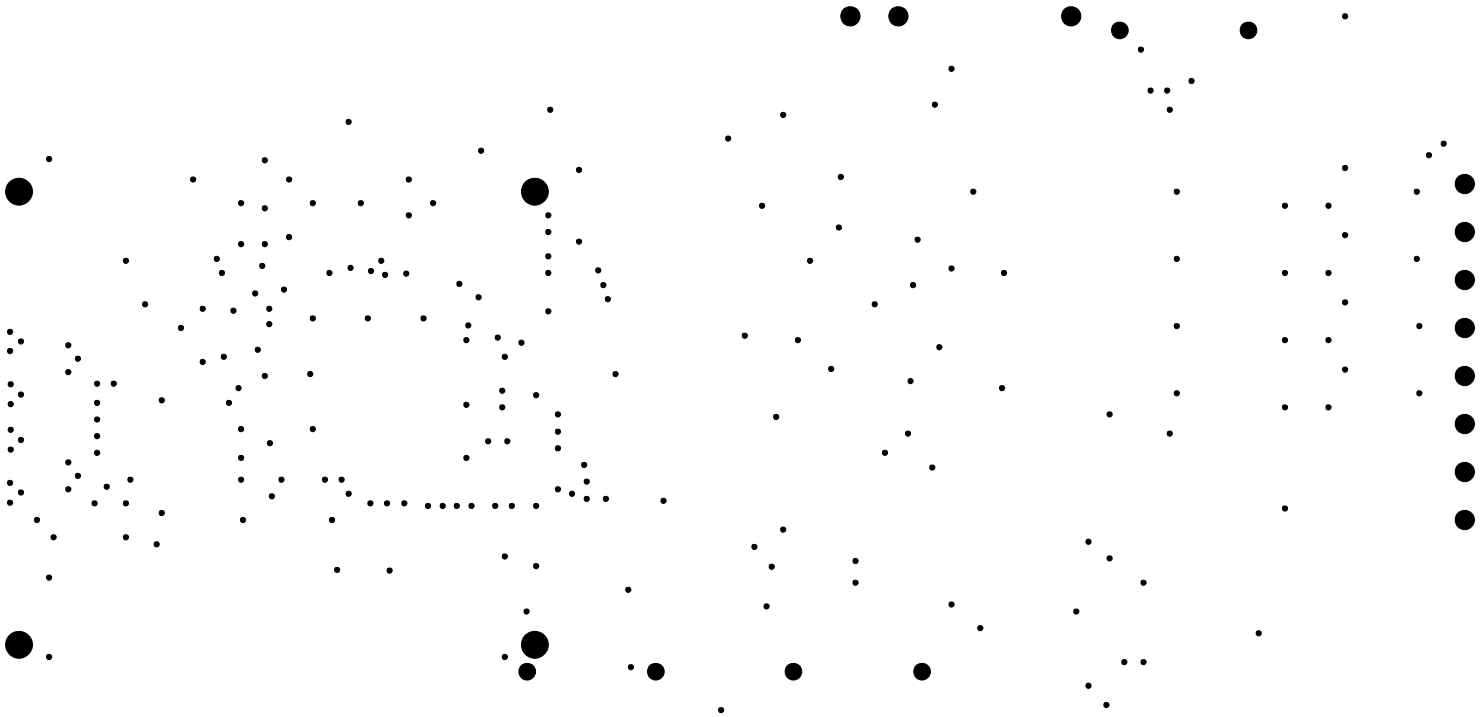
PRIMARY SOLDER PASTE



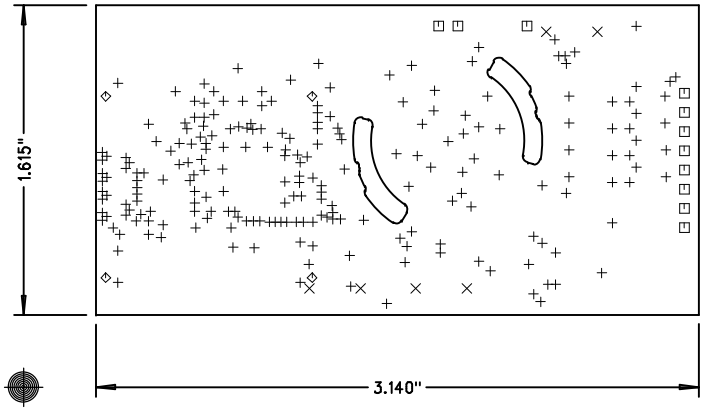
SECONDARY SOLDER PASTE







PRIMARY DRILL



NOTES : UNLESS OTHERWISE SPECIFIED

1. MANUFACTURE IN ACCORDANCE WITH IPC-6012, TYPE 3, CLASS 2.
2. END PRODUCT FEATURES SHALL NOT VARY MORE THAN 20% FROM ARTWORK ORIGINALS.
3. MATERIAL SHALL BE COPPER CLAD FR-4, NEMA GRADE PER IPC-4101/26, COLOR NATURAL.
4. COPPER WEIGHT SHALL BE 0.5 OZ./SQ. FT. BEFORE PLATING.
5. ALL PLATED THROUGH HOLES SHALL HAVE A MINIMUM OF 0.001" COPPER.
6. DRILL HOLE TOLERANCE AFTER PLATING SHALL BE ±0.003".
7. MINIMUM ANNULAR RING SHALL BE 0.001".
8. MINIMUM ANNULAR RING AT EMERGENT CONDUCTORS SHALL BE 0.003".
9. FINAL PCB THICKNESS SHALL BE 0.062" ±10%.
10. WARP/TWIST SHALL NOT EXCEED 1.0%
11. FINISH SHALL BE LPI, BLACK SMOBC, ENIG BOTH SIDES.
12. SILKSCREEN WITH NONCONDUCTIVE WHITE EPOXY INK.
13. REFERENCE ADDITIONAL FAB NOTES IN FILE README.TXT

LAYER STACKUP	FILE NAMES
PRIMARY SILKSCREEN	A50_PSS.PHO
PRIMARY SOLDERMASK	A50_PSM.PHO
PRIMARY SIDE	A50_PRI.PHO
GROUND PLANE	A50_L02.PHO
POWER PLANE	A50_L03.PHO
SECONDARY SIDE	A50_SEC.PHO
SECONDARY SOLDERMASK	A50_SSM.PHO
SECONDARY SILKSCREEN	A50_SSS.PHO

SCALE: NONE

SIZE	QTY	SYM	PLT	TOOL	TOL
0.012	219	+	P	1	+0/-0.012
0.036	6	X	N	2	+/-0.003
0.040	11	□	P	3	+/-0.003
0.056	4	◇	N	4	+/-0.003

UNLESS OTHERWISE SPECIFIED

DIMENSIONS ARE IN INCHES AND APPLY AFTER FINISH

INTERPRET DRAWING PER MIL-D-1000

TOLERANCES

HOLE TOLERANCES PER 78027

DECIMALS	ANGLES	SURFACES
.XX +/- .XXX +/-	+/-	MICROINCHES

PART TO BE FREE OF BURRS

BREAK EDGES	BEND RADIUS	BEND RELIEF
MAX	MAX	MAX

DESIGN	YAS	30JUN2016
LAYOUT	CT	30JUN2016

DO NOT SCALE DRAWING

COMPANY: SILICON LABS
400 W Cesar Chavez
AUSTIN, TX 78701
(512)416-8500
www.silabs.com

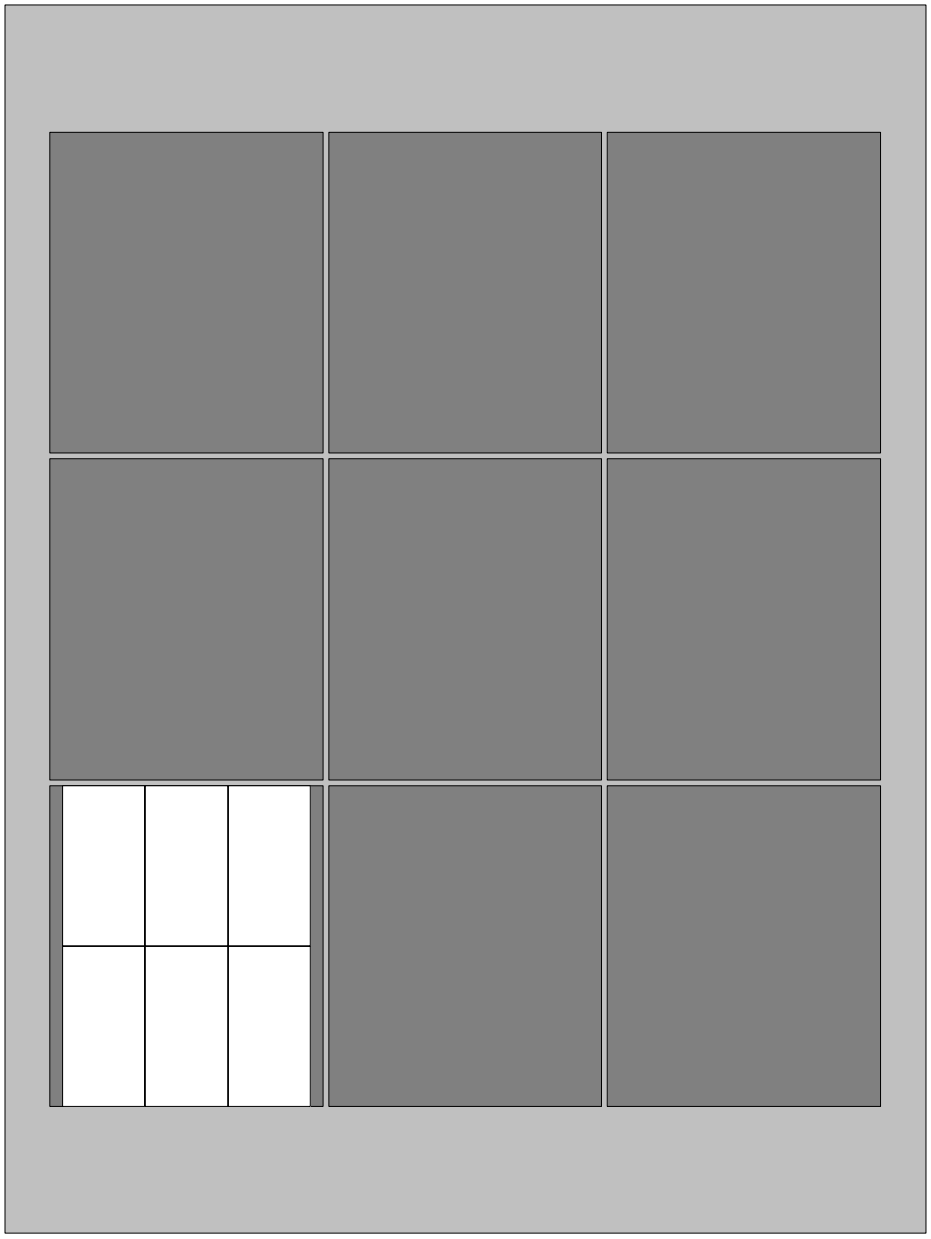
NAME: IST-A0050 .

REV : 5.0

SIZE A

PART NUMBER: .

SCALE 1:1 | FABRICATION DRAWING | SHEET 1 OF 1



IST-A50 REV 5.0

Size:
Panel: 18.0 x 24.0
Array: 5.345 x 6.28
Part: 1.615 x 3.14

Panel Yield:
9 Arrays of 6 Parts
54 Parts Total
69.9% Material Utilization

Matrix:
On Panel: 3 x 3, Origin: X0.8825 Y2.48
On Array: 3 x 2

Spacing:
On Panel: 0.1 x 0.1
On Array: 0.0 x 0.0

Panel Borders:
Left: 0.8825 Right: 0.8825
Top: 2.48 Bottom: 2.48

Array Borders:
Left: 0.25 Right: 0.25
Top: 0.0 Bottom: 0.0

Notes:

Please add 4, 0.125" NP tooling holes located 0.125" from tab corners and 3, 40/120 fiduials to each side of array located 0.25" from tooling holes.