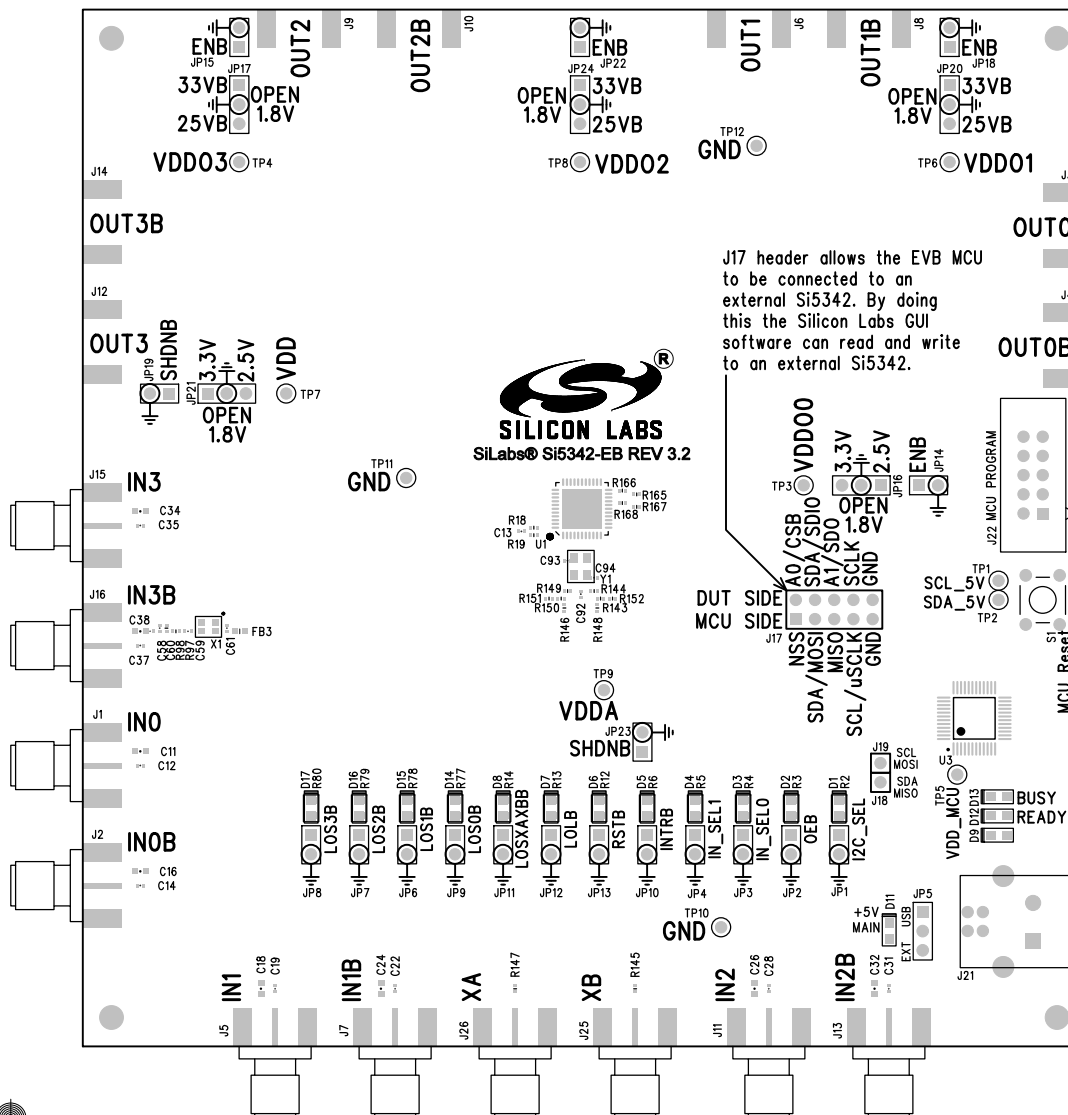
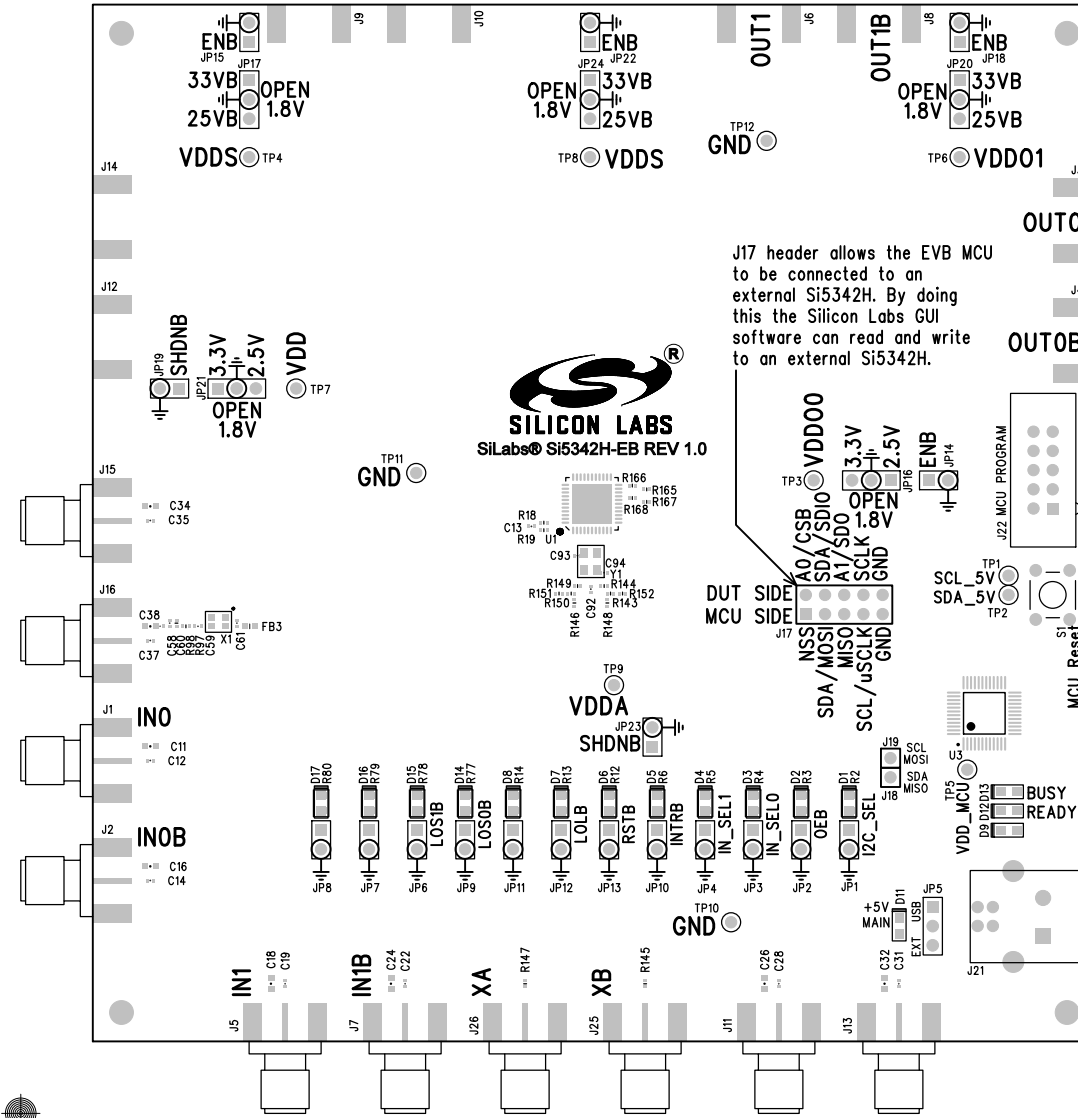


PRIMARY SILKSCREEN

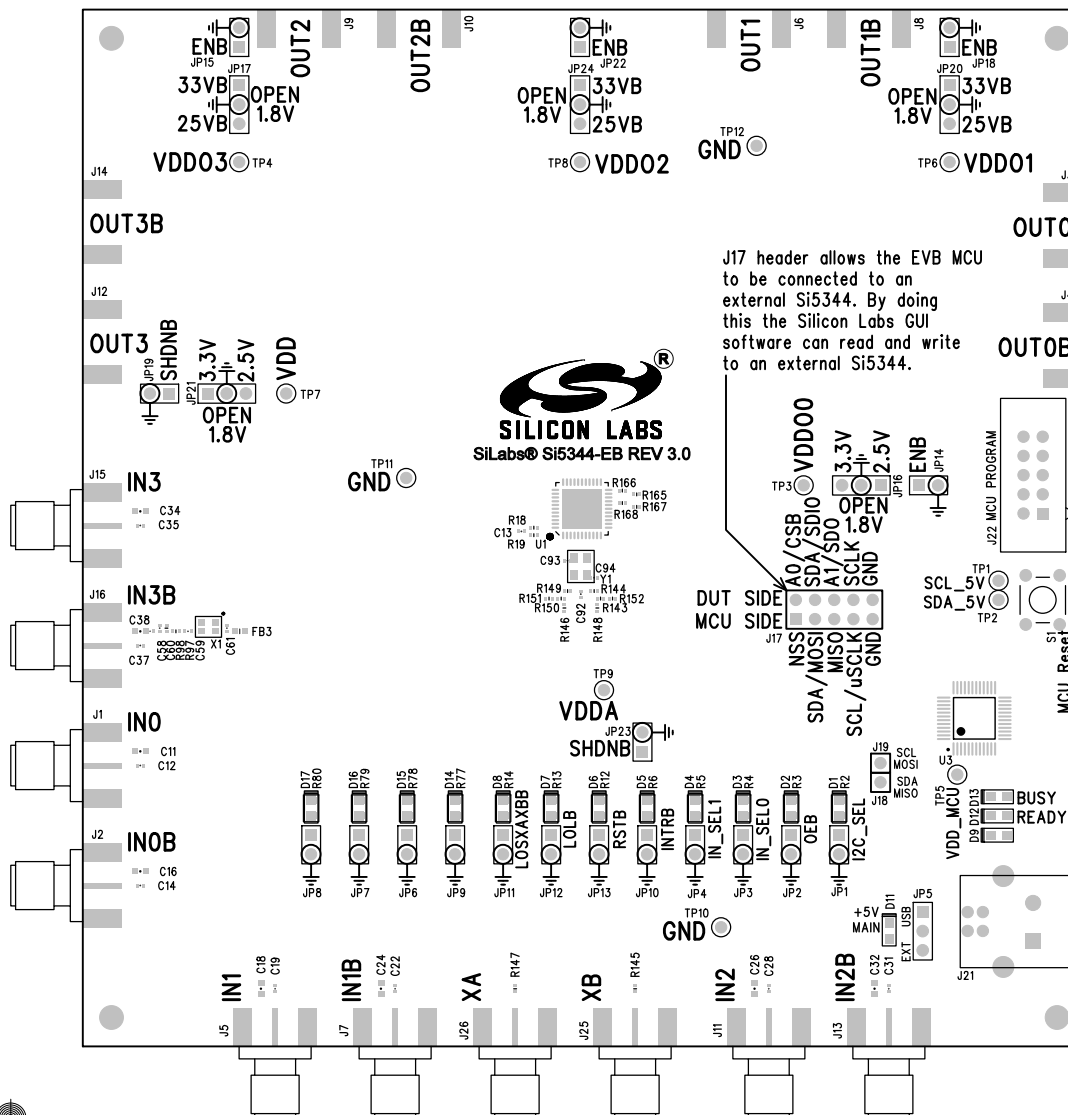


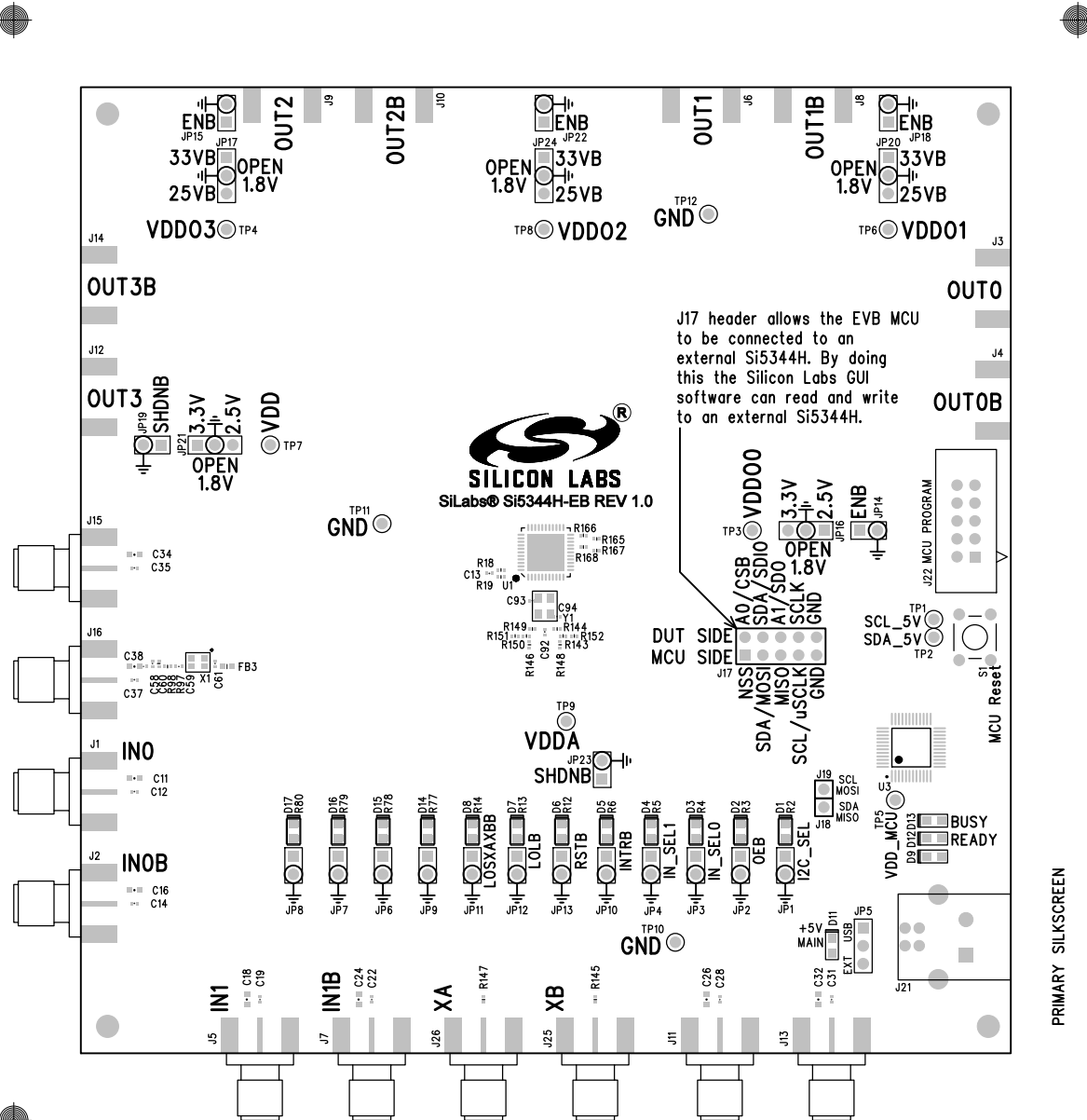




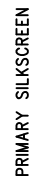
J17 header allows the EVB MCU to be connected to an external Si5342H. By doing this the Silicon Labs GUI software can read and write to an external Si5342H.

PRIMARY SILKSCREEN





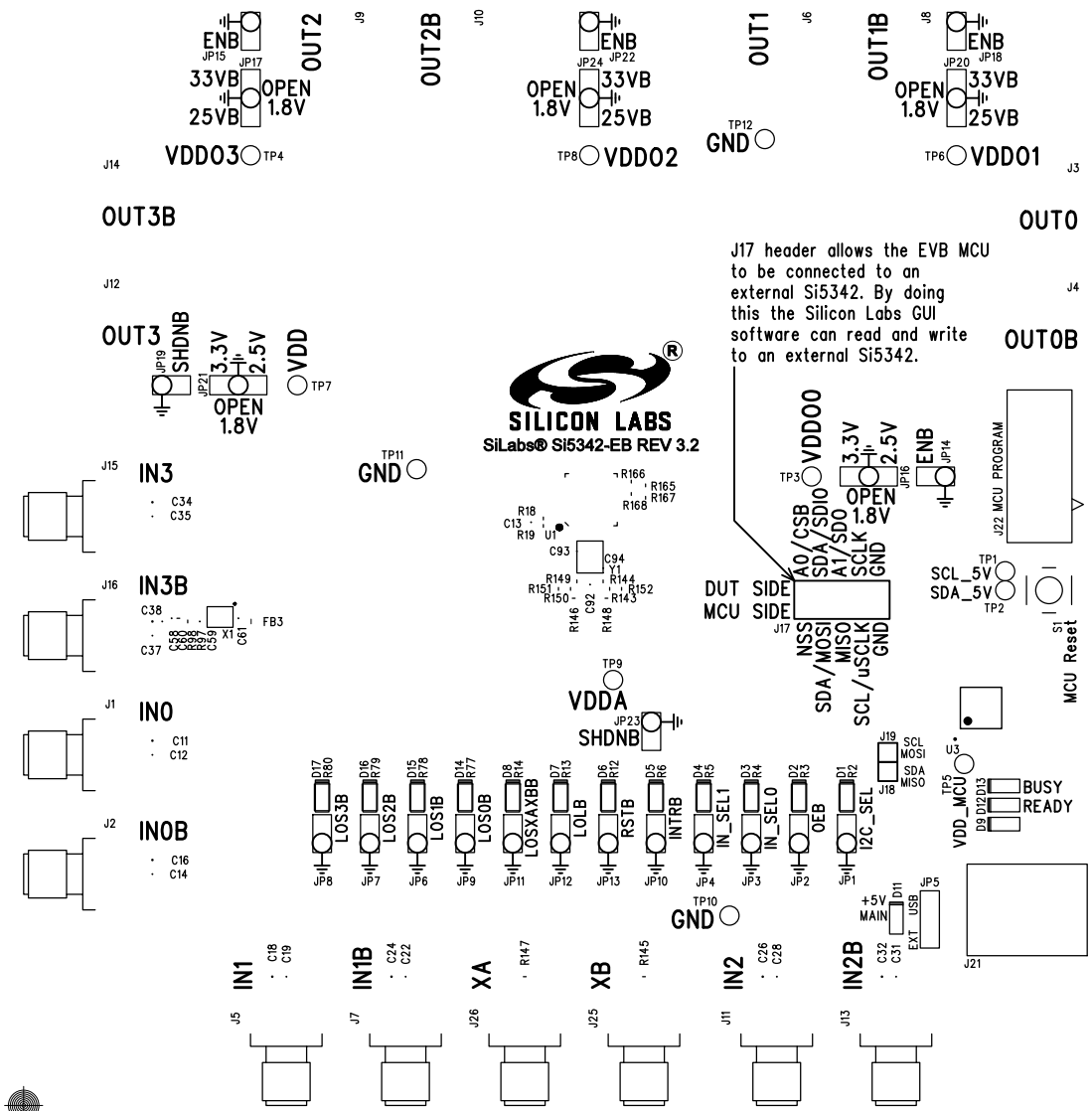
PRIMARY SILKSCREEN

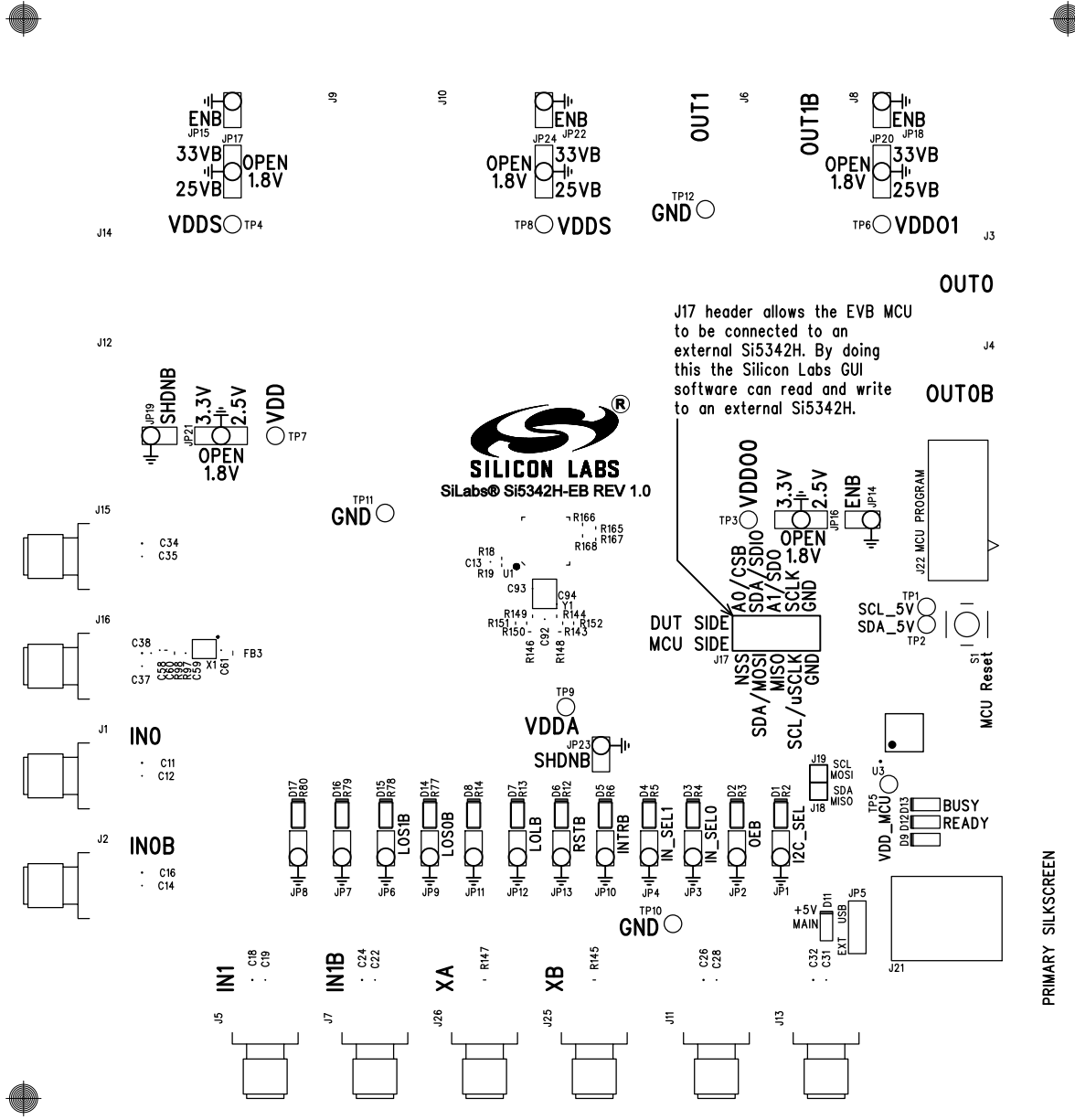


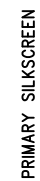
J17 header allows the EVB MCU to be connected to an external Si5346. By doing this the Silicon Labs GUI software can read and write to an external Si5346.

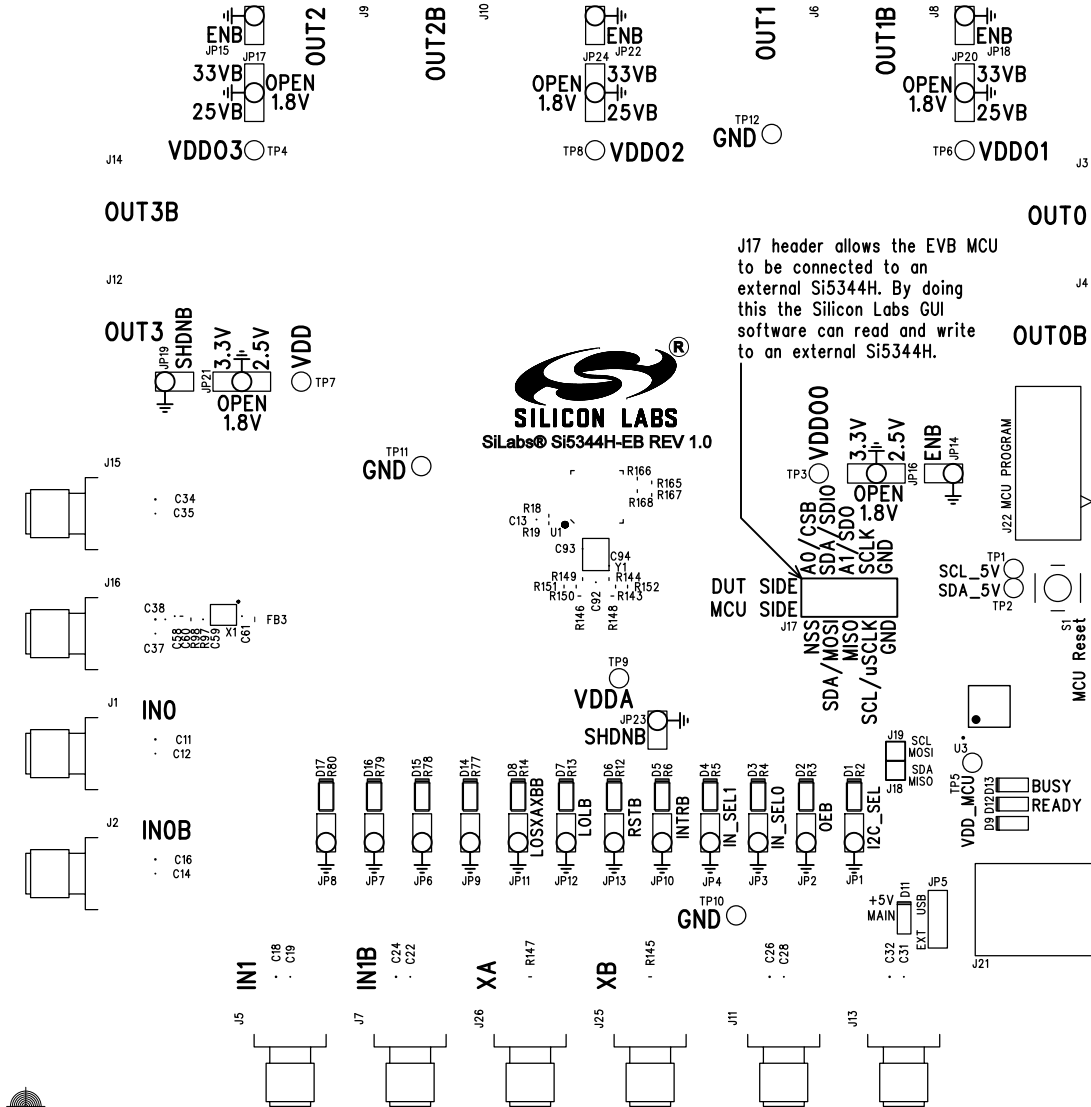


PRIMARY SILKSCREEN





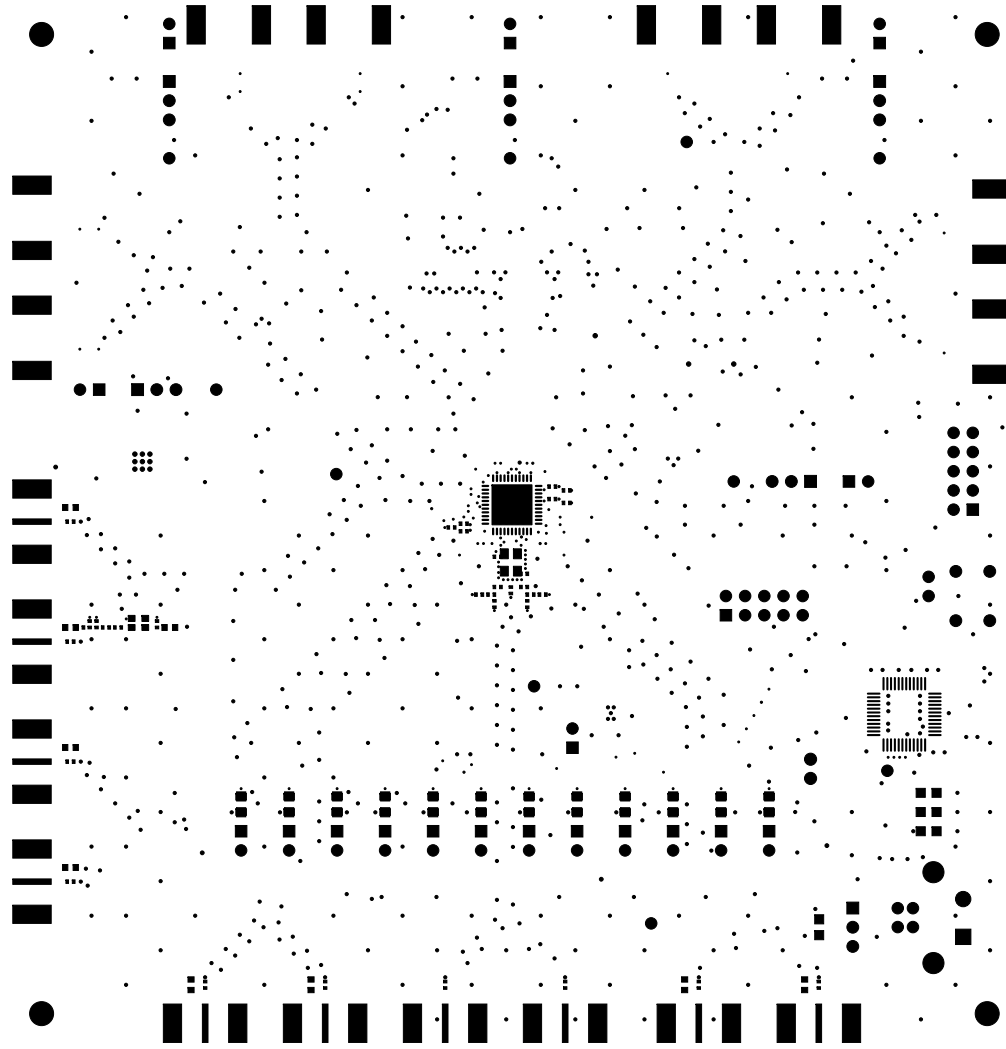




J17 header allows the EVB MCU to be connected to an external Si5344H. By doing this the Silicon Labs GUI software can read and write to an external Si5344H.

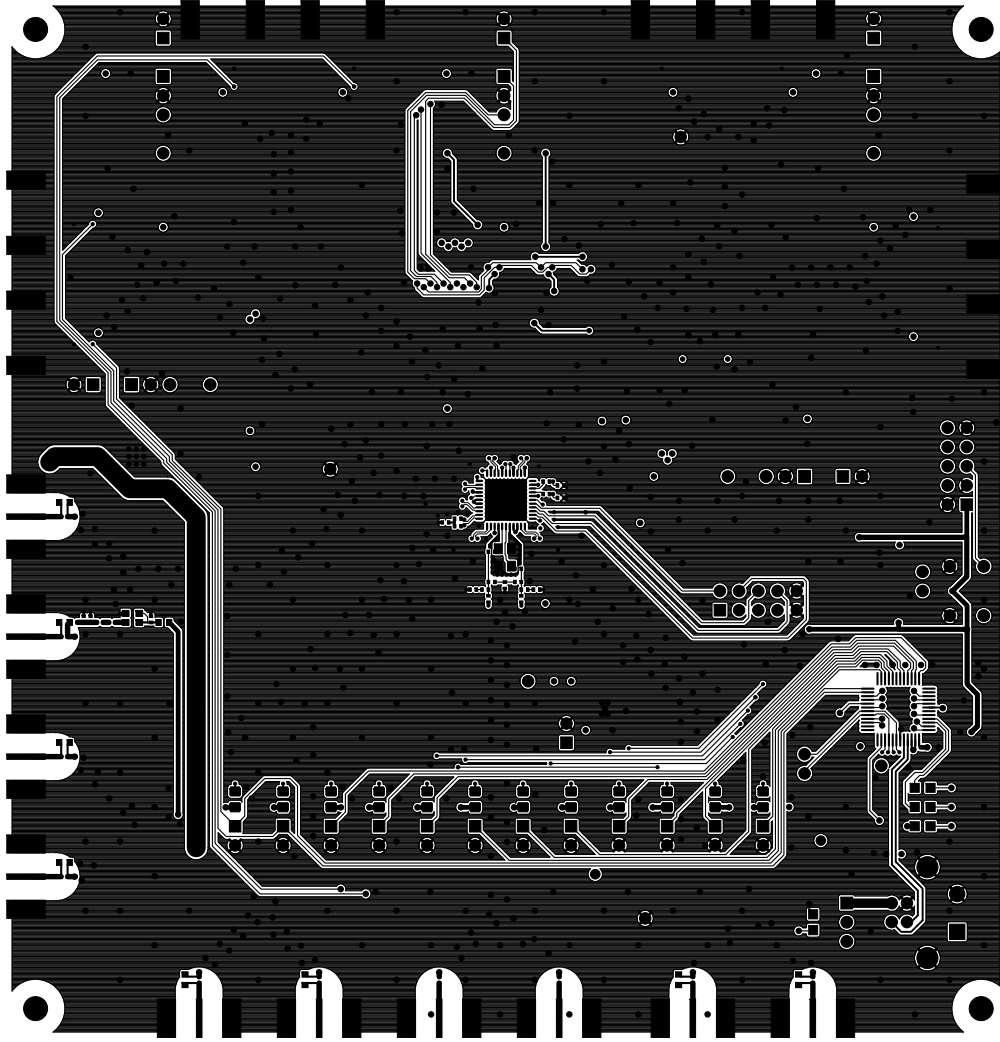


PRIMARY SILKSCREEN

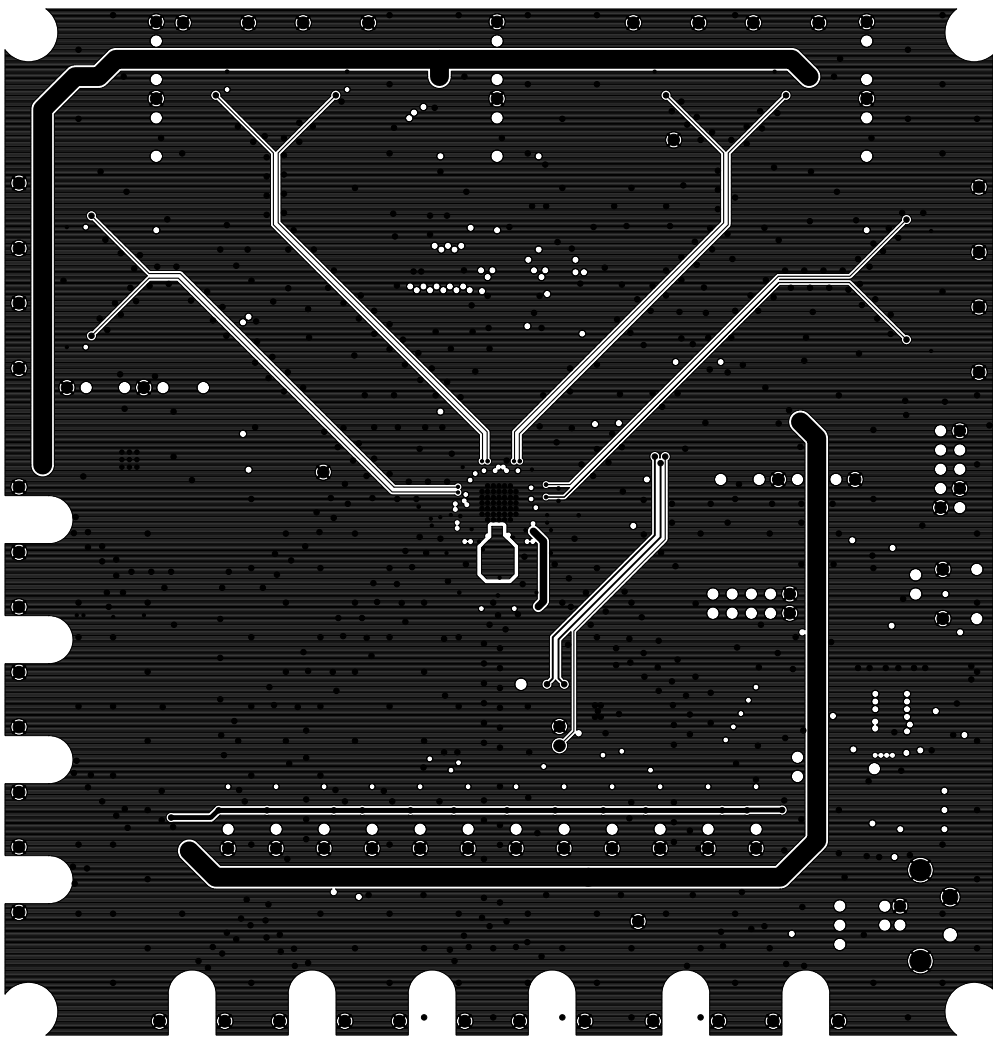


PRIMARY SOLDER MASK



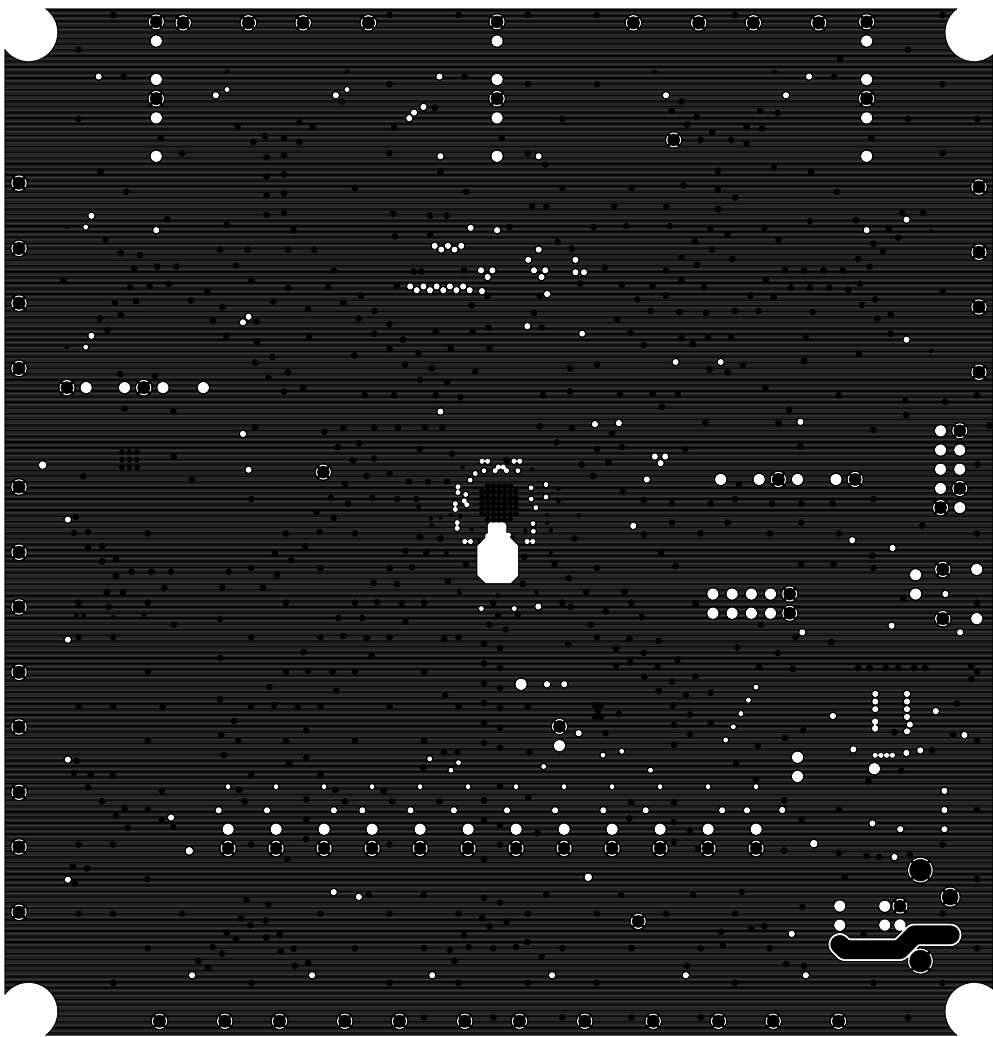


PRIMARY SIDE



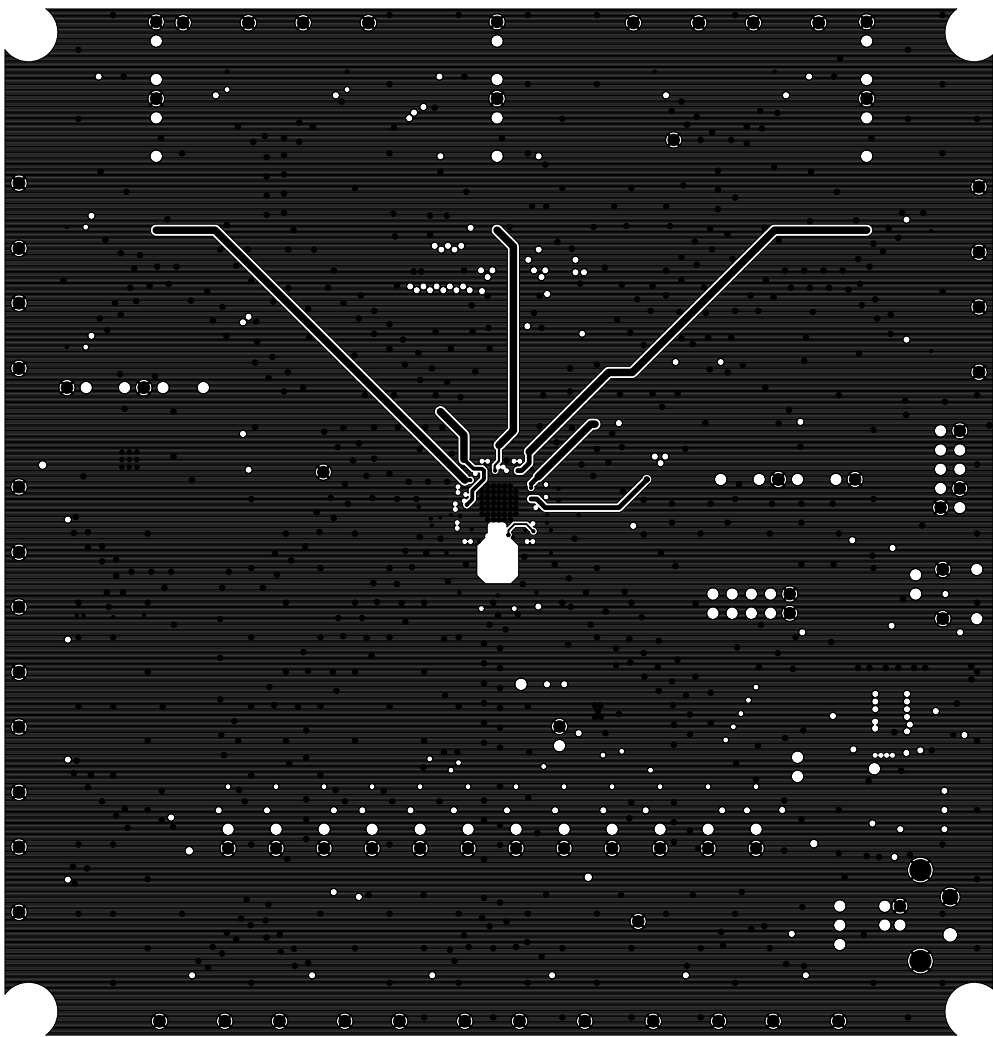
L02





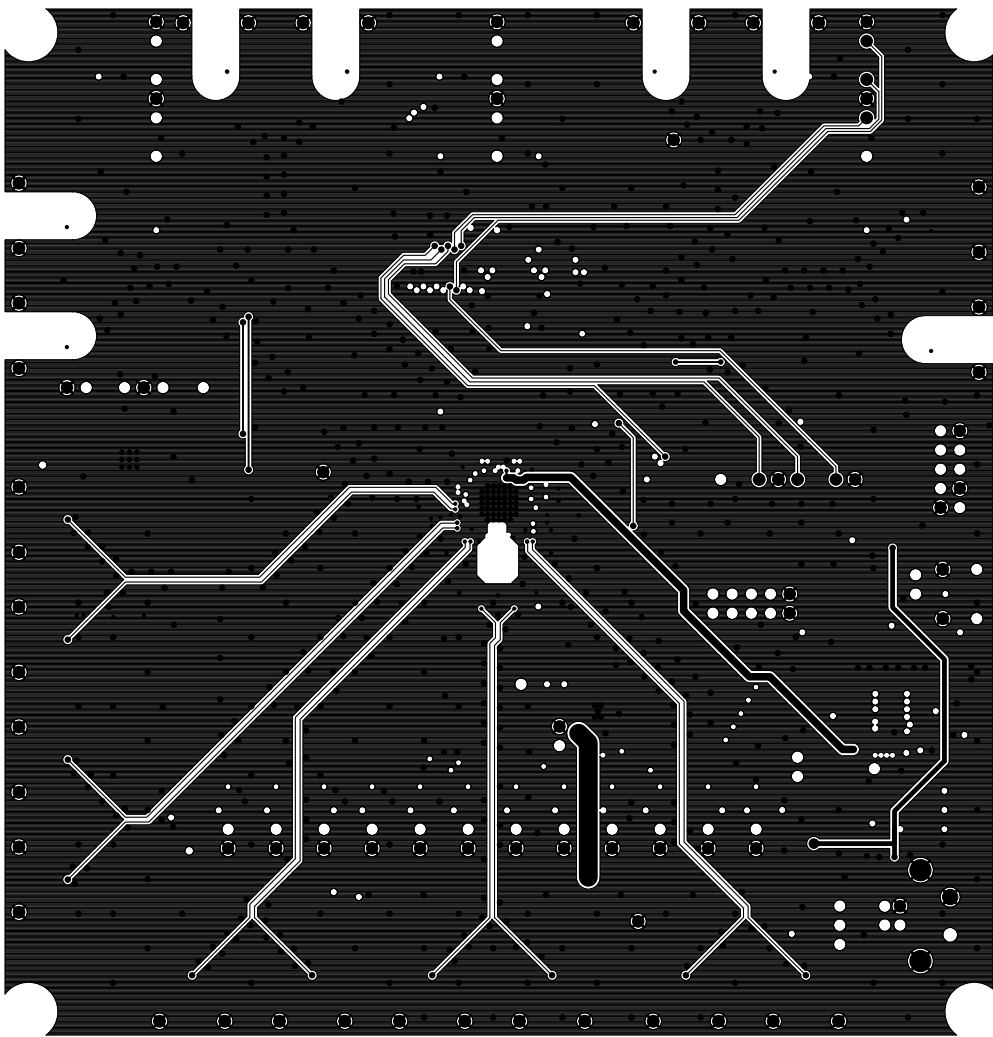
L03





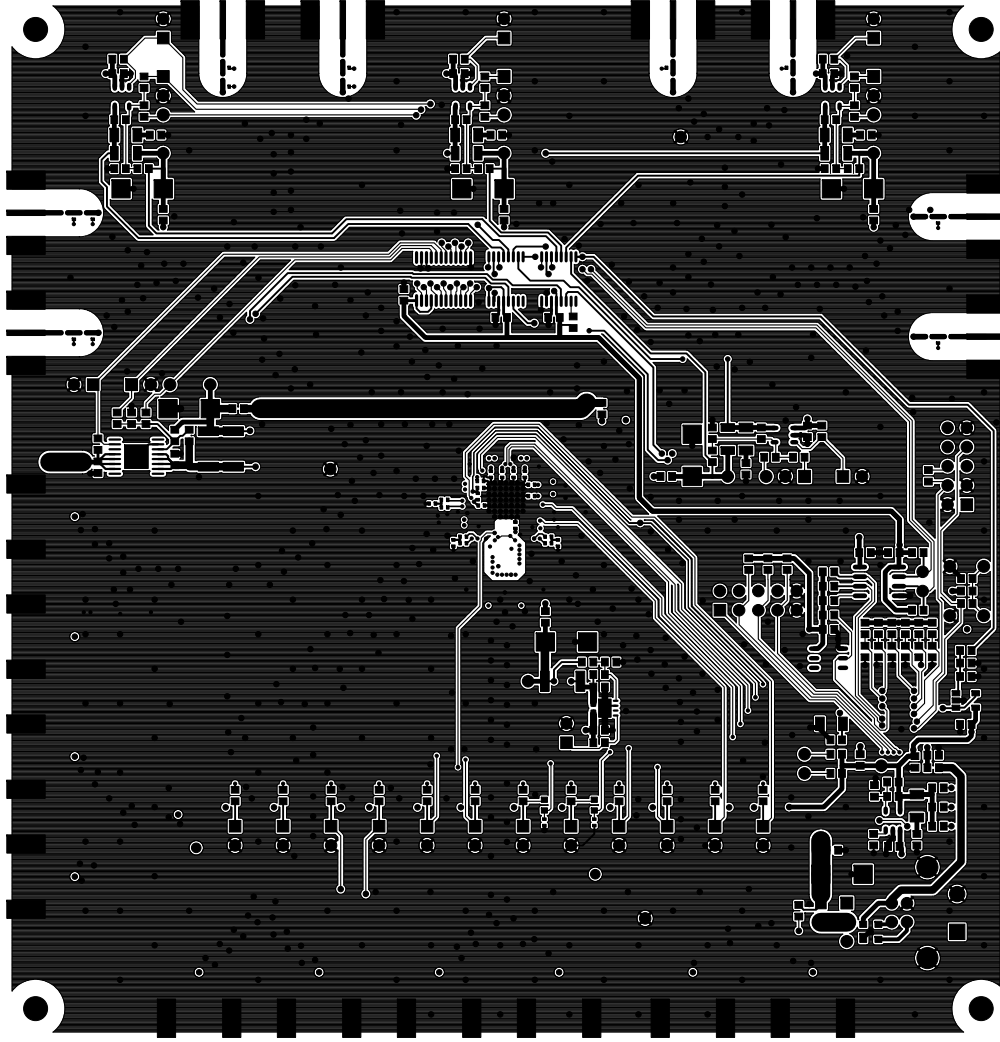
L04



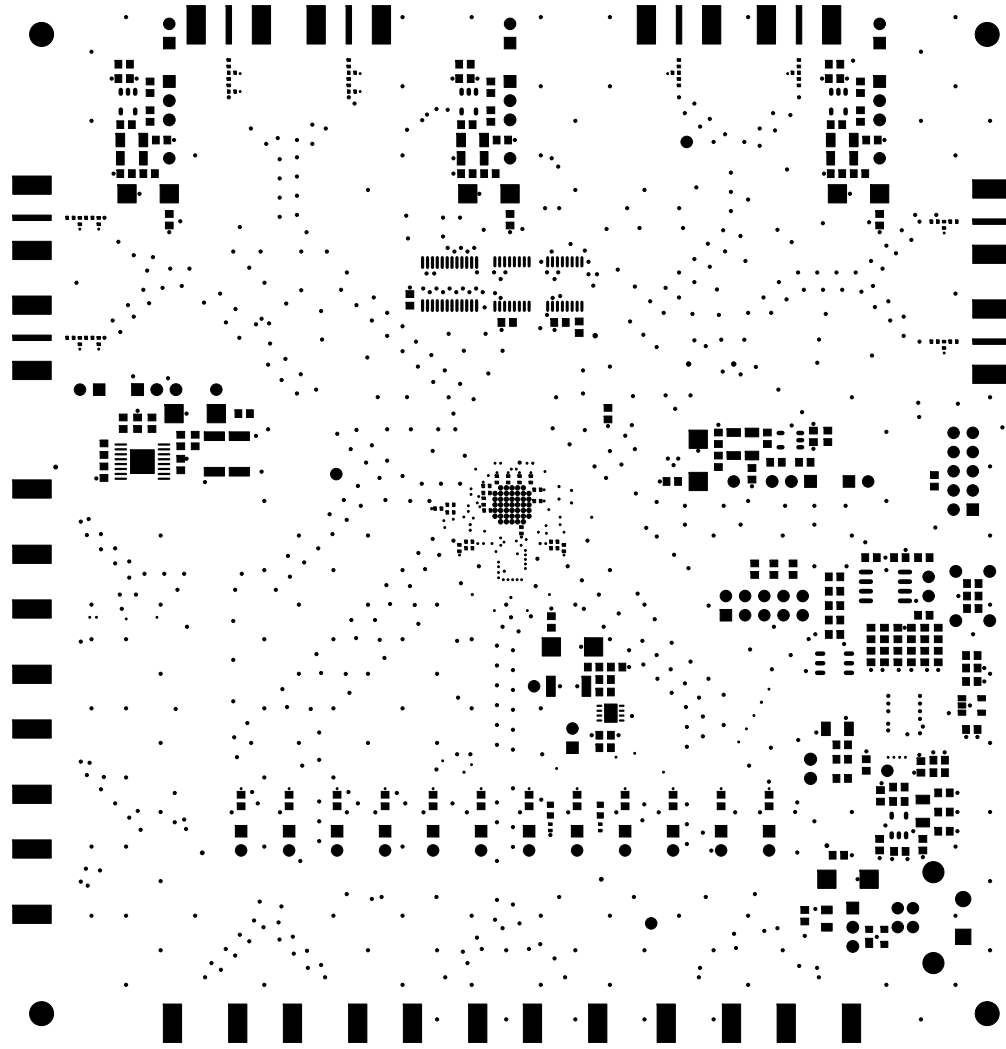


L05



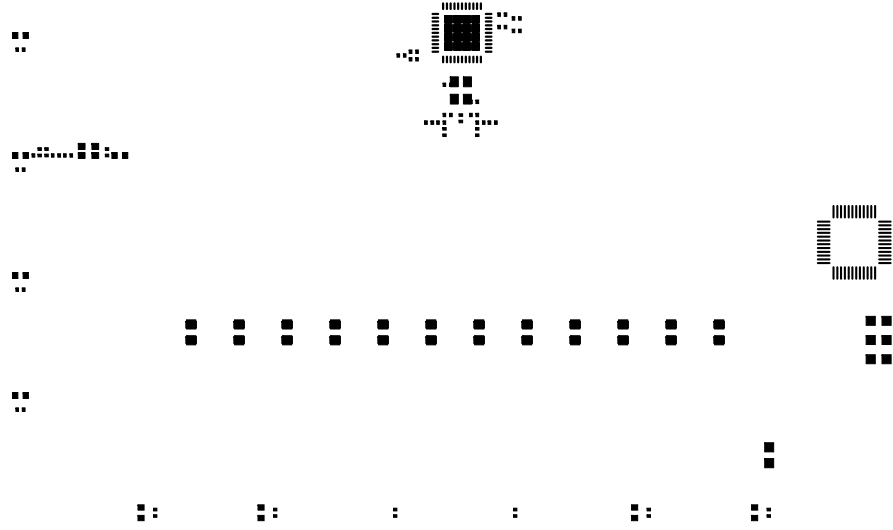


SECONDARY SIDE

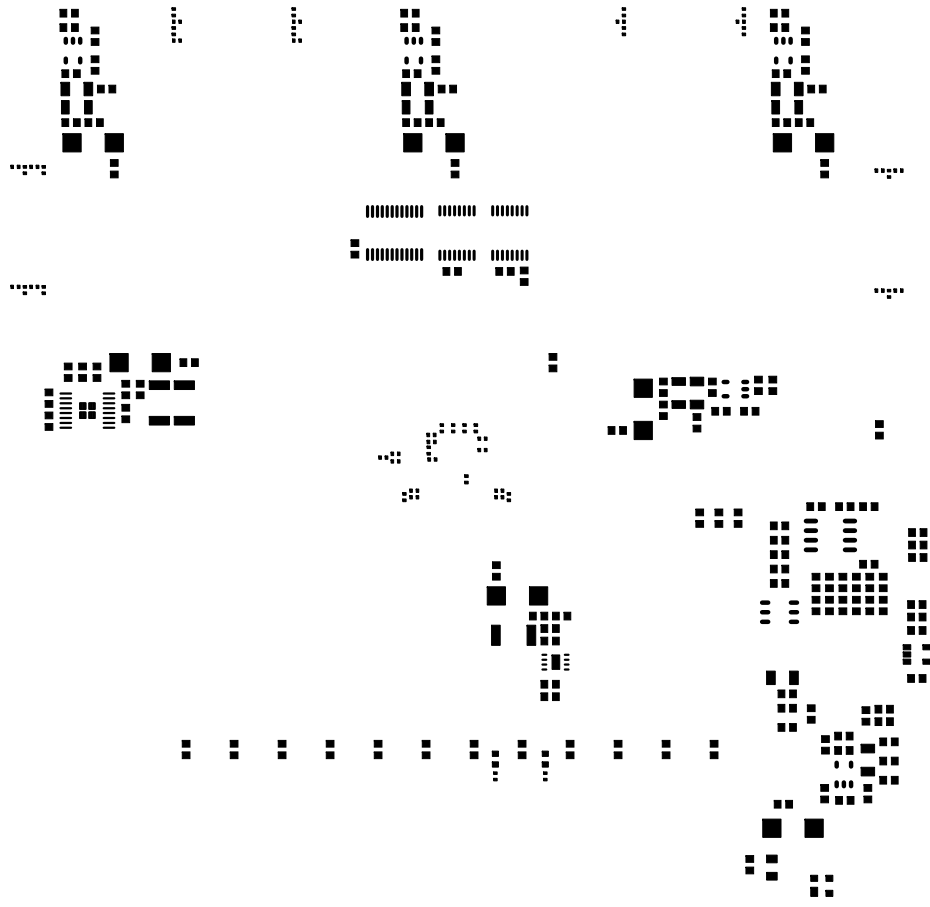


SECONDARY SOLDER MASK



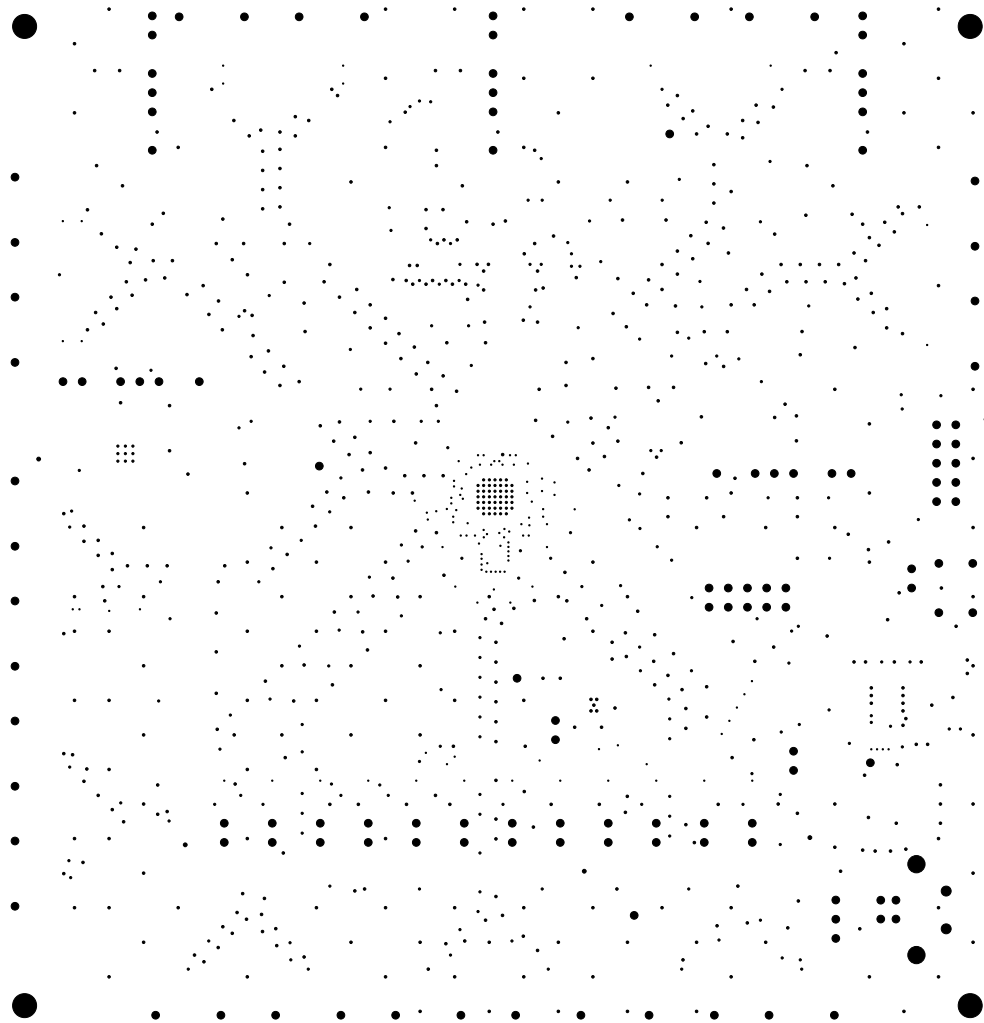


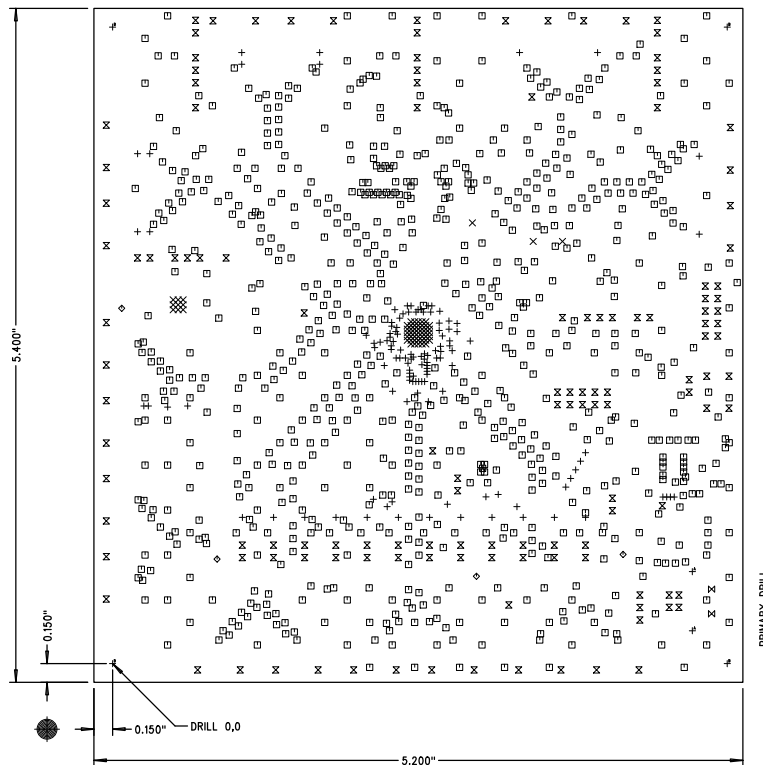
PRIMARY SOLDER PASTE



SECONDARY SOLDER PASTE








NOTES : UNLESS OTHERWISE SPECIFIED

1. MANUFACTURE IN ACCORDANCE WITH IPC-6012, TYPE 3, CLASS 2.
2. END PRODUCT FEATURES SHALL NOT VARY MORE THAN 20% FROM ARTWORK ORIGINALS.
3. MATERIAL SHALL BE COPPER CLAD ISOLA FR-406, Dk=3.9 & ISOLA FR-406 PREPREG, Dk=3.9 w/BALANCE OF MATERIAL TO BE COMPATIBLE FR-4 MEETING IPC-4101/26, PER LAYER STACKUP DETAIL.
4. COPPER WEIGHT SHALL BE 0.5 OZ./SQ. FT. BEFORE PLATING.
5. ALL PLATED THROUGH HOLES SHALL HAVE A MINIMUM OF 0.001" COPPER.
6. DRILL HOLE TOLERANCE AFTER PLATING SHALL BE ± 0.003 ".
7. MINIMUM ANNULAR RING SHALL BE 0.001".
8. MINIMUM ANNULAR RING AT EMERGENT CONDUCTORS SHALL BE 0.003".
9. FINAL PCB THICKNESS SHALL BE 0.062" $\pm 10\%$.
10. WARP/TWIST SHALL NOT EXCEED 1.0X.
11. FINISH SHALL BE LPI, BLUE SMOGG, ENIG BOTH SIDES.
12. SILKSCREEN WITH NONCONDUCTIVE WHITE EPOXY INK.
13. INTERNAL 0.157MM TRACES TO BE 50 OHM $Z_0 \pm 5\%$.
TOP 0.725MM TRACES TO BE 50 OHM $Z_0 \pm 5\%$ REF TO L03.
BOTTOM 0.725MM TRACES TO BE 50 OHM $Z_0 \pm 5\%$ REF TO L04.
14. VENDOR TO PROVIDE PCB MICRO-SECTION OF COUPON AREA & TDR TEST REPORT.
15. REFERENCE ADDITIONAL FAB NOTES IN FILE README.TXT

LAYER STACKUP		FILE NAMES
PRIMARY SILKSCREEN		5346-EB_PSS.PHO
PRIMARY SOLDERMASK		5346-EB_PSM.PHO
PRIMARY SIDE		5346-EB_PRI.PHO
FR-406 - 7MIL THK		
RF ROUTE/GND		5346-EB_L02.PHO
FR-406 - 7MIL THK		
GROUND PLANE		5346-EB_L03.PHO
FR-4 IPC-4101/26		
POWER ROUTE/GND		5346-EB_L04.PHO
FR-406 - 7MIL THK		
RF ROUTE/GND		5346-EB_L05.PHO
FR-406 - 7MIL THK		
SECONDARY SIDE		5346-EB_SEC.PHO
SECONDARY SOLDERMASK		5346-EB_SSM.PHO
SECONDARY SILKSCREEN		5346-EB_SSS.PHO

SCALE: NONE

SIZE	QTY	SYM	PLT	TOOL	TOL
0.007	124	+	P	1	+0/-0.007
0.012	57	×	P	2	+0/-0.012
0.013	771	□	P	3	+0/-0.013
0.020	4	◇	P	4	+/-0.003
0.040	132	⊗	P	5	+/-0.003
0.052	2	⊗	P	6	+/-0.003
0.091	2	A	P	7	+/-0.003
0.125	4	B	N	8	+/-0.003

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DIMENSIONS ARE IN INCHES AND APPLY AFTER FINISH DIMENSIONS IN BRACKETS () ARE IN MILLIMETERS INTERPRET DRAWING PER MIL-D-1000		TOLERANCES		NAME: Si534x-EB44	
HOLE TOLERANCES PER 78027		TOLERANCES		REV: 3.0	
DECIMALS XX +/- .XXX +/-	ANGLES +/-	SURFACES MICRONICHES		DESIGN LAYOUT	MA CT
PART TO BE FREE OF BURRS		DATE: 11JUL2014		SIZE B	PART NUMBER:
BREAK EDGES MAX	BEND RADIUS MAX	BEND RELIEF MAX		DO NOT SCALE DRAWING	
SCALE: 1:1		FABRICATION DRAWING		SHEET 1 OF 1	