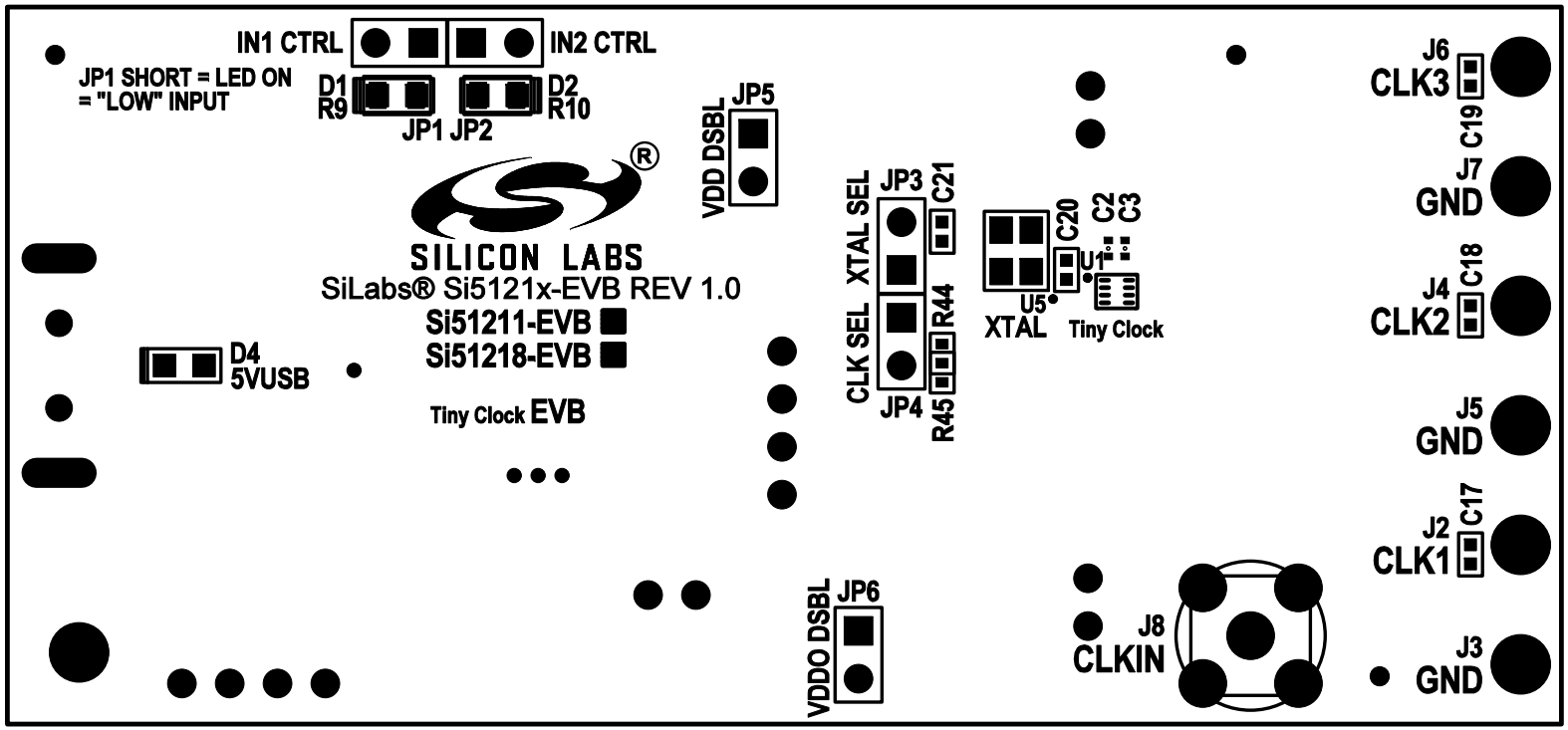
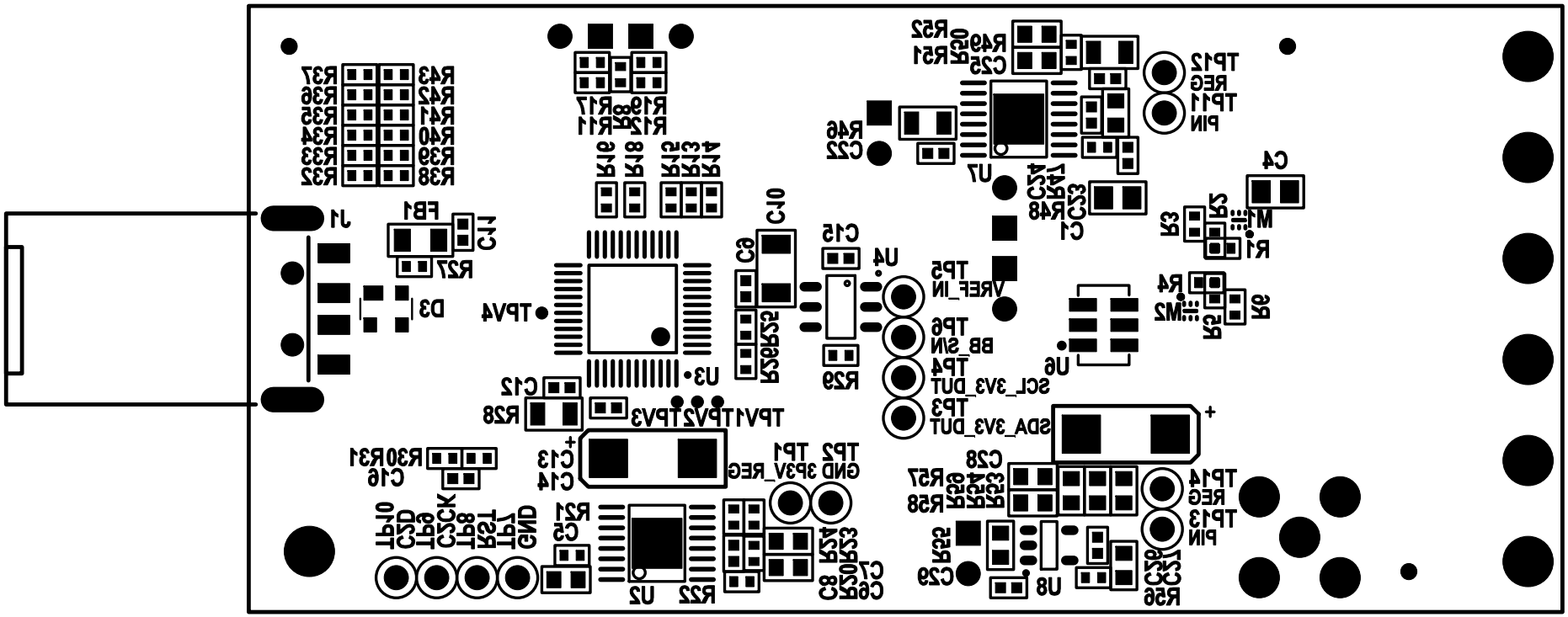
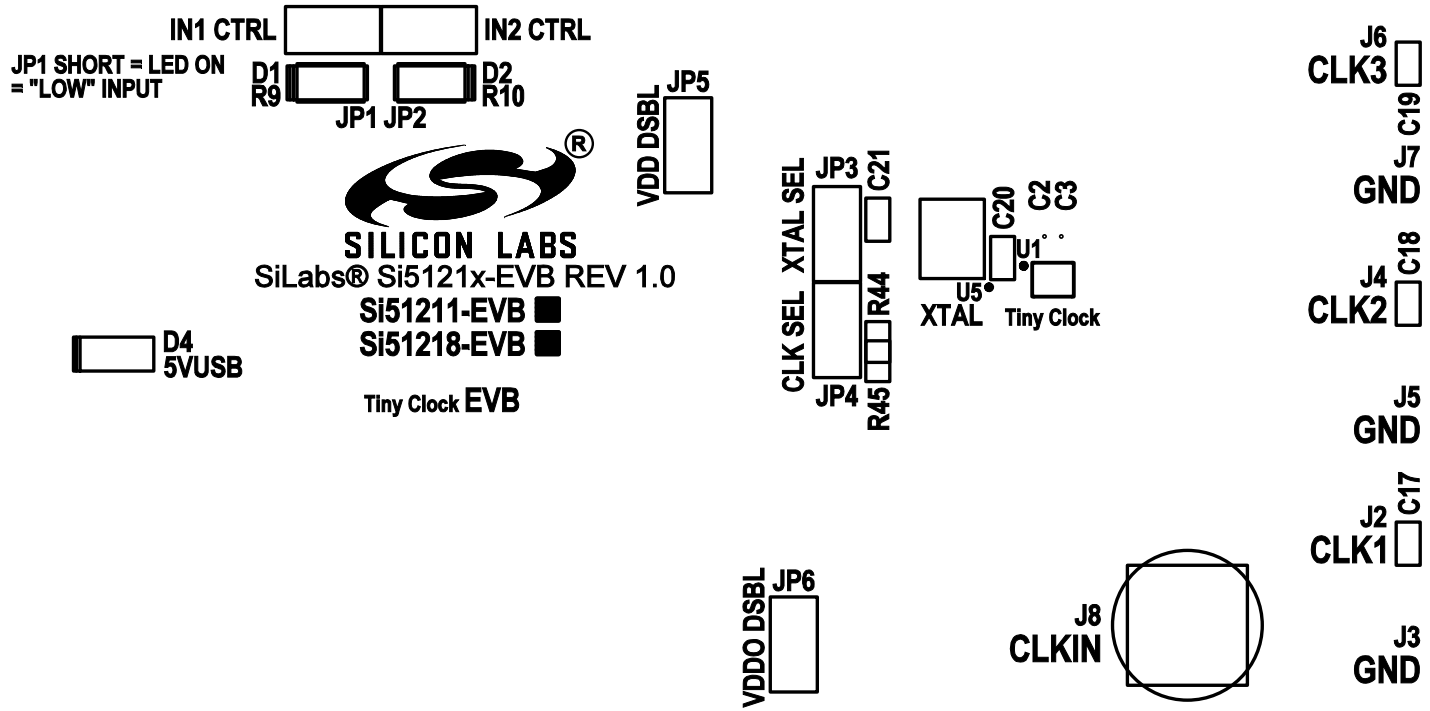


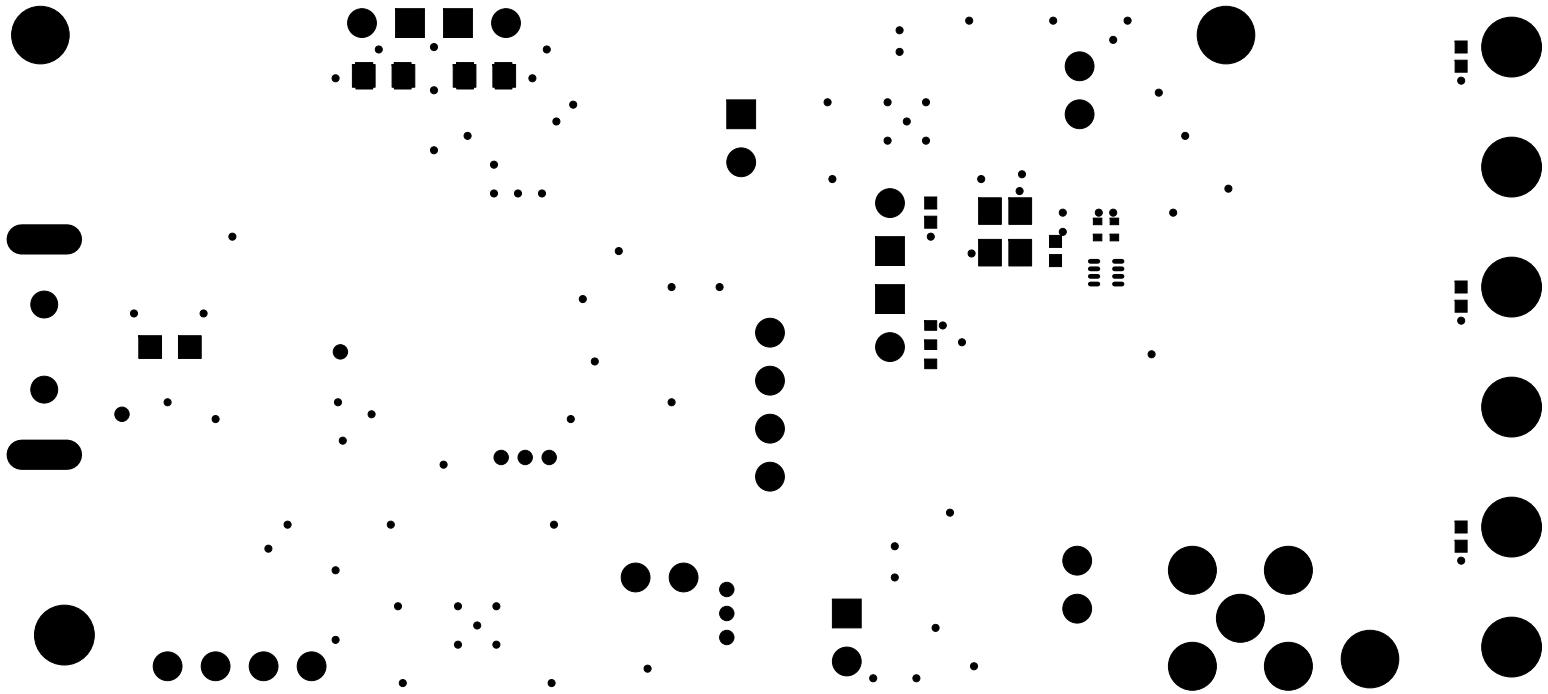
PRIMARY SILKSCREEN



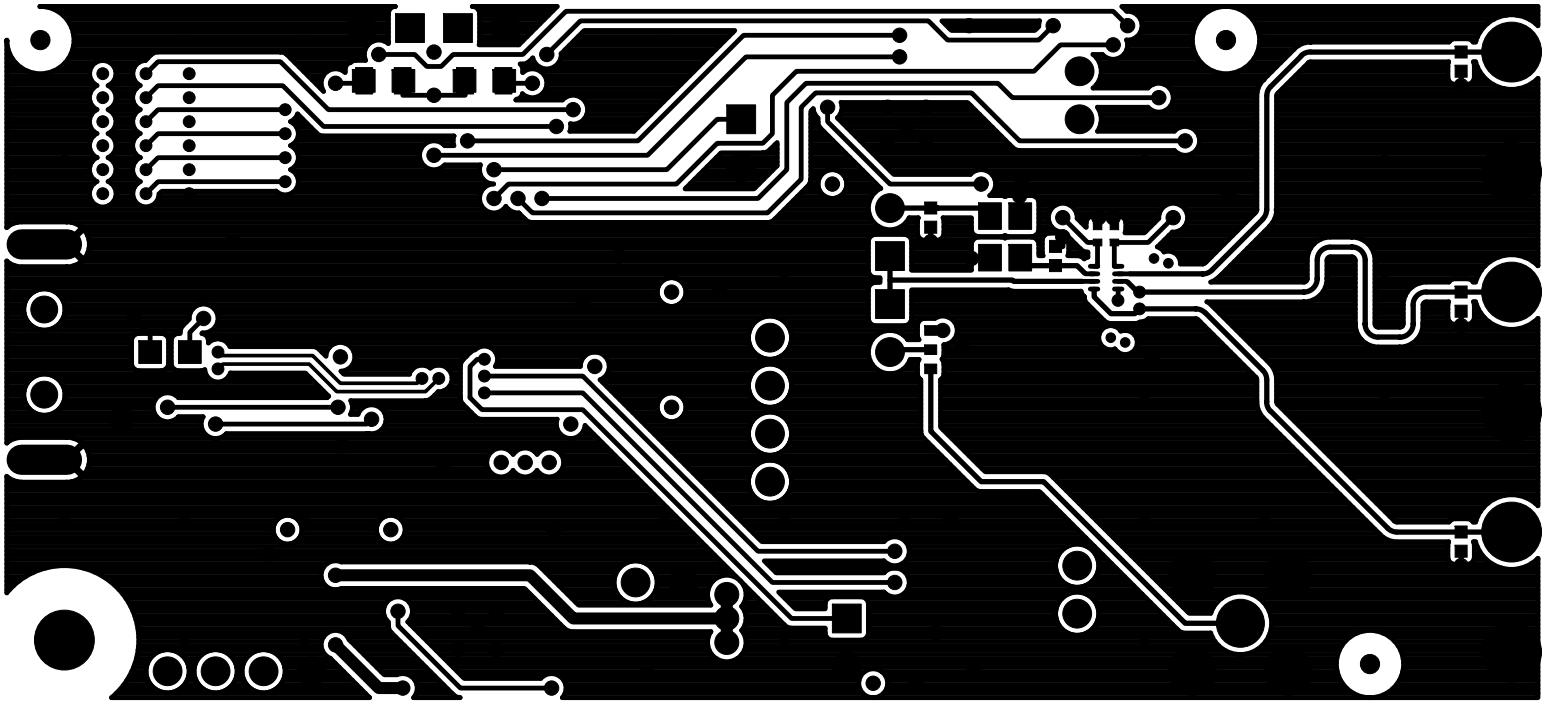
SECONDARY SILKSCREEN



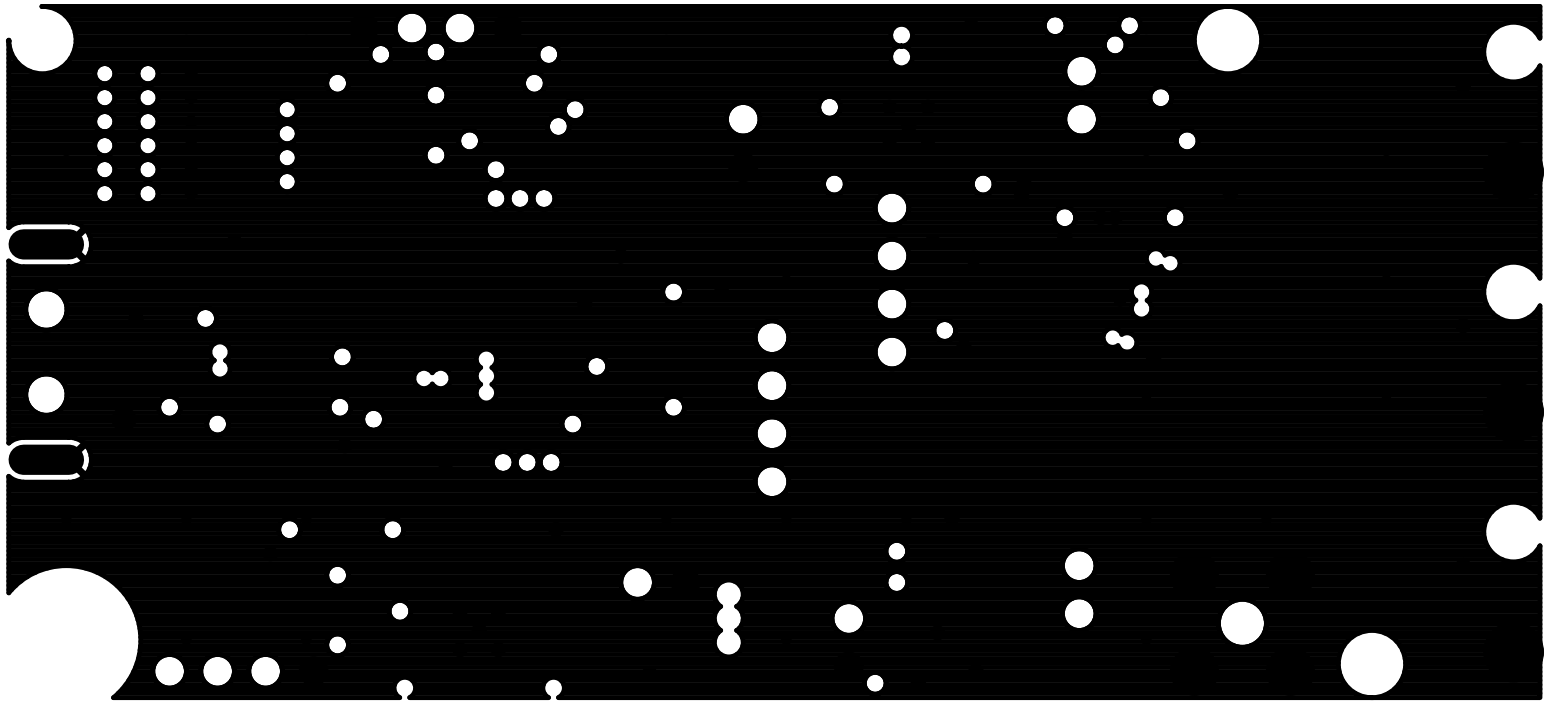
PRIMARY SILKSCREEN



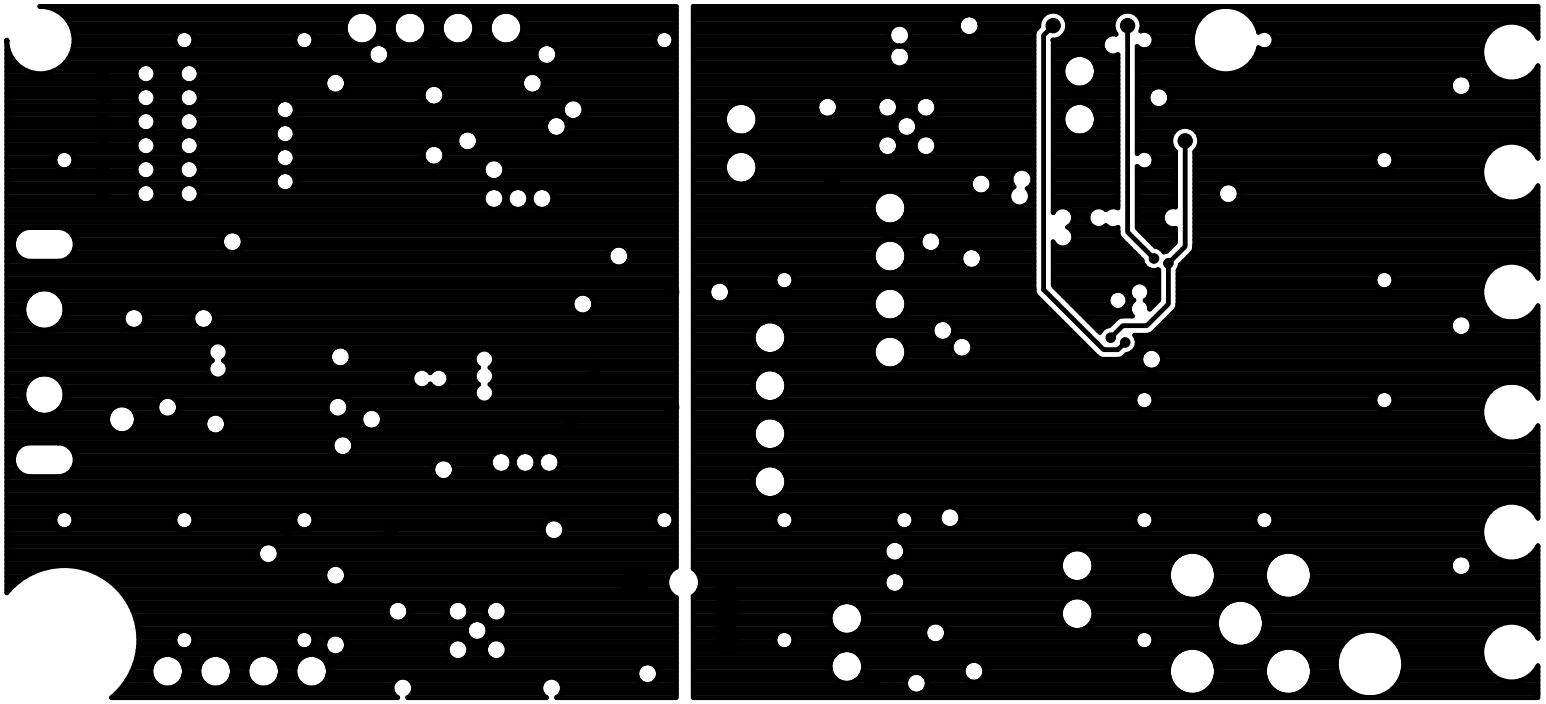
PRIMARY SOLDER MASK



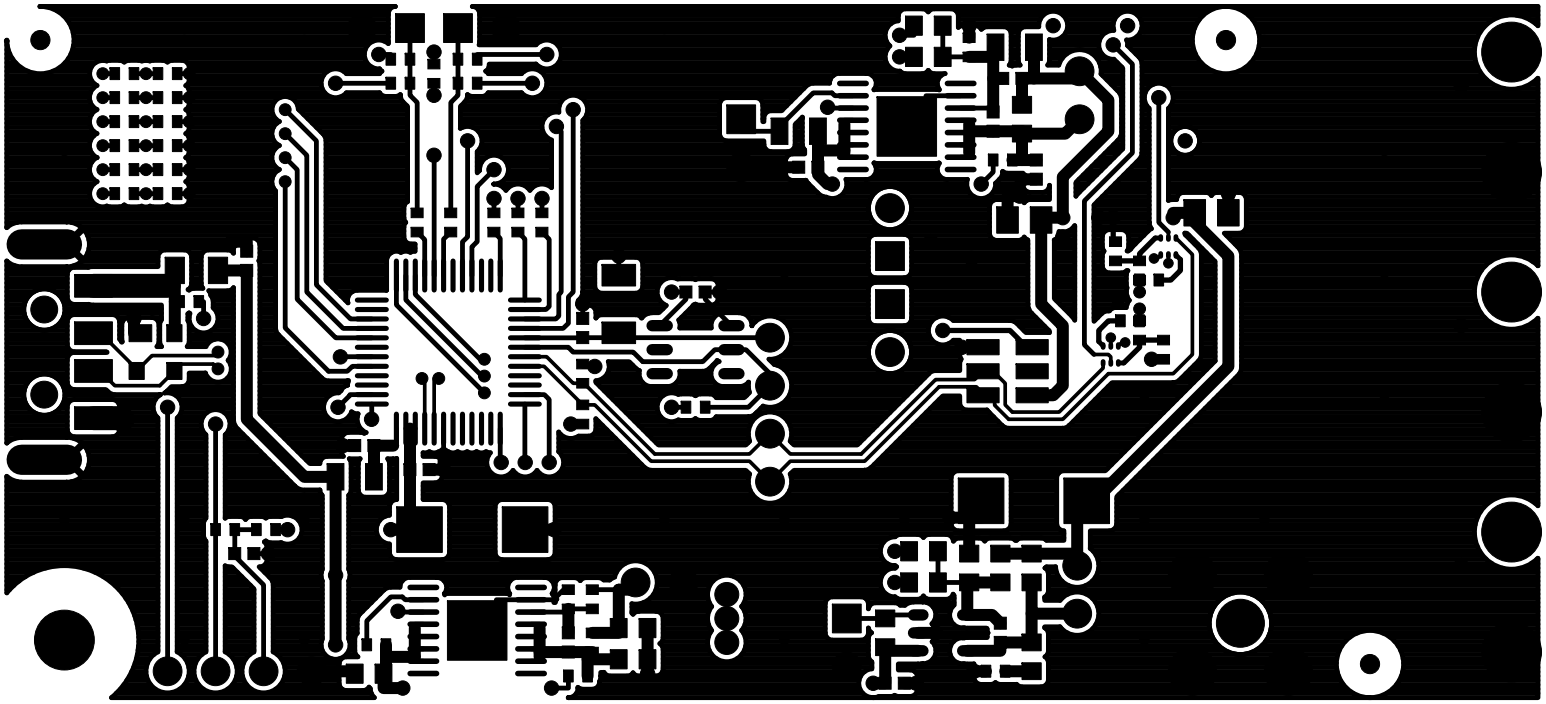
PRIMARY SIDE



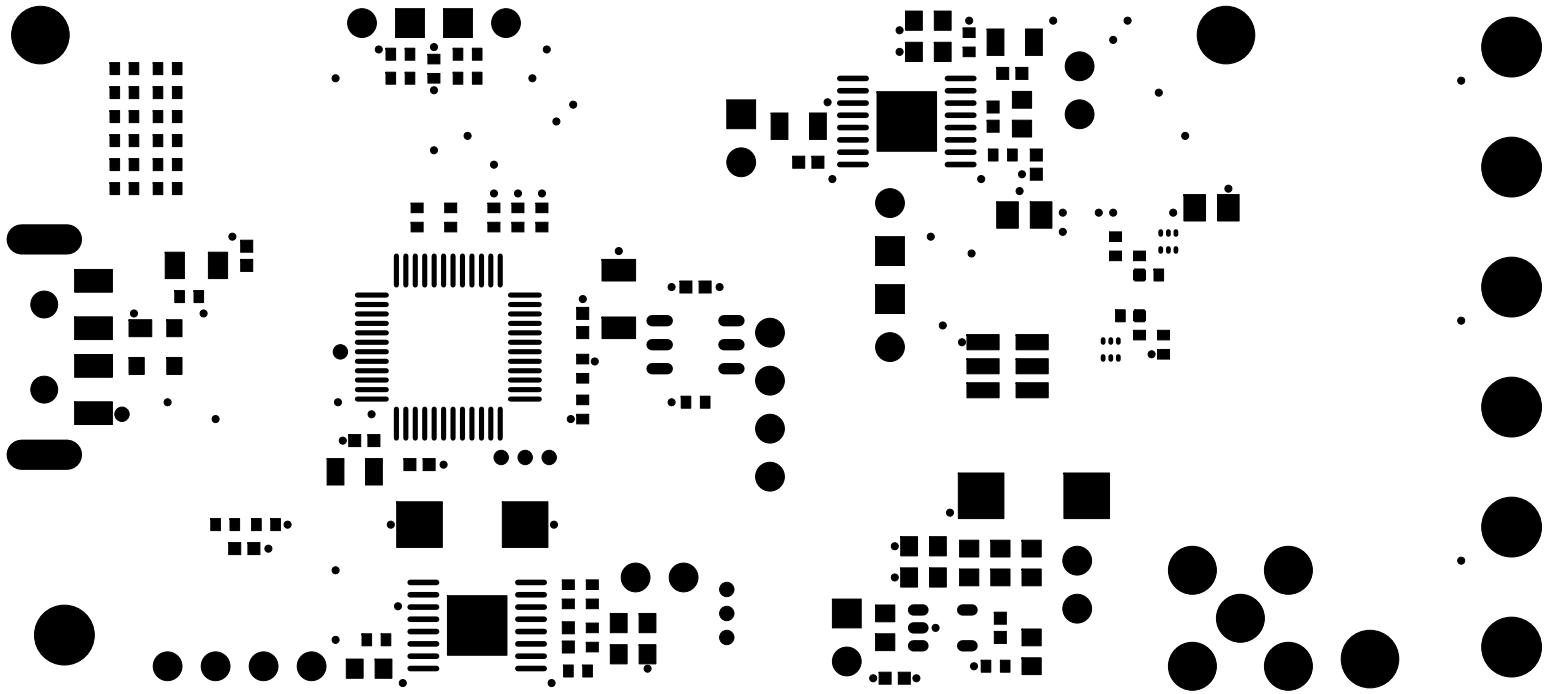
INNER LAYER2



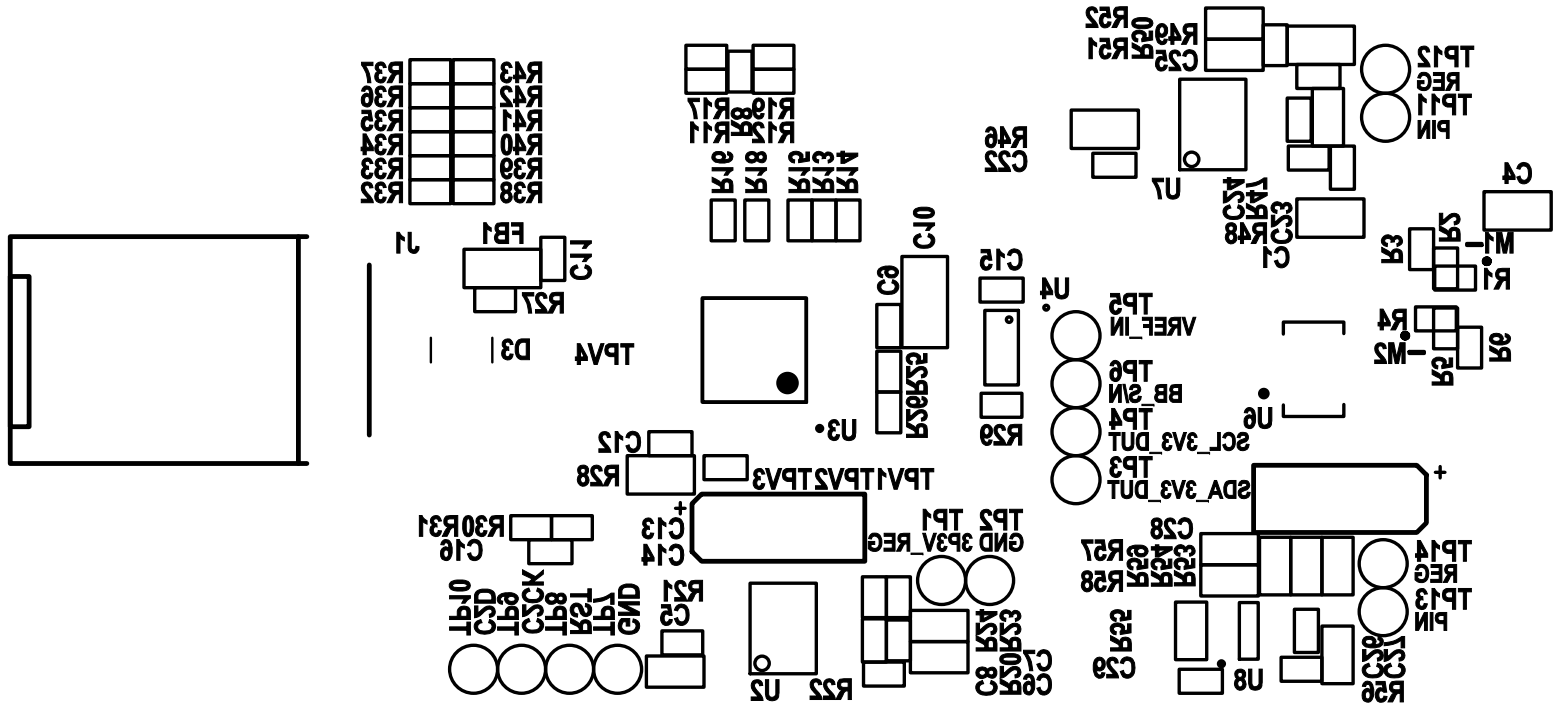
INNER LAYER3



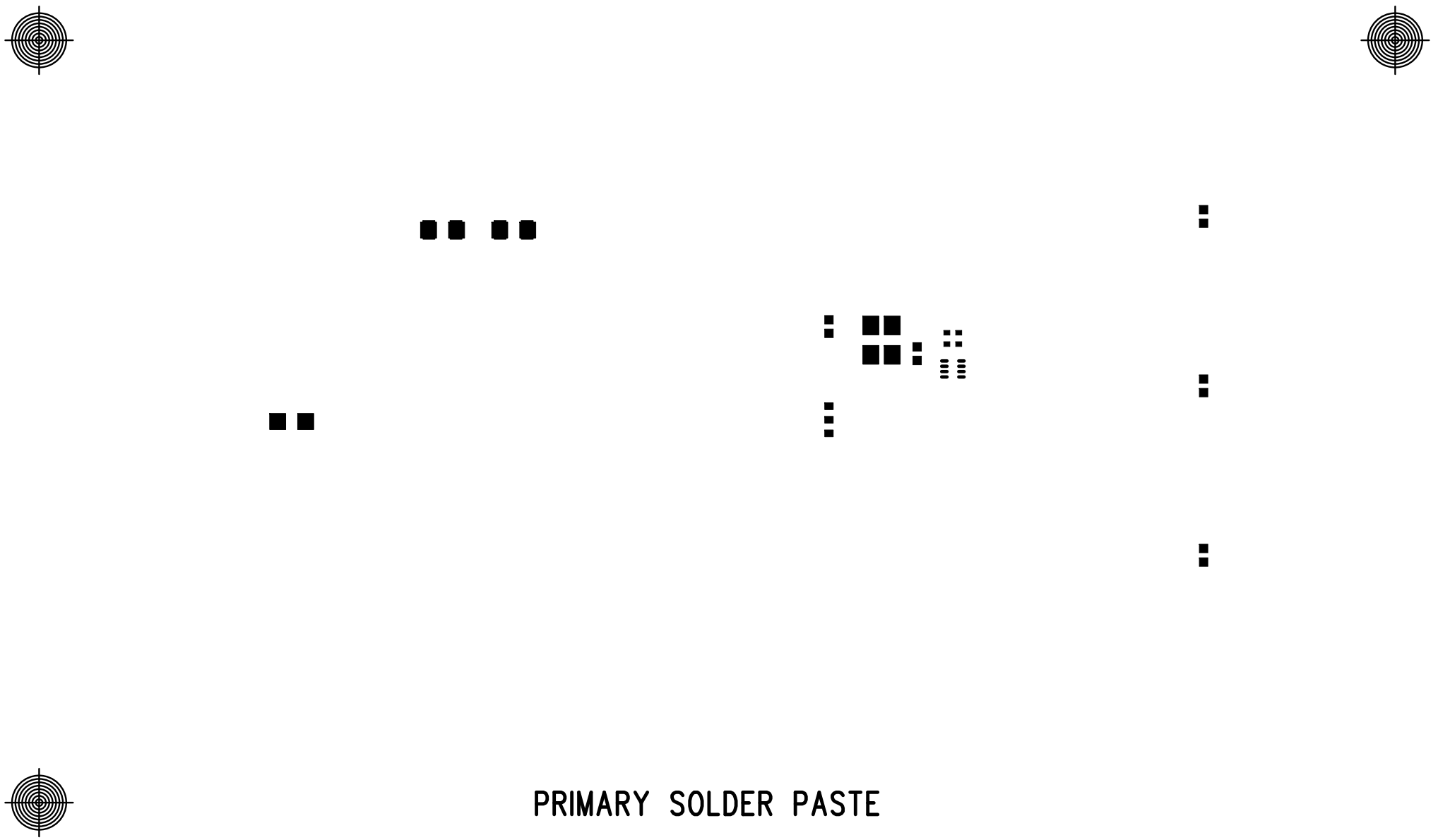
SECONDARY SIDE



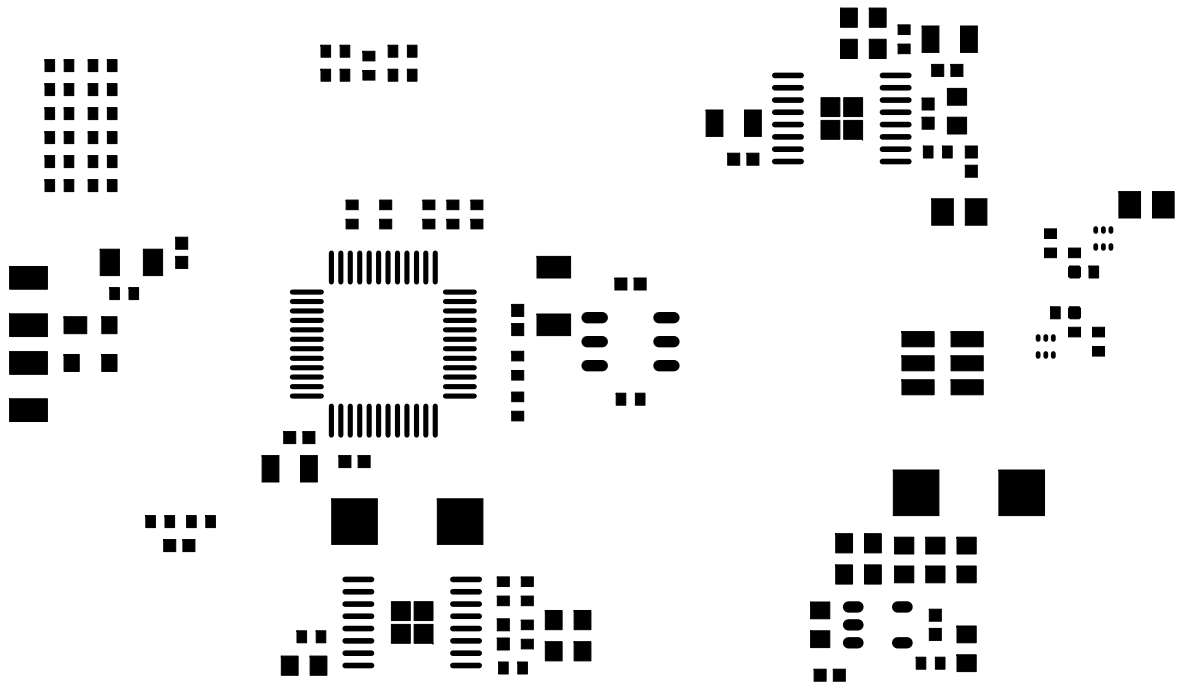
SECONDARY SOLDER MASK



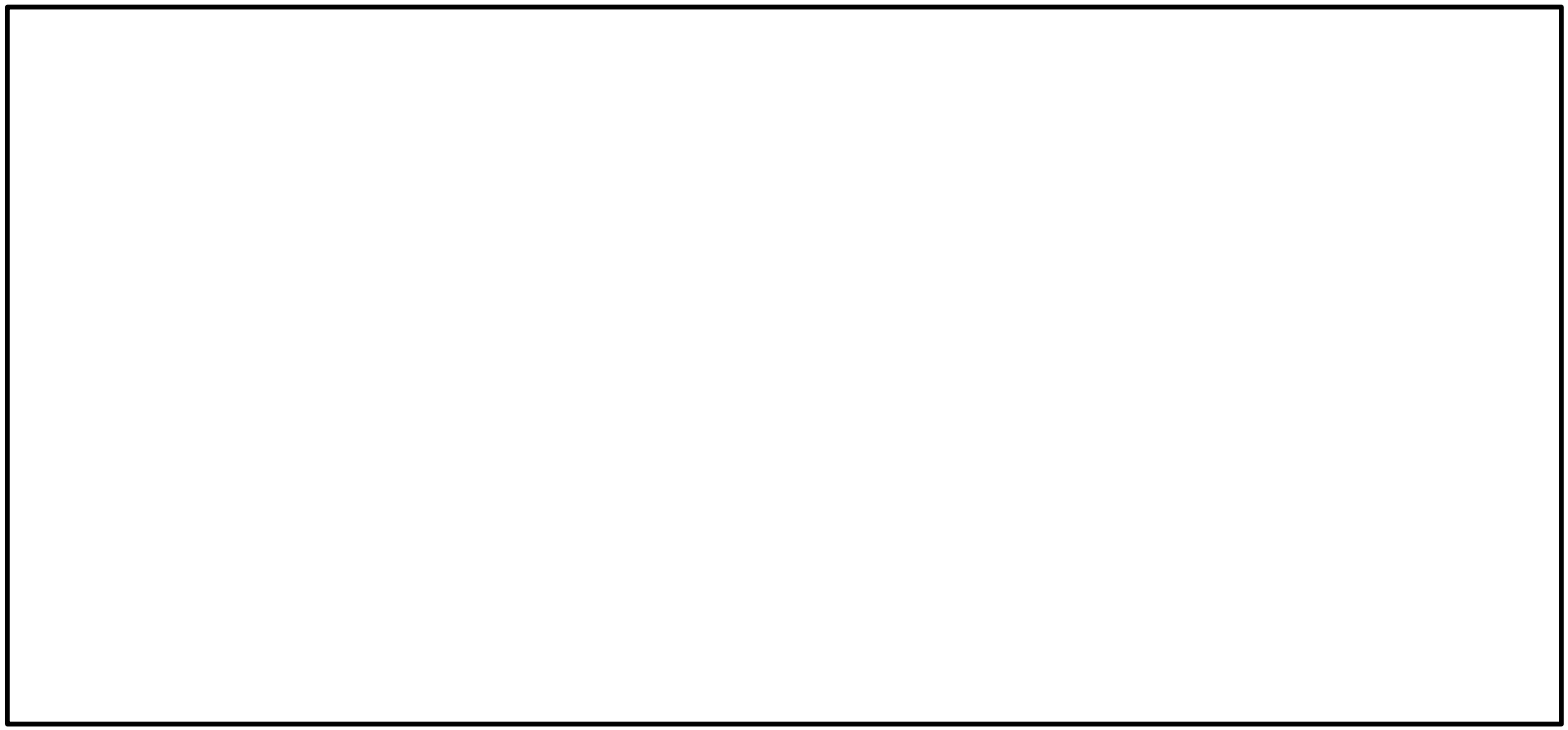
SECONDARY SILKSCREEN

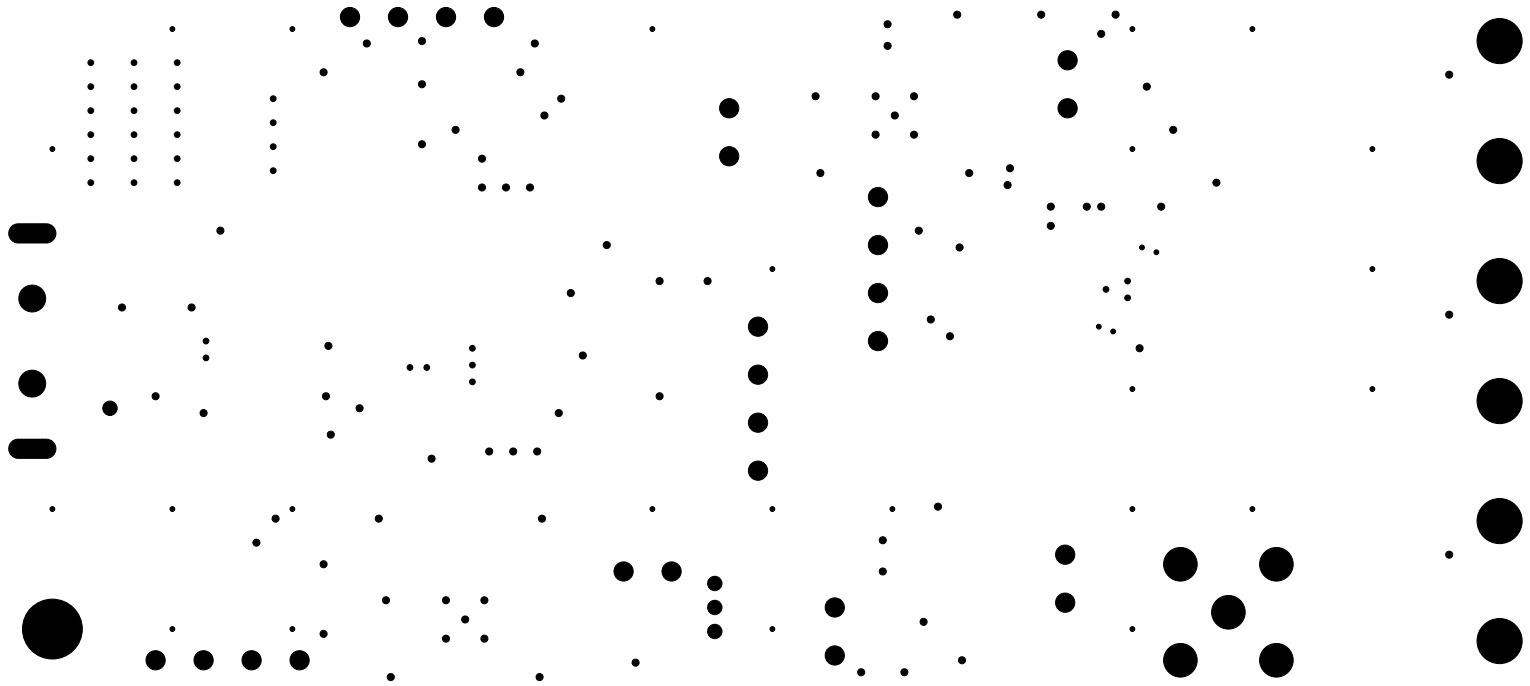


PRIMARY SOLDER PASTE



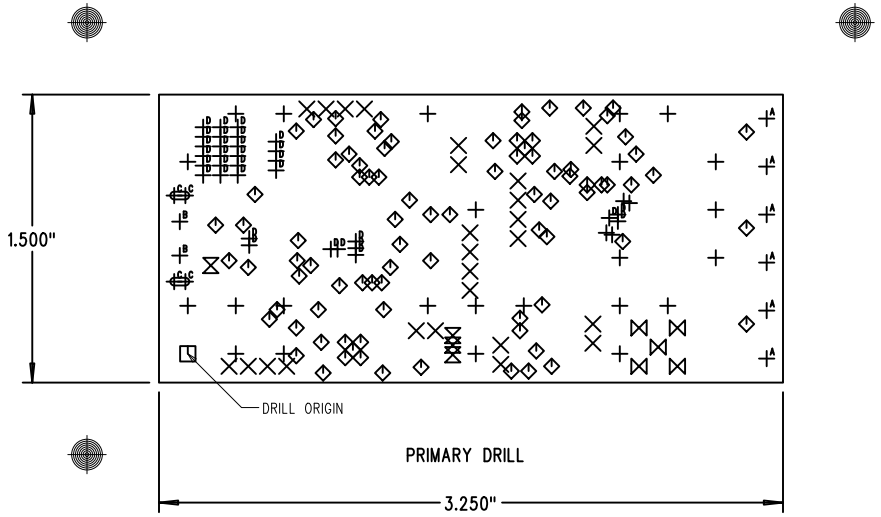
SECONDARY SOLDER PASTE





NOTES : UNLESS OTHERWISE SPECIFIED

1. MANUFACTURE IN ACCORDANCE WITH IPC-6012, TYPE 3, CLASS 2.
2. END PRODUCT FEATURES SHALL NOT VARY MORE THAN 20% FROM ARTWORK ORIGINALS.
3. LAMINATE AND PREPREG SHALL BE AS PER IPC-4101/26,83,98 WITH A DECOMPOSITION TEMPERATURE >= 345°C, COLOR, NATURAL.
4. COPPER WEIGHT SHALL BE 1.0 OZ./SQ. FT. BEFORE PLATING.
5. ALL PLATED THROUGH HOLES SHALL HAVE A MINIMUM OF 0.001" COPPER.
6. DRILL HOLE TOLERANCE AFTER PLATING SHALL BE ±0.003".
7. MINIMUM ANNULAR RING SHALL BE 0.001".
8. MINIMUM ANNULAR RING AT EMERGENT CONDUCTORS SHALL BE 0.003".
9. FINAL PCB THICKNESS SHALL BE 0.062" ±10%.
10. WARP/TWIST SHALL NOT EXCEED 1.0%
11. FINISH SHALL BE LPI, GREEN S.M.O.B.C., BALANCE ENIG.
12. SILKSCREEN WITH NONCONDUCTIVE WHITE EPOXY INK.
13. REFERENCE ADDITIONAL FAB NOTES IN FILE README.TXT



DO NOT ADJUST SPECIFIED GEOMETRIES WITHOUT APPROVAL FROM SILICON LABS.

GERBER FILENAME	LAYER	SINGLE ENDED IMPEDANCE: IMPEDANCE (OHMS)	SINGLE ENDED IMPEDANCE: TRACE WIDTH (INCH)	DIFFERENTIAL IMPEDANCE: IMPEDANCE (OHMS)	DIFFERENTIAL IMPEDANCE: TRACE WIDTH (INCH)	DIFFERENTIAL IMPEDANCE: TRACE GAP (INCH)	BASE COPPER WEIGHT (AFTER PLATING)	THICKNESS (INCH)
5121x_PSS.PHO	PRIMARY SILKSCREEN							
5121x_PSM.PHO	PRIMARY SOLDER MASK							
5121x_PRI.PHO	L01 PRIMARY (Signal)	50	0.011	–	–	–	2.0 oz	0.008
	FR-406							
5121x_L02.PHO	L02 PLANE (Gnd)						0.5 oz	0.040
	FR-406							
5121x_L03.PHO	L03 PLANE (Gnd/Pwr)						0.5 oz	0.008
	FR-406							
5121x_SEC.PHO	L04 SECONDARY (Signal)	50	0.011	–	–	–	2.0 oz	0.062"
5121x_SSM.PHO	SECONDARY SOLDER MASK							
5121x_SSS.PHO	SECONDARY SILKSCREEN							

SIZE	QTY	SYM	PLATED	TOL
0.01	28	+	YES	+/-0.0
0.04	26	X	YES	+/-0.0
0.125	1	□	NO	+/-0.0
0.015	88	◇	YES	+/-0.0
0.03	4	⧖	YES	+/-0.0
0.07	5	⋈	YES	+/-0.0
0.094	6	+A	YES	+/-0.0
0.056	2	+B	NO	+/-0.0
0.04 x 0.09843	2	+C	YES	+/-0.0
0.012	32	+D	YES	+/-0.0

UNLESS OTHERWISE SPECIFIED

DIMENSIONS ARE IN INCHES AND APPLY AFTER FINISH
DIMENSIONS IN BRACKETS [ ] ARE IN MILLIMETERS
INTERPRET DRAWING PER MIL-D-1000

TOLERANCES

HOLE TOLERANCES PER 78027

DECIMALS	ANGLES	SURFACES
.XX +/- .XXX +/-	+/-	MICROINCHES

PART TO BE FREE OF BURRS

BREAK EDGES	BEND RADIUS	BEND RELIEF
MAX	MAX	MAX

DESIGN	HS	15JAN2016
LAYOUT	AA	15JAN2016

DO NOT SCALE DRAWING

COMPANY: SILICON LABS
400 W Cesar Chavez
AUSTIN, TX 78701
(512)416-8500
www.silabs.com

NAME: Si5121x-EVB

REV : 1.0

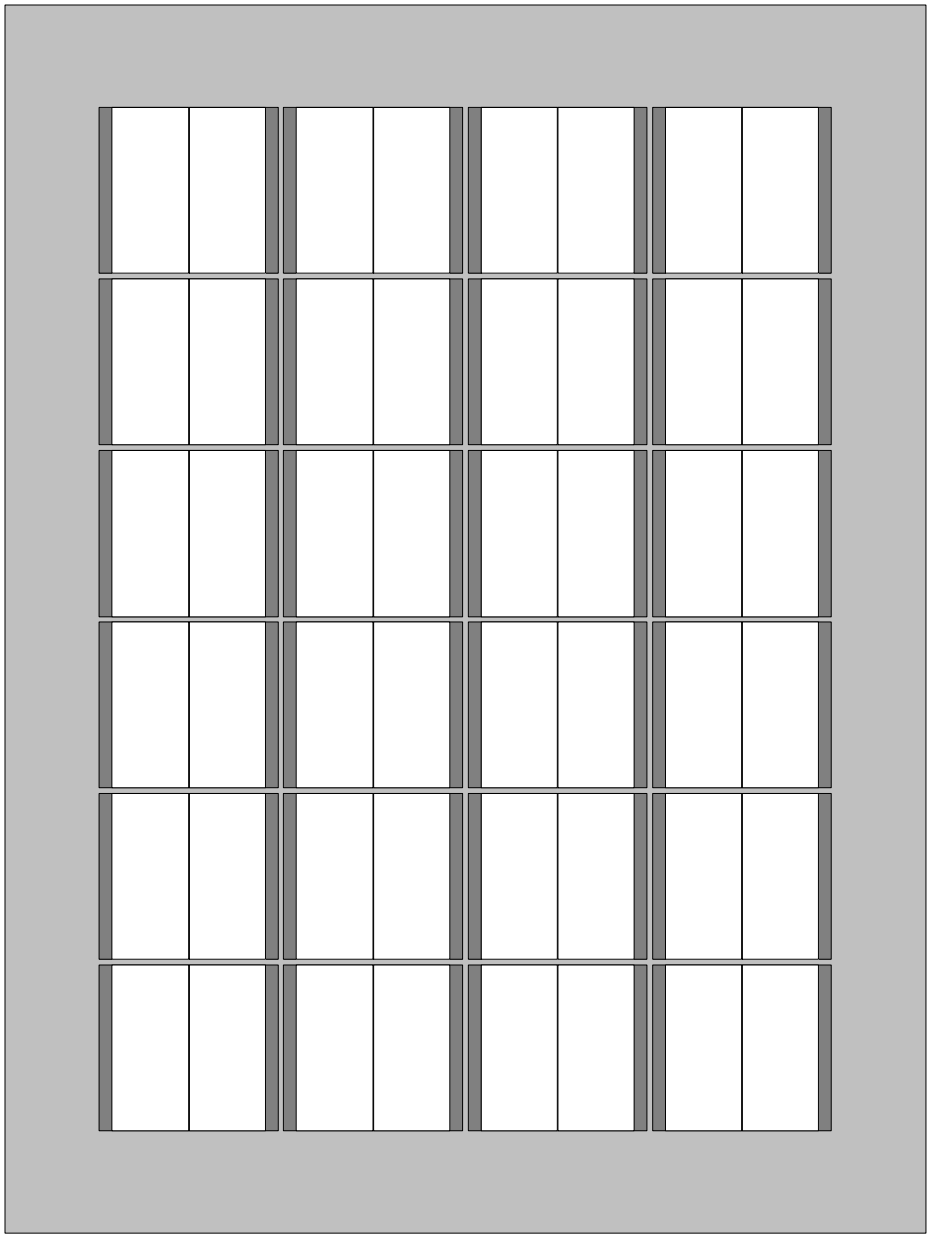
SIZE A

PART NUMBER: .

SCALE 1:1

FABRICATION DRAWING

SHEET 1 OF 1



Si5121x-EVB Rev1.0

Size:
Panel: 18.0 x 24.0
Array: 3.5 x 3.25
Part: 1.5 x 3.25

Panel Yield:
24 Arrays of 2 Parts
48 Parts Total
63.2% Material Utilization

Matrix:
On Panel: 4 x 6, Origin: X1.85 Y2.0
On Array: 2 x 1

Spacing:
On Panel: 0.1 x 0.1
On Array: 0.0 x 0.0

Panel Borders:
Left: 1.85 Right: 1.85
Top: 2.0 Bottom: 2.0

Array Borders:
Left: 0.25 Right: 0.25
Top: 0.0 Bottom: 0.0

Notes:

Please add 4, 0.128" NP tooling holes located 0.125" from tab corners and 3, 40/120 fiduals to array, located 0.25" from tooling holes.
Score PCB as well.