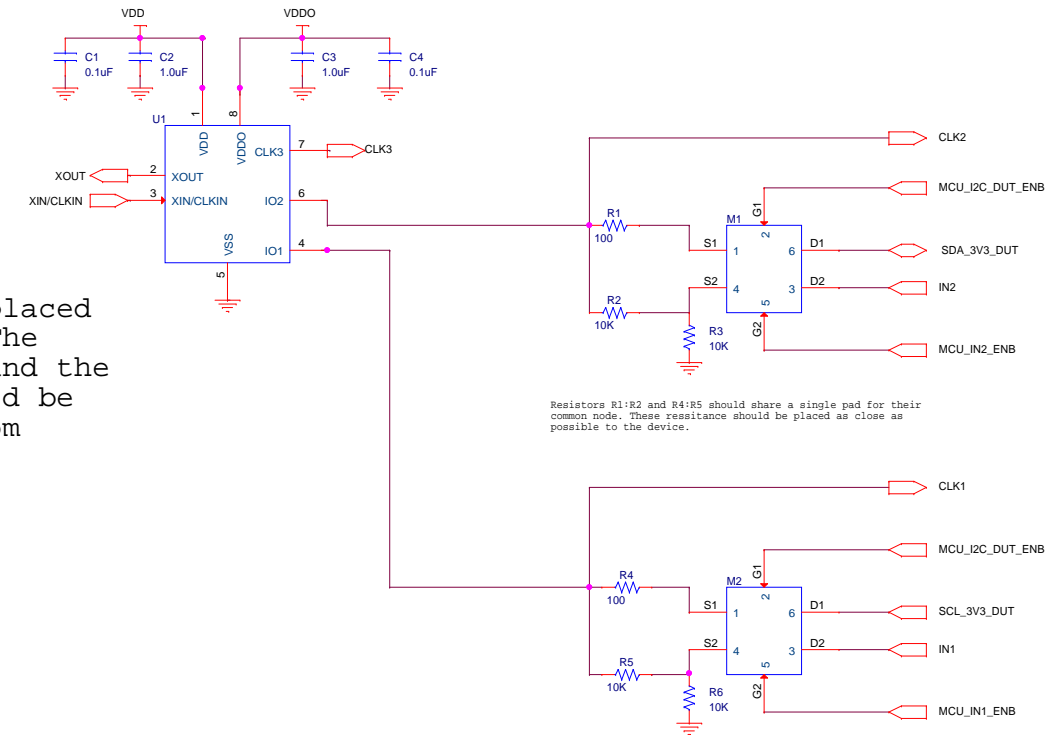
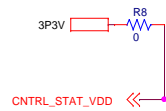


Place the 0.1uF and 1uF capacitances as close as possible to the supply pins and on the top layer

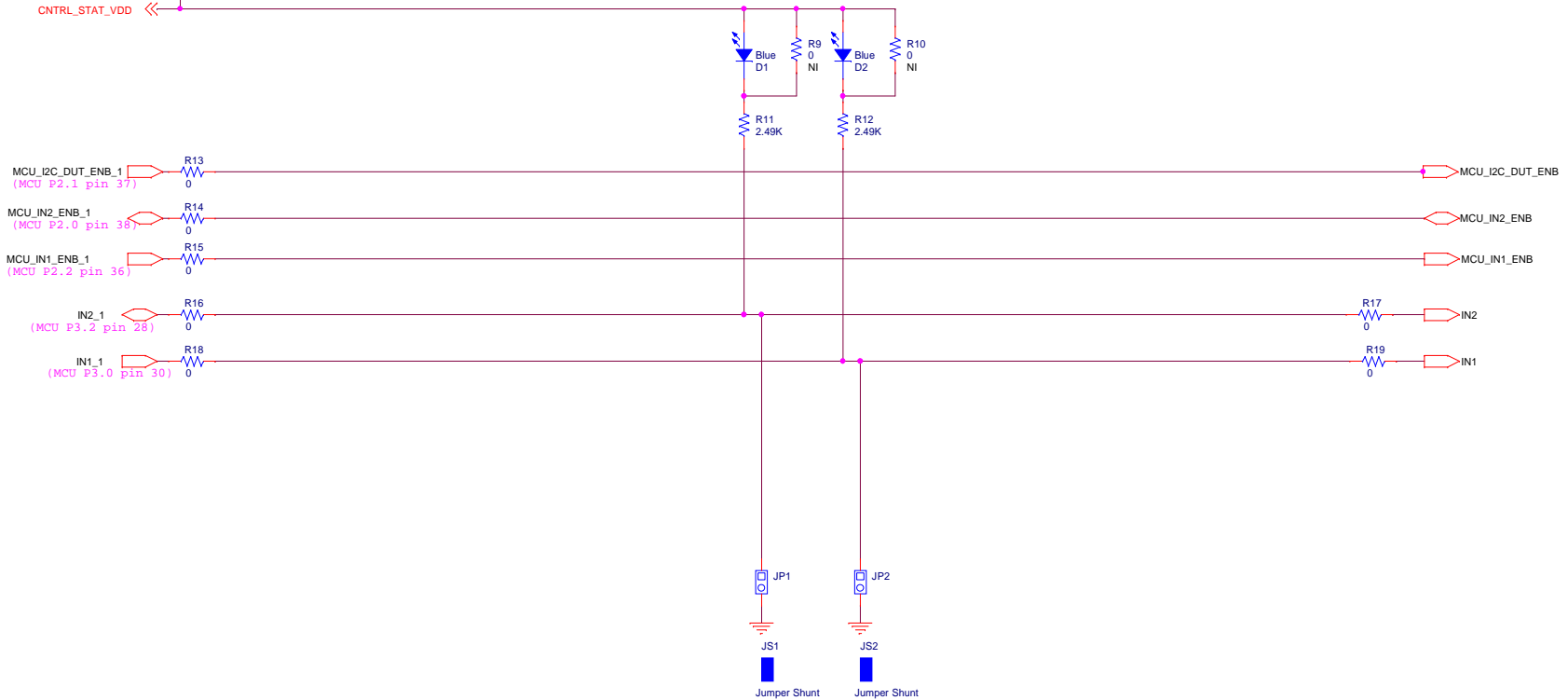


Resistors R1:R2 and R4:R5 should share a single pad for their common node. These resistance should be placed as close as possible to the device.

CONTROL PINS CONNECTIONS



Each LED and the resistor in parallel with it use the same layout pads. Both are never installed at the same time. The LEDs and jumpers JP1,JP2 should appear on the top layer. All other components should be placed in the bottom layer.



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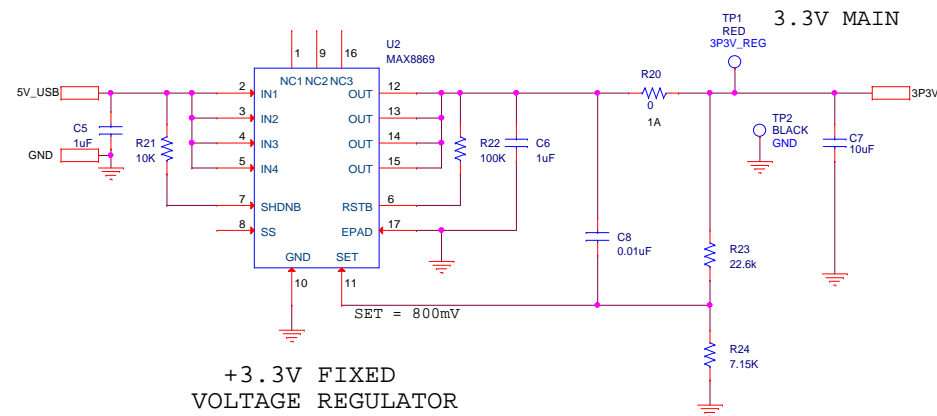
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FIXED +3.3V REGULATOR [3.3V circuitry]

Fixed 3.3V 1A Voltage Regulator



+3.3V FIXED
VOLTAGE REGULATOR

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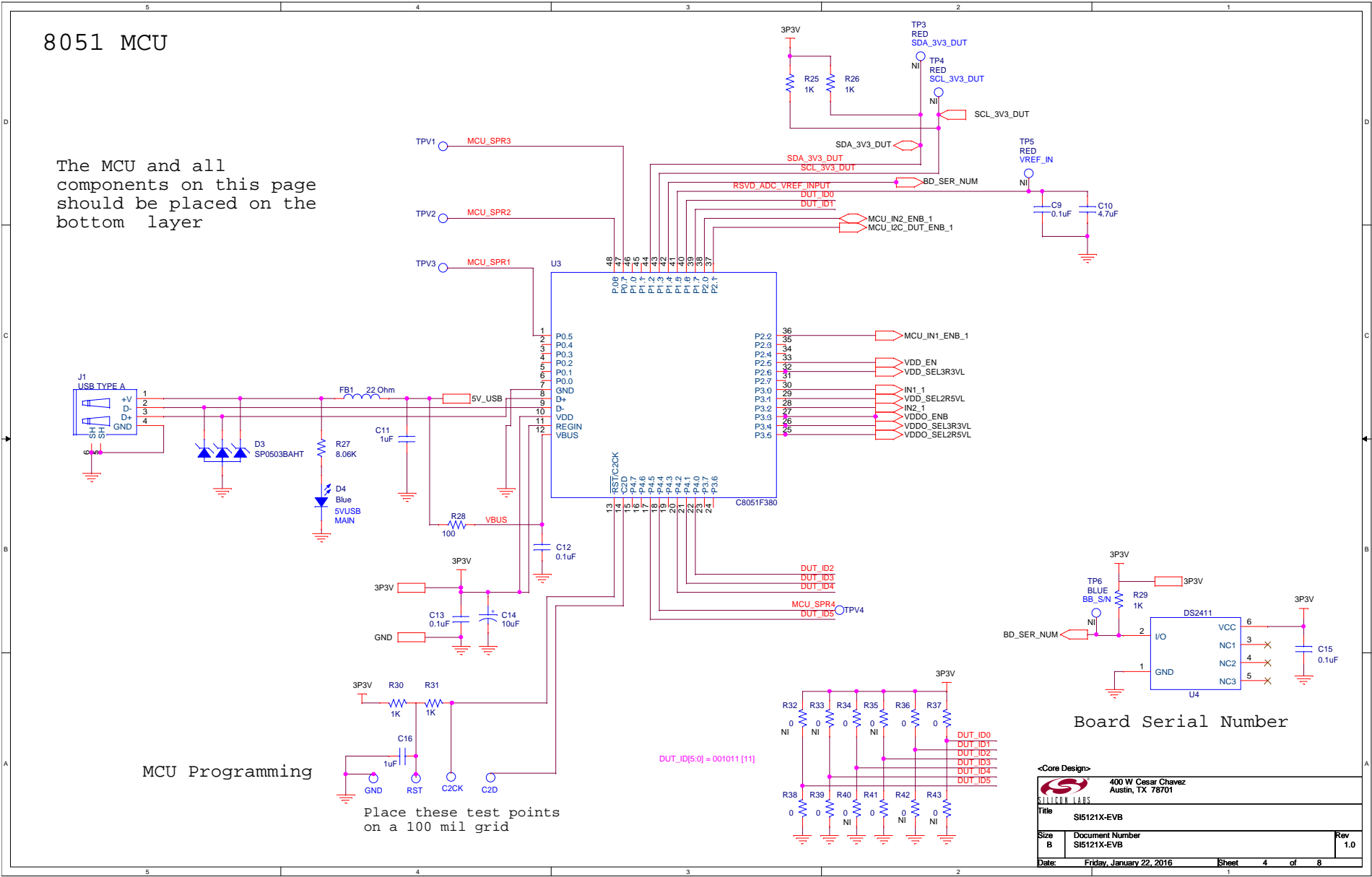
Title SI5121X-EVB

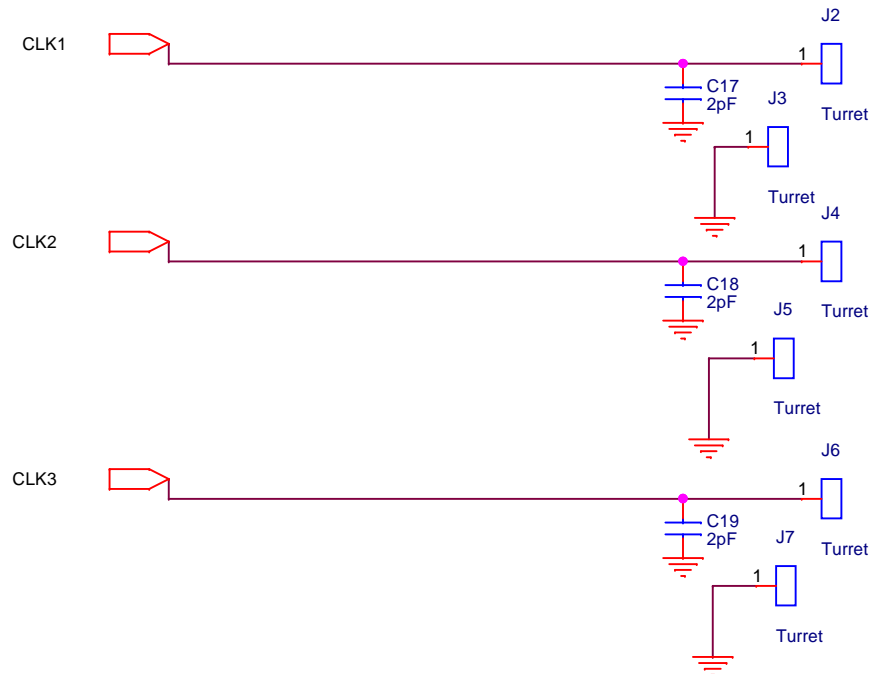
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The output trace length should be 1-2 inches. The test points should be placed after the capacitance load and each output test point should have a ground test point (within a 250 mil distance).

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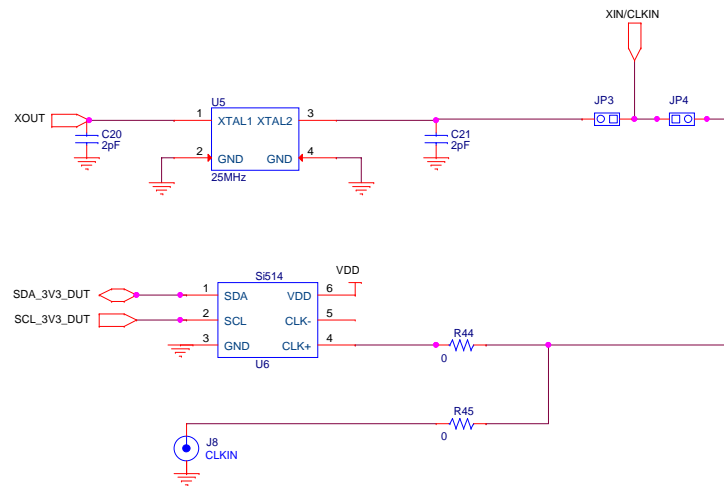
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REFERENCE INPUT CONNECTIONS



The crystal and crystal loads C20, C21 and the jumpers JP3,JP4 should be on the top layer. All other components should be on the bottom layer.

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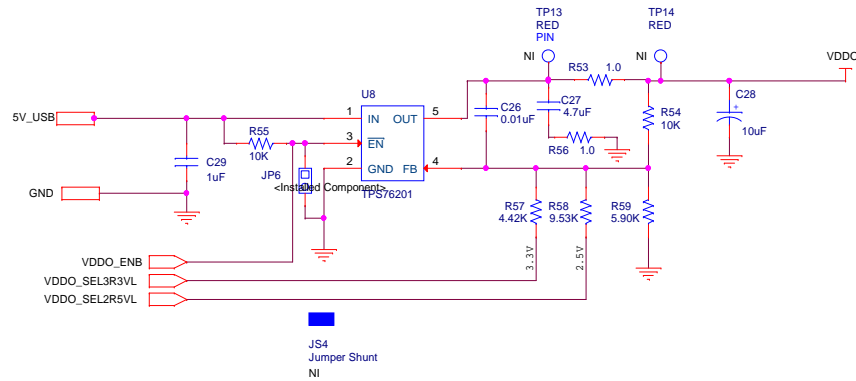
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100 mA Adjustable Voltage Regulator



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