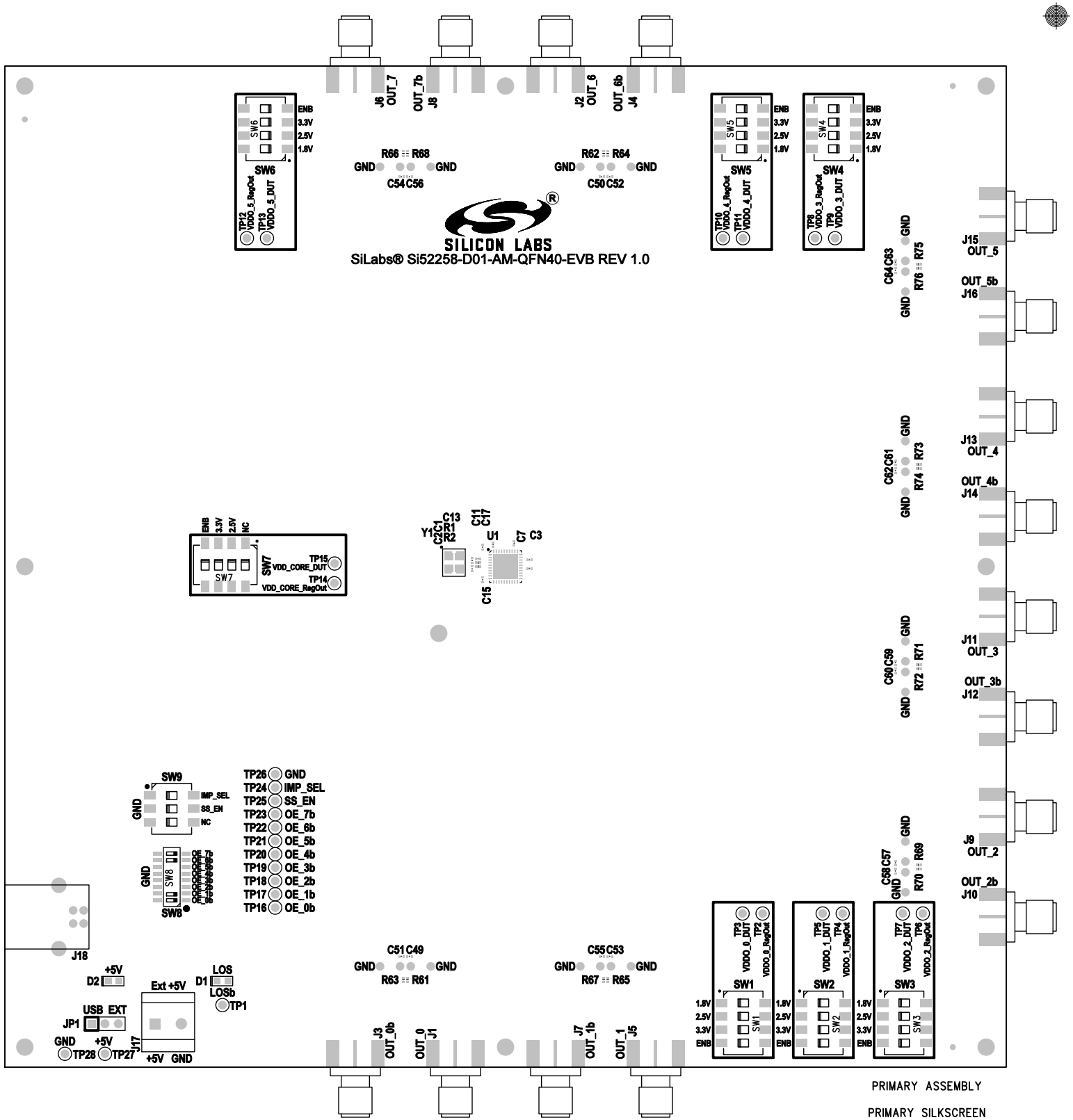
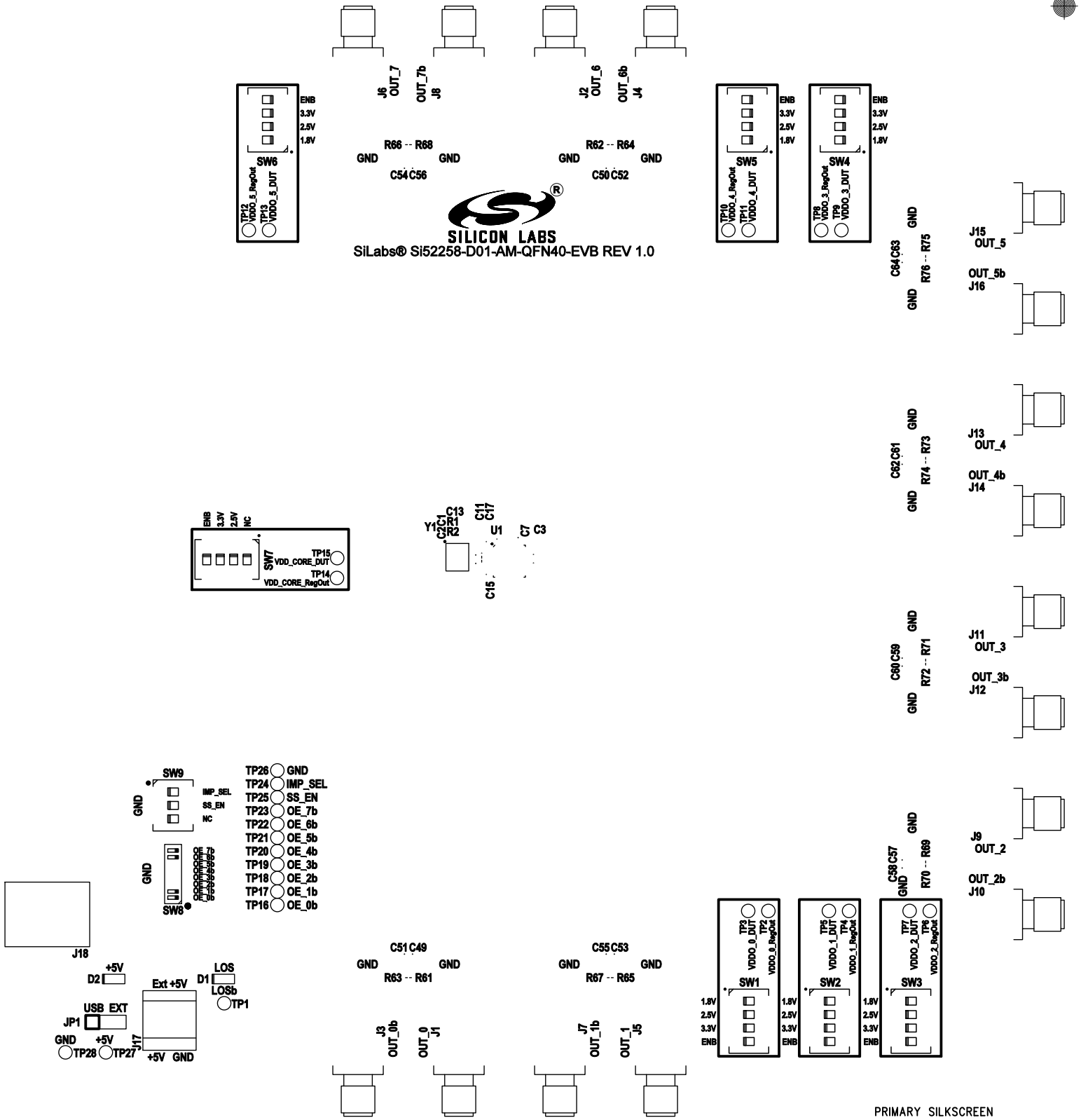


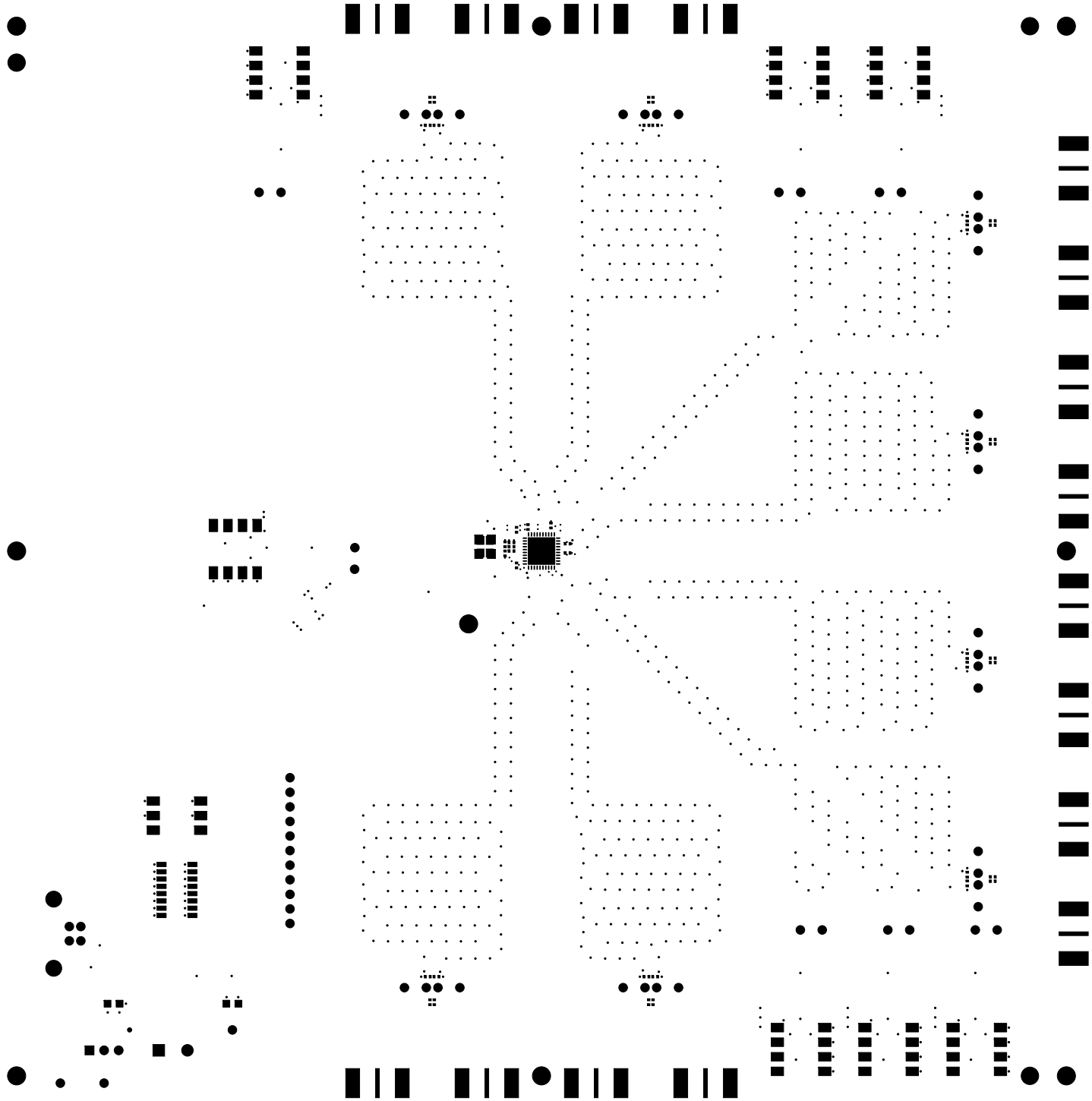
PRIMARY ASSEMBLY

PRIMARY SILKSCREEN

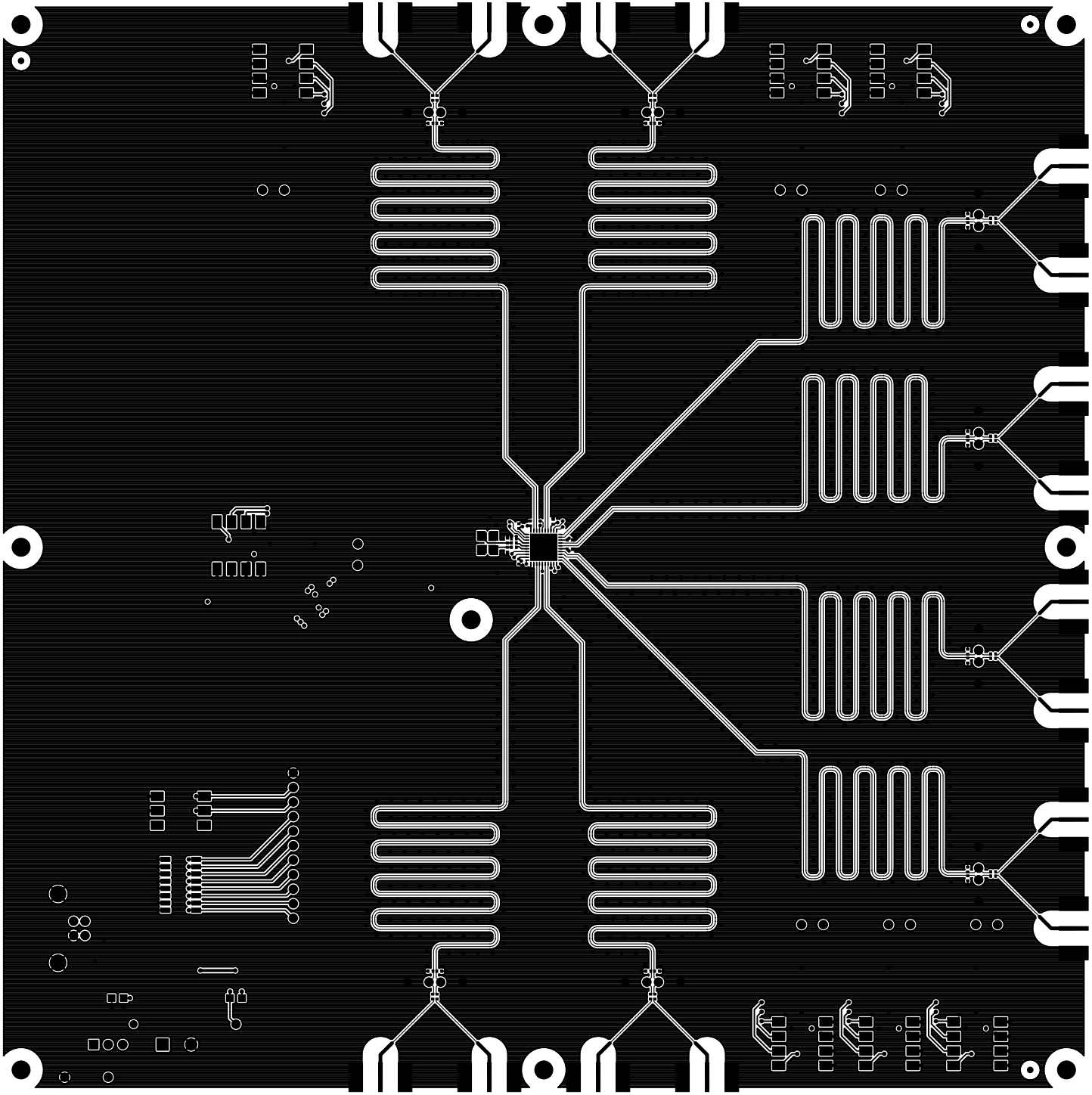
SECONDARY ASSEMBLY

SECONDARY SILKSCREEN

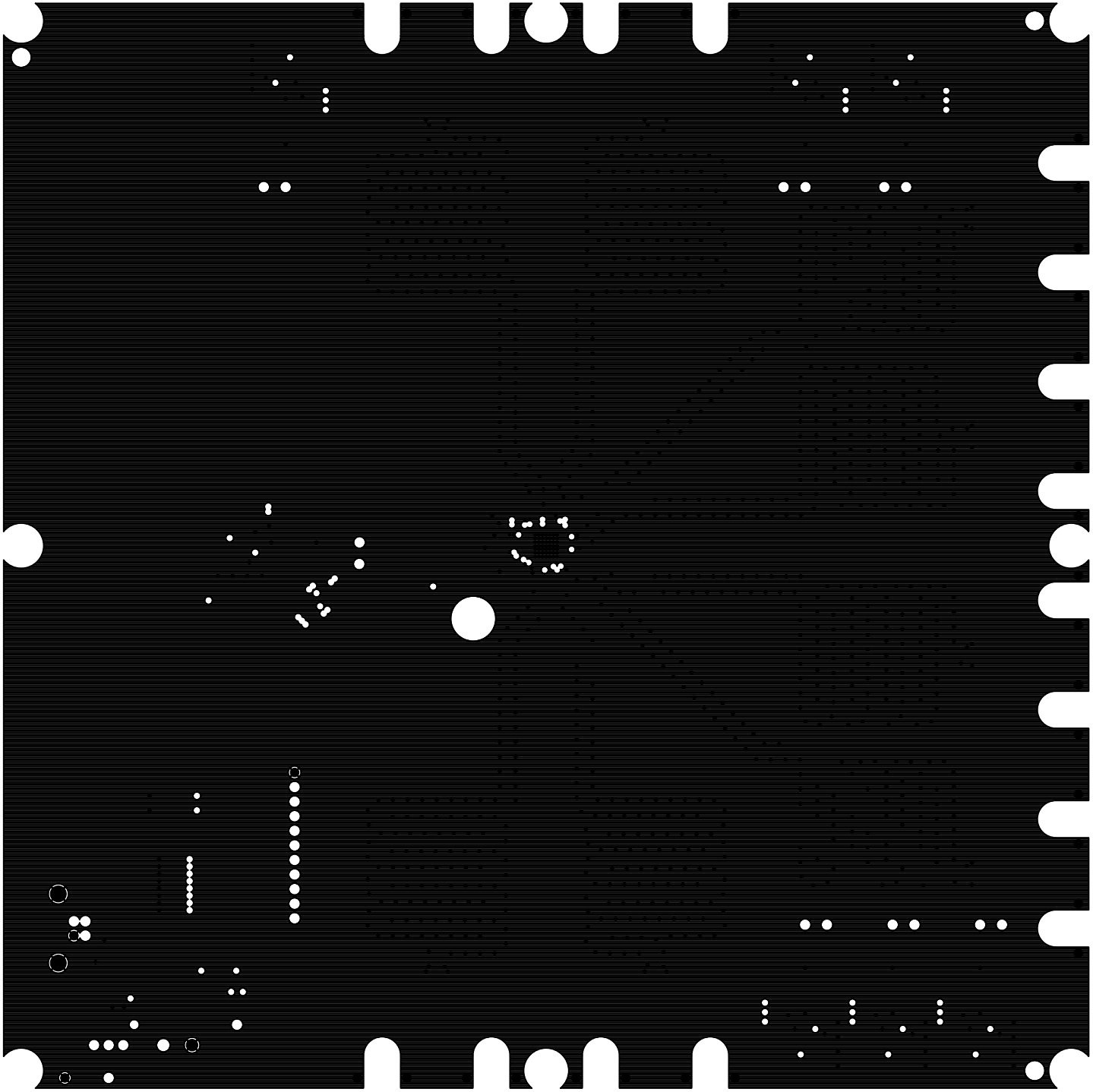

SILICON LABS
SiLabs® Si52258-D01-AM-QFN40-EVB REV 1.0
J6 OUT_7
OUT_7b J8
J2 OUT_6
OUT_6b J4
R66 -- R68
R62 -- R64
GND
C54 C56
C50 C52
SW6
SW5
SW4
ENB
3.3V
2.5V
1.8V
TP12 VDDO_5_RegOut
TP13 VDDO_5_DUT
TP10 VDDO_4_RegOut
TP11 VDDO_4_DUT
TP8 VDDO_3_RegOut
TP9 VDDO_3_DUT
C64 C63
R76 -- R75
J15 OUT_5
OUT_5b J16
C62 C61
R74 -- R73
J13 OUT_4
OUT_4b J14
C60 C59
R72 -- R71
J11 OUT_3
OUT_3b J12
C58 C57
R70 -- R69
J9 OUT_2
OUT_2b J10
SW7
NC
TP15 VDD_CORE_DUT
TP14 VDD_CORE_RegOut
Y1 C2 C9 R1 R2 C13 C1 C11 C17 U1 C7 C3
C15
SW9
IMP_SEL
SS_EN
SW8
TP26 GND
TP24 IMP_SEL
TP25 SS_EN
TP23 OE_7b
TP22 OE_6b
TP21 OE_5b
TP20 OE_4b
TP19 OE_3b
TP18 OE_2b
TP17 OE_1b
TP16 OE_0b
J18
D2 +5V
D1 LOS
LOSb TP1
Ext +5V
USB EXT
JP1
GND TP28 +5V TP27
J17
C51 C49
R63 -- R61
C55 C53
R67 -- R65
J3 OUT_0b
OUT_0 J1
J7 OUT_1b
OUT_1 J5
TP3 VDDO_0_DUT
TP2 VDDO_0_RegOut
TP5 VDDO_1_DUT
TP4 VDDO_1_RegOut
TP7 VDDO_2_DUT
TP6 VDDO_2_RegOut
SW1
SW2
SW3
PRIMARY SILKSCREEN



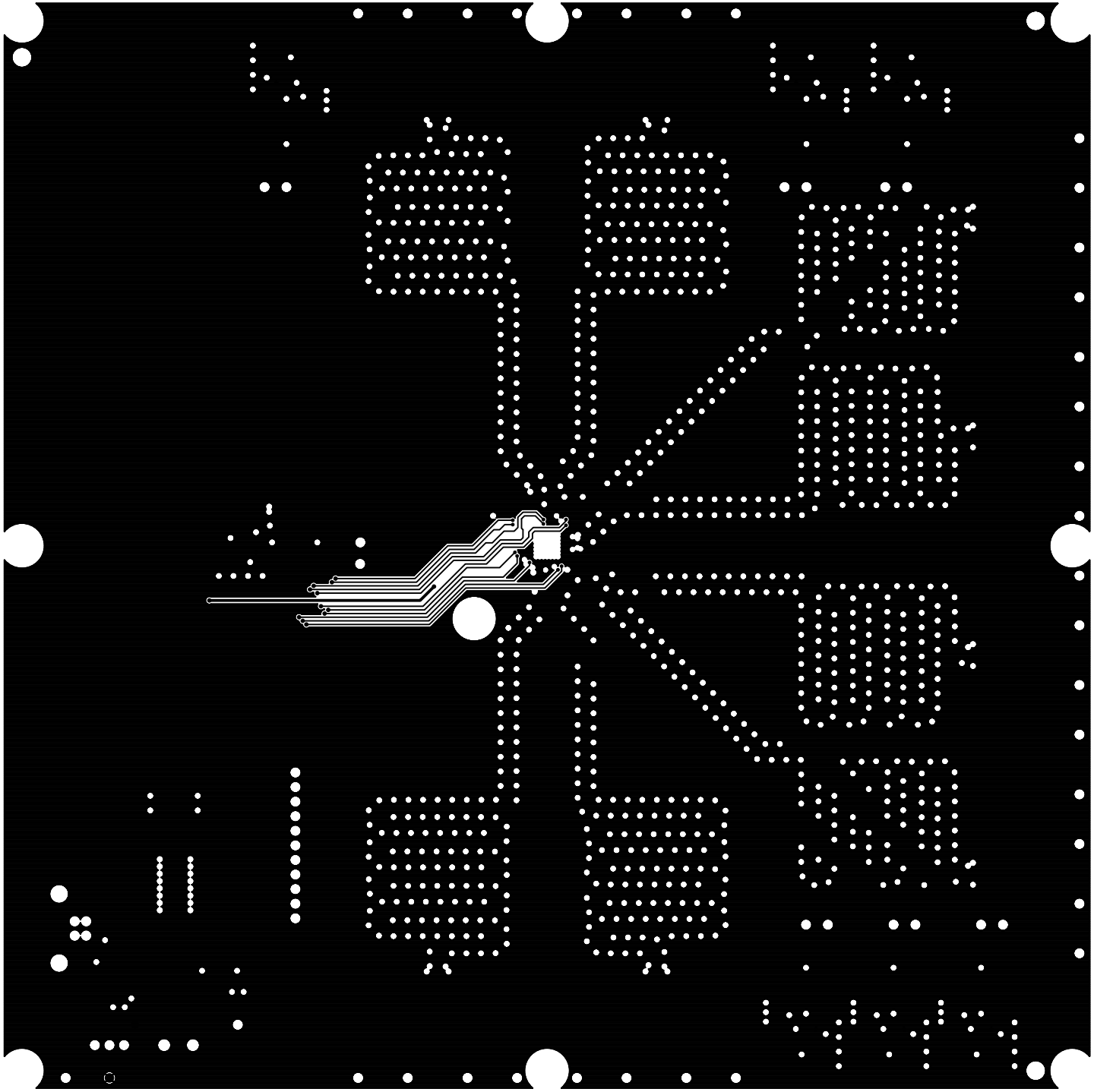
PRIMARY SOLDER MASK



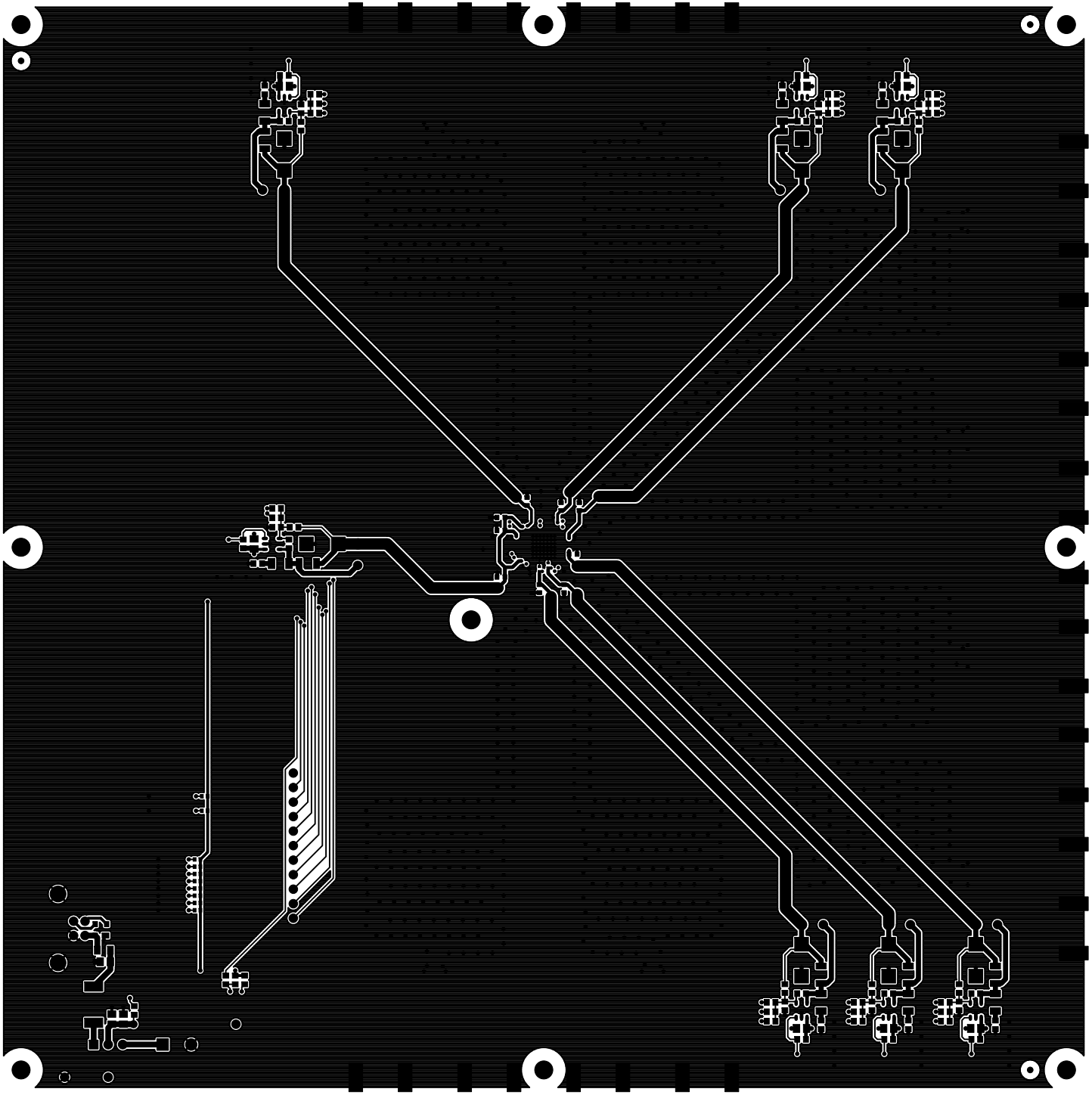
PRIMARY SIDE



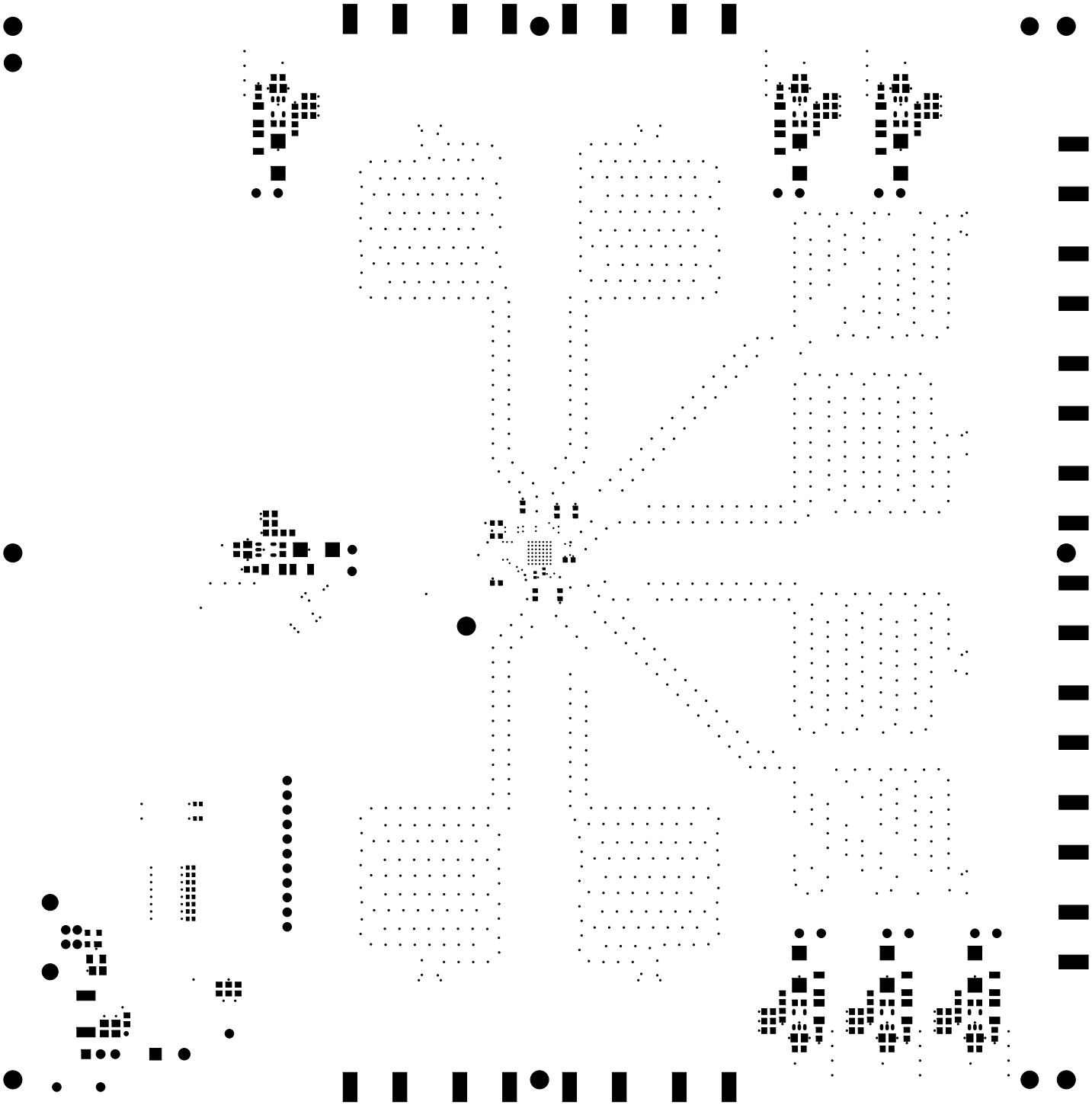
LAYER 02



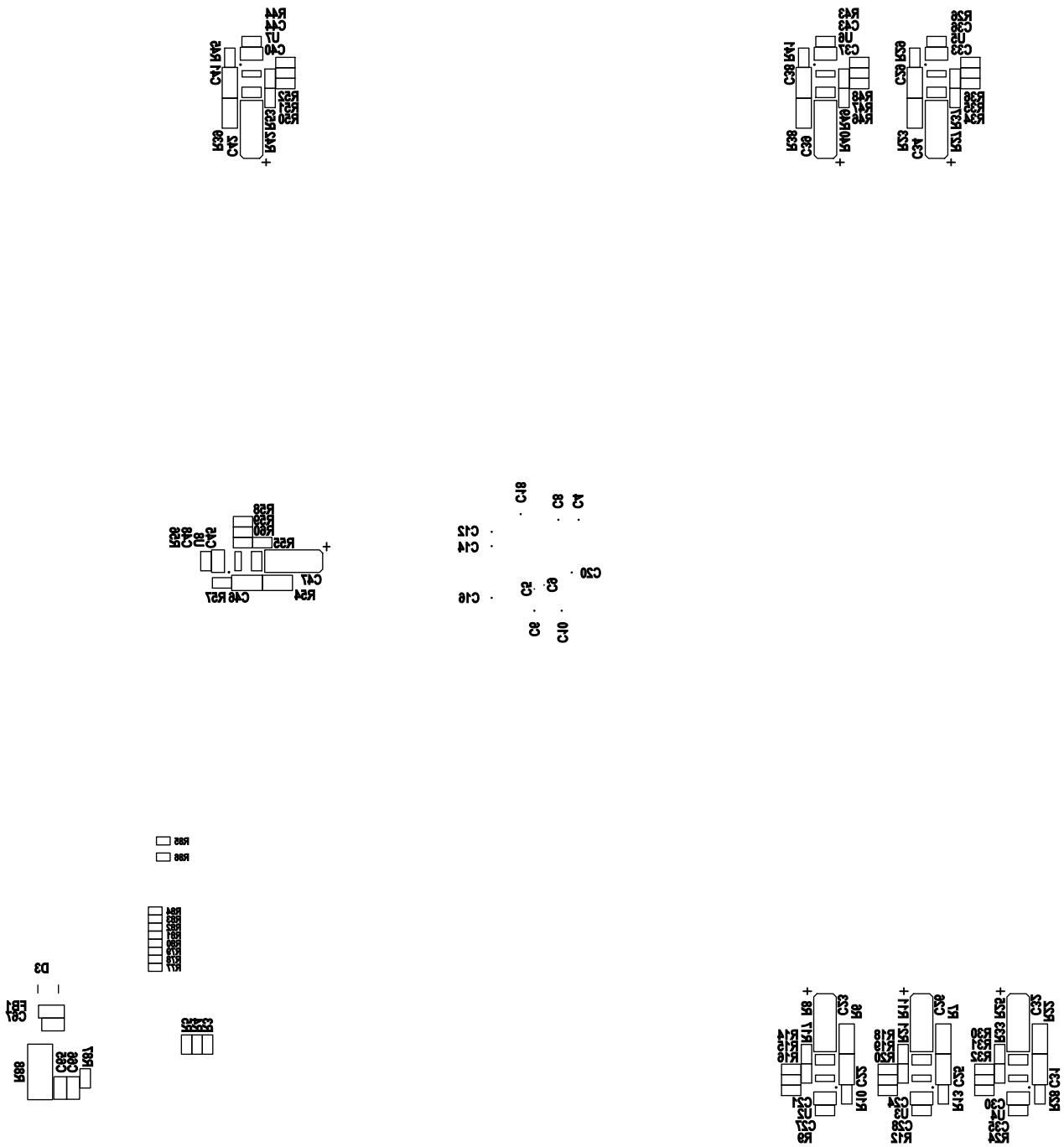
LAYER 03



SECONDARY SIDE



SECONDARY SOLDER MASK


C24
C26
R34
C25
C27
R36
C28
C29
R35
C30
C31
R37
C32
C33
R38
C34
C35
R39
C36
C37
R40
C38
C39
R41
C40
C41
R42
C42
C43
R43
C44
C45
R44
C46
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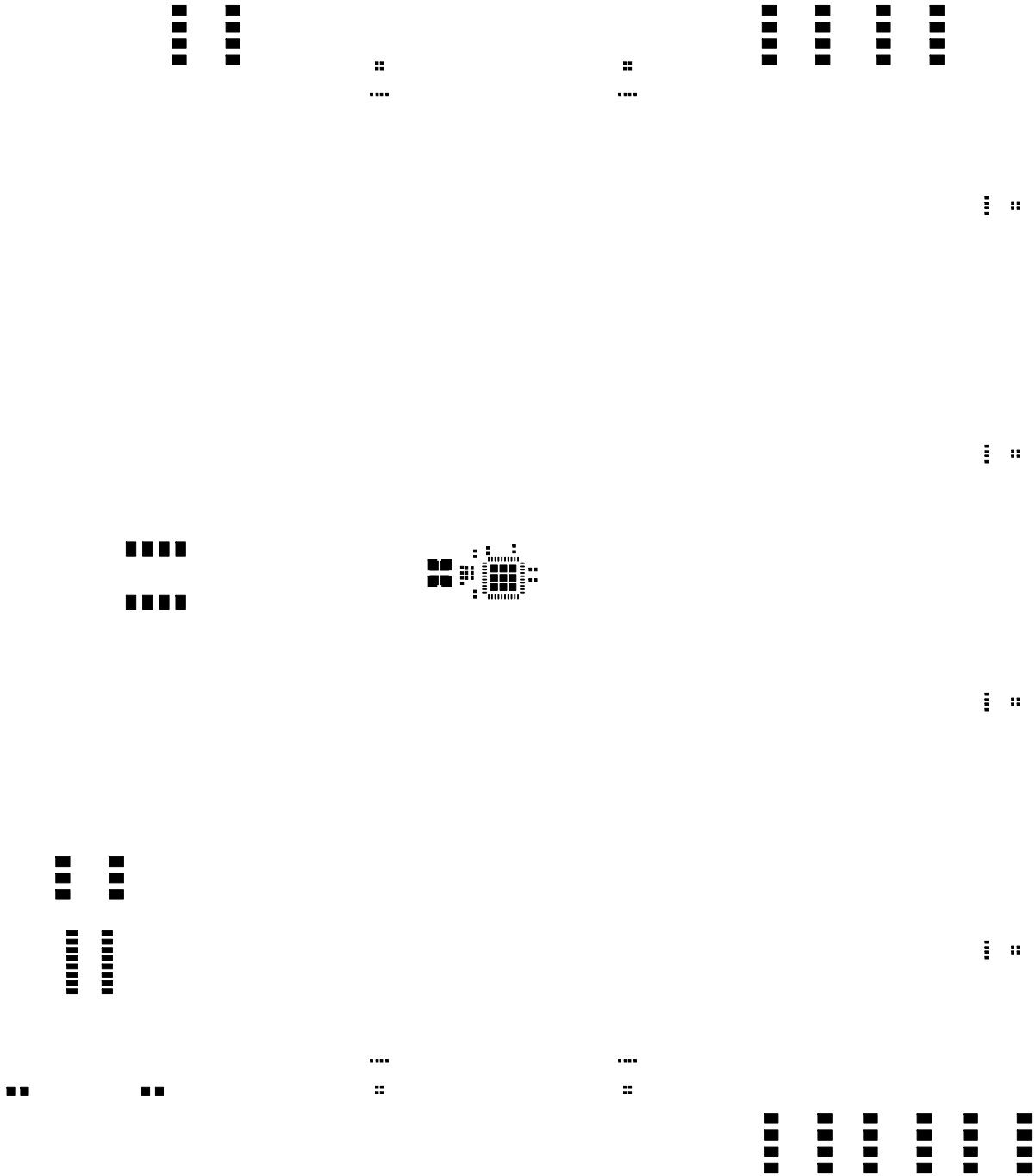
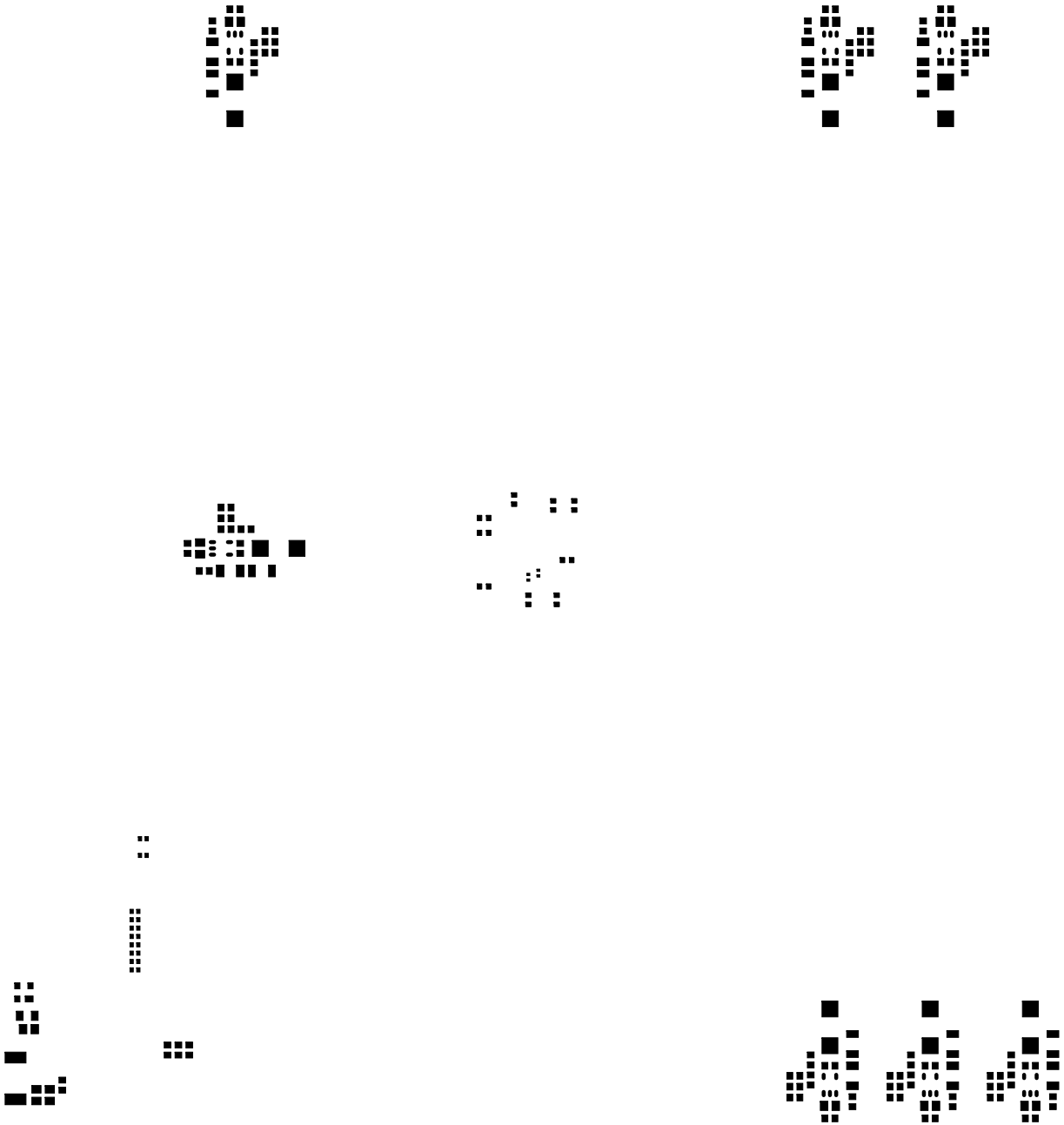
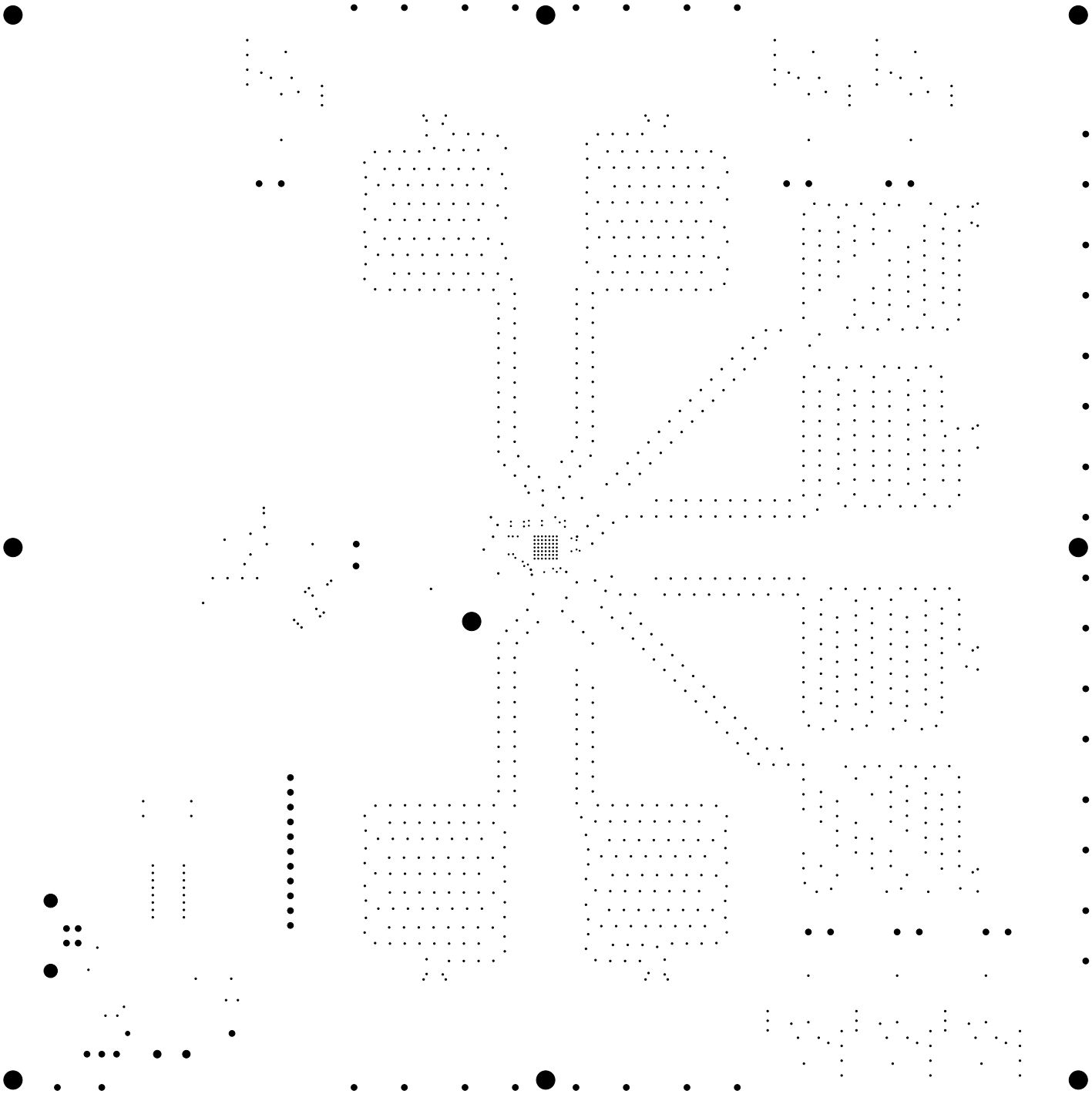
C51
R47
C52
C53
R48
C54
C55
R49

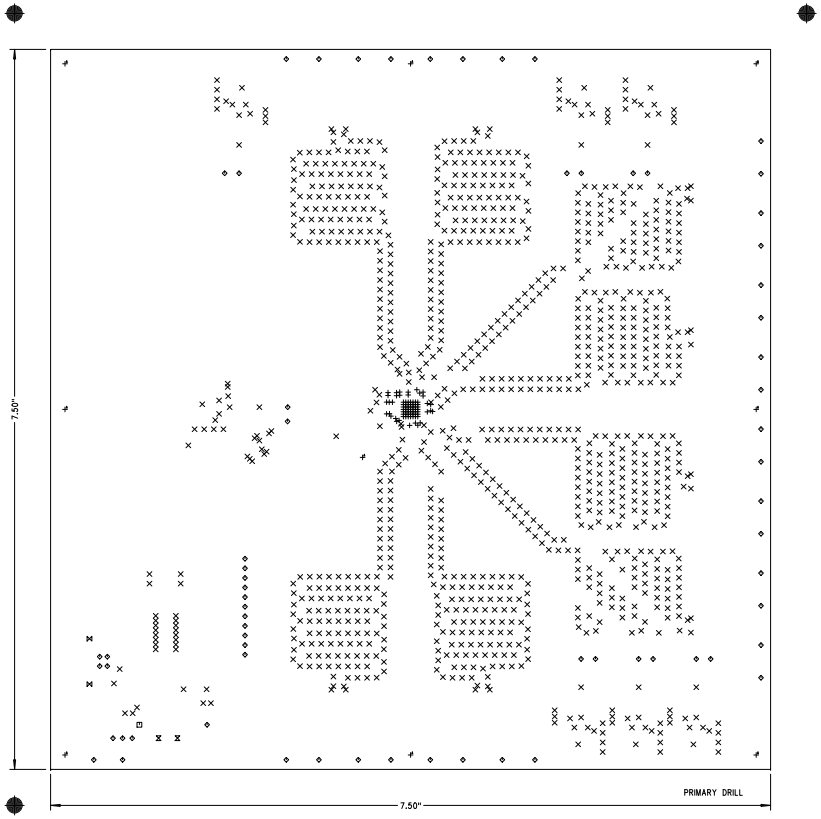


PRIMARY SOLDER PASTE



SECONDARY SOLDER PASTE





NOTES : UNLESS OTHERWISE SPECIFIED

1. MANUFACTURE IN ACCORDANCE WITH IPC-6012, TYPE 3, CLASS 2.
2. END PRODUCT FEATURES SHALL NOT VARY MORE THAN 20% FROM ARTWORK ORIGINALS.
3. LAMINATE AND PREPREG SHALL BE AS PER IPC-4101/26,83,98 WITH A DECOMPOSITION TEMPERATURE >= 345°C, COLOR, NATURAL.
4. COPPER WEIGHT SHALL BE 0.5 OZ./SQ. FT. BEFORE PLATING.
5. ALL PLATED THROUGH HOLES SHALL HAVE A MINIMUM OF 0.001" COPPER.
6. DRILL HOLE TOLERANCE AFTER PLATING SHALL BE ±0.003".
7. MINIMUM ANNULAR RING SHALL BE 0.001".
8. MINIMUM ANNULAR RING AT EMERGENT CONDUCTORS SHALL BE 0.003".
9. FINAL PCB THICKNESS SHALL BE 0.062" ±10%.
10. WARP/TWIST SHALL NOT EXCEED 1.0%
11. FINISH SHALL BE LPI, BLUE SMOBC, ENIG BOTH SIDES.
12. SILKSCREEN WITH NONCONDUCTIVE WHITE EPOXY INK.
13. EXTERNAL 6.0MIL TRACES TO BE 42.5 OHM Zo ±5%.
    EXTERNAL 26MIL TRACES TO BE 42.5 OHM Zo ±5% REF TO L03.

14. VENDOR TO PROVIDE PCB MICRO-SECTION OF COUPON AREA & TDR TEST REPORT.
15. REFERENCE ADDITIONAL FAB NOTES IN FILE README.TXT

LAYER STACKUP	FILE NAMES
PRIMARY SILKSCREEN	52258-D01-AM-QFN40-CEVB_PSS.PHO
PRIMARY SOLDERMASK	52258-D01-AM-QFN40-CEVB_PSM.PHO
PRIMARY SIDE/RF ROUTE	52258-D01-AM-QFN40-CEVB_PRL.PHO
370HR	2.8MIL THK
GROUND PLANE	52258-D01-AM-QFN40-CEVB_L02.PHO
370HR	8MIL THK
PWR PLANE	52258-D01-AM-QFN40-CEVB_L03.PHO
370HR	46.5MIL THK
SECONDARY SIDE	52258-D01-AM-QFN40-CEVB_SEC.PHO
SECONDARY SOLDERMASK	52258-D01-AM-QFN40-CEVB_SSM.PHO
SECONDARY SILKSCREEN	52258-D01-AM-QFN40-CEVB_SSS.PHO

0.062" THK

SCALE: NONE

SIZE	QTY	SYM	PLT	TOOL	TOL
0.008	79	+	P	1	+0/-0.008
0.012	1112	×	P	2	+0/-0.012
0.030	1	□	P	3	+/-0.003
0.040	67	◇	P	4	+/-0.003
0.052	2	⧖	P	5	+/-0.003
0.091	2	⋈	P	6	+/-0.003
0.125	9	A	N	7	+/-0.003

UNLESS OTHERWISE SPECIFIED

DIMENSIONS ARE IN INCHES AND APPLY AFTER FINISH
DIMENSIONS IN BRACKETS [ ] ARE IN MILLIMETERS
INTERPRET DRAWING PER ML-D-1000

TOLERANCES

HOLE TOLERANCES PER 78027

DECIMALS	ANGLES	SURFACES
.XX +/- .XXX +/-	+/-	MICROINCHES

PART TO BE FREE OF BURRS

BREAK EDGES	BEND RADIUS	BEND RELIEF
MAX	MAX	MAX

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DESIGN	TS	02JUL2019
LAYOUT	AA	02JUL2019

DO NOT SCALE DRAWING

COMPANY: SILICON LABS
400 W CESAR CHAVEZ ST.
AUSTIN, TX 78701
(512)416-8500
www.silabs.com

NAME: Si52258-D01-AM-QFN40-EVB

REV : 1.0

SIZE: C

PART NUMBER:

SCALE 1:1 | FABRICATION DRAWING | SHEET 1 OF 1