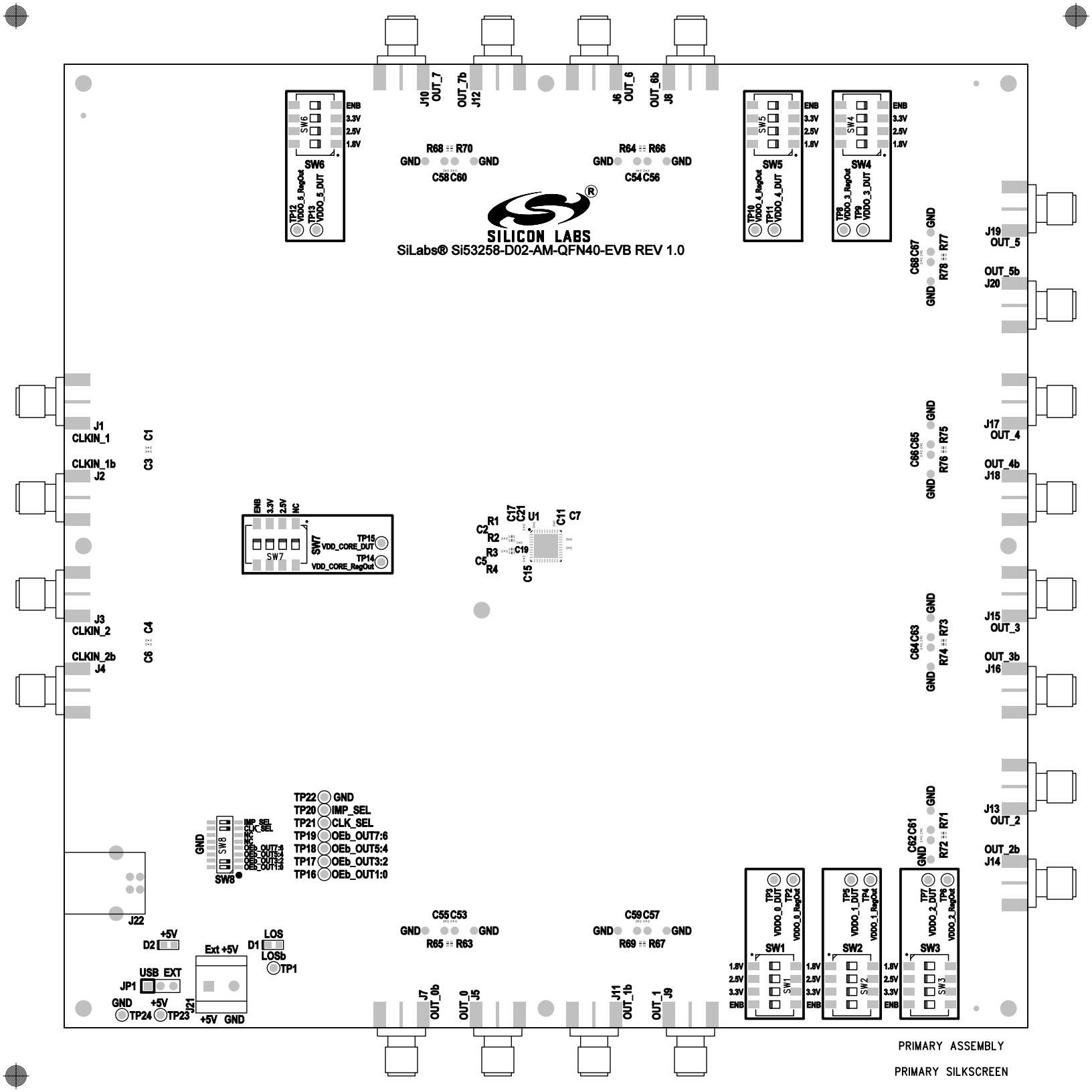
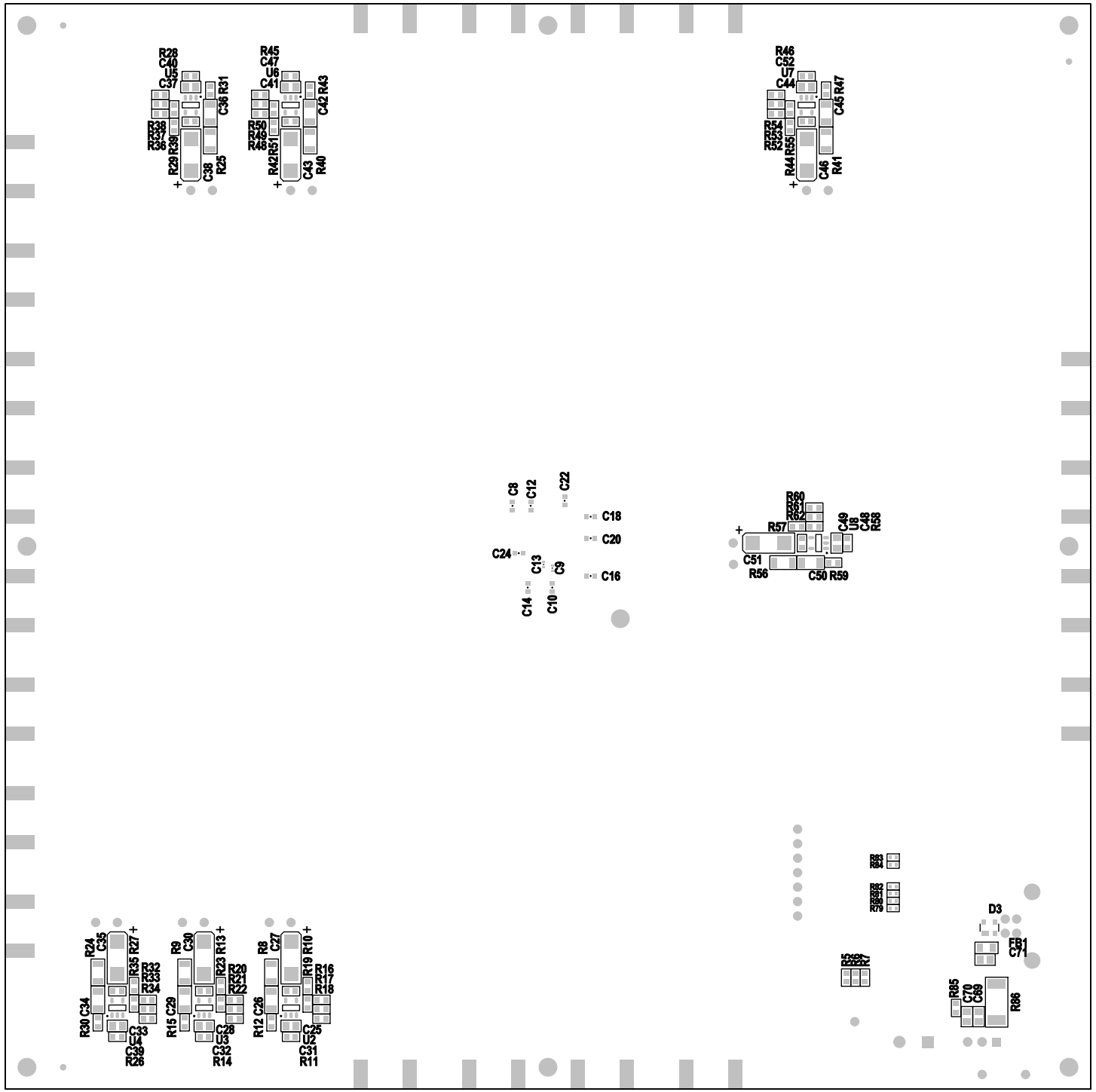
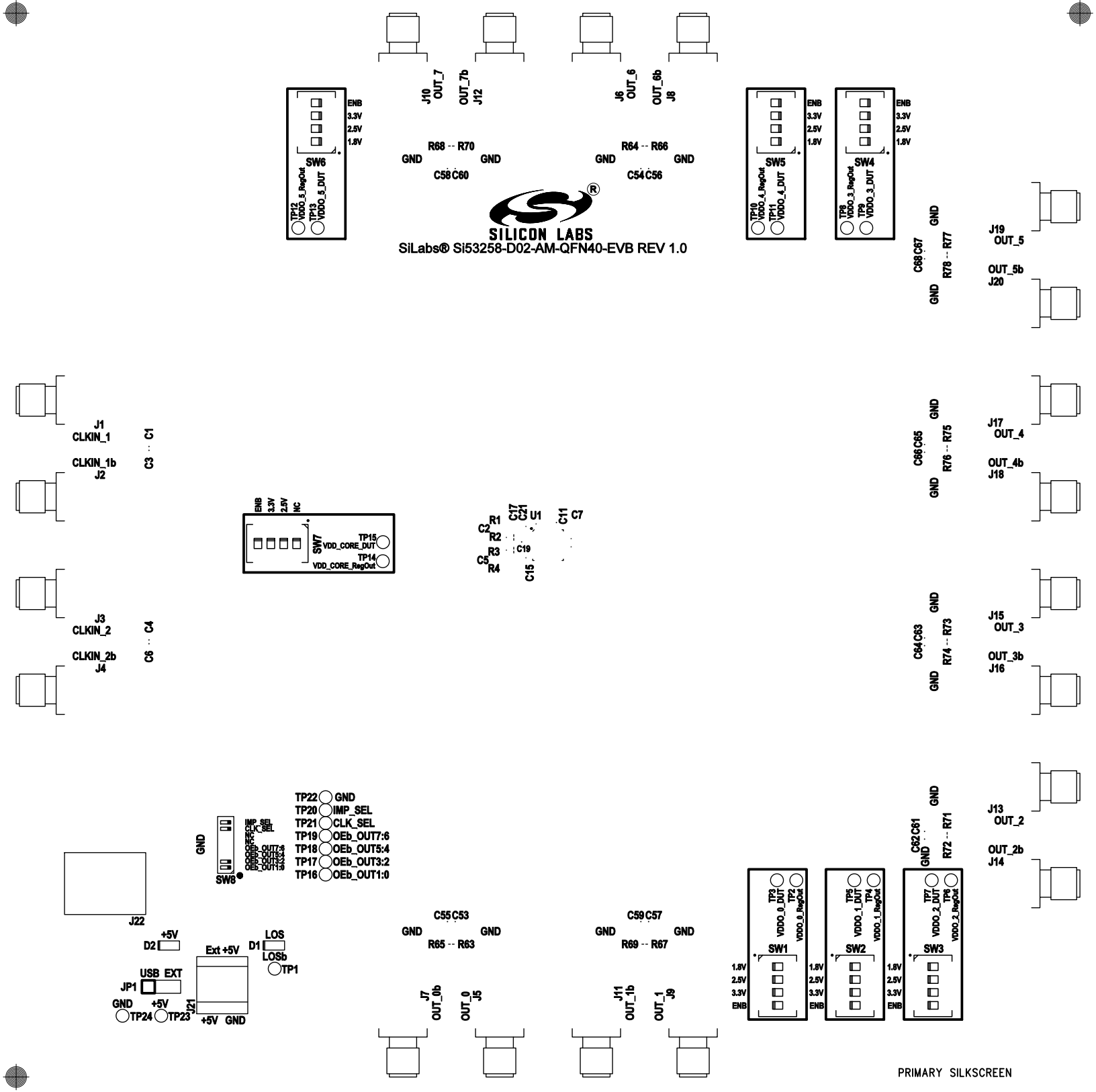
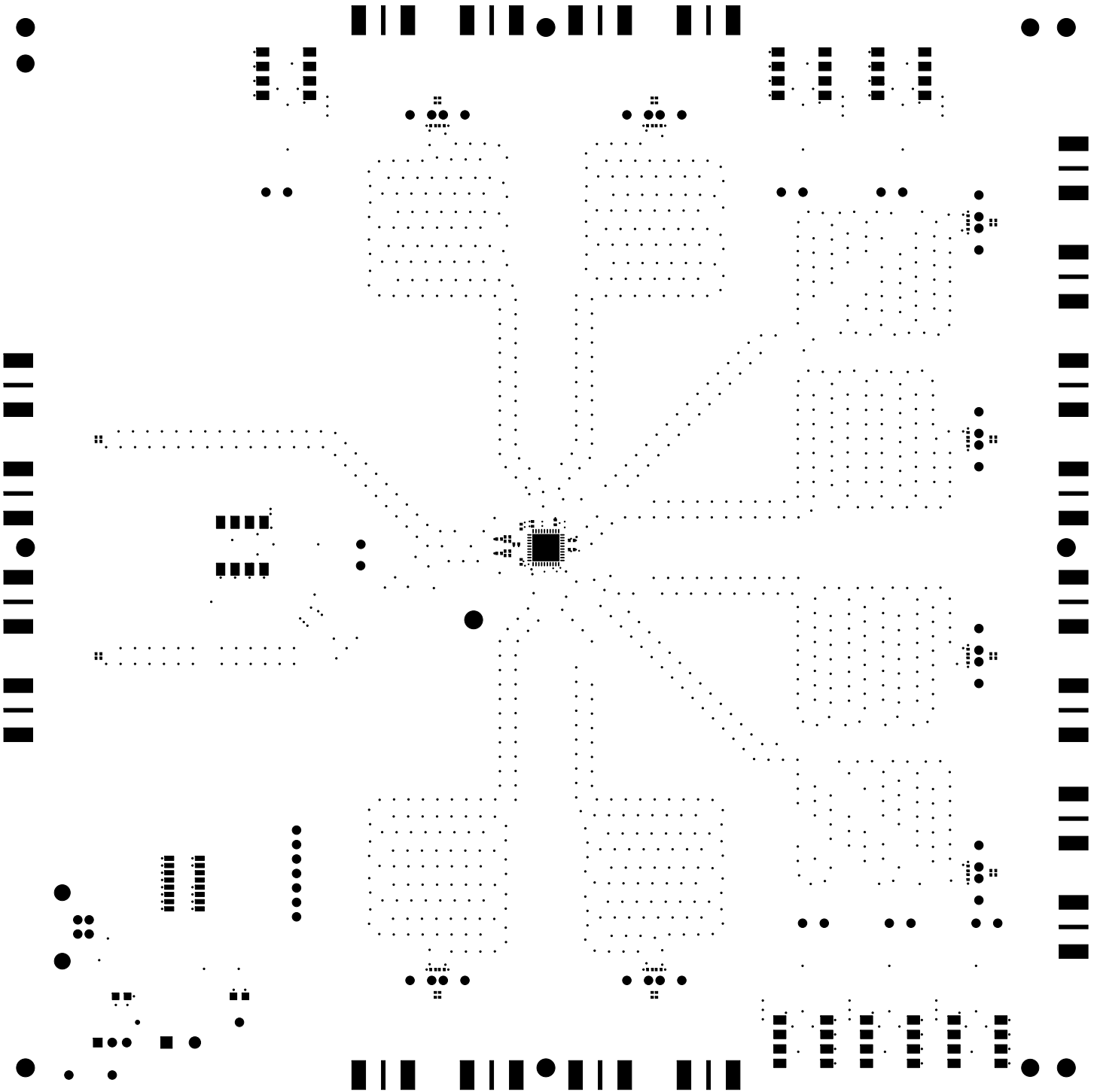

SILICON LABS
SiLabs® Si53258-D02-AM-QFN40-EVB REV 1.0
PRIMARY ASSEMBLY
PRIMARY SILKSCREEN



SECONDARY ASSEMBLY

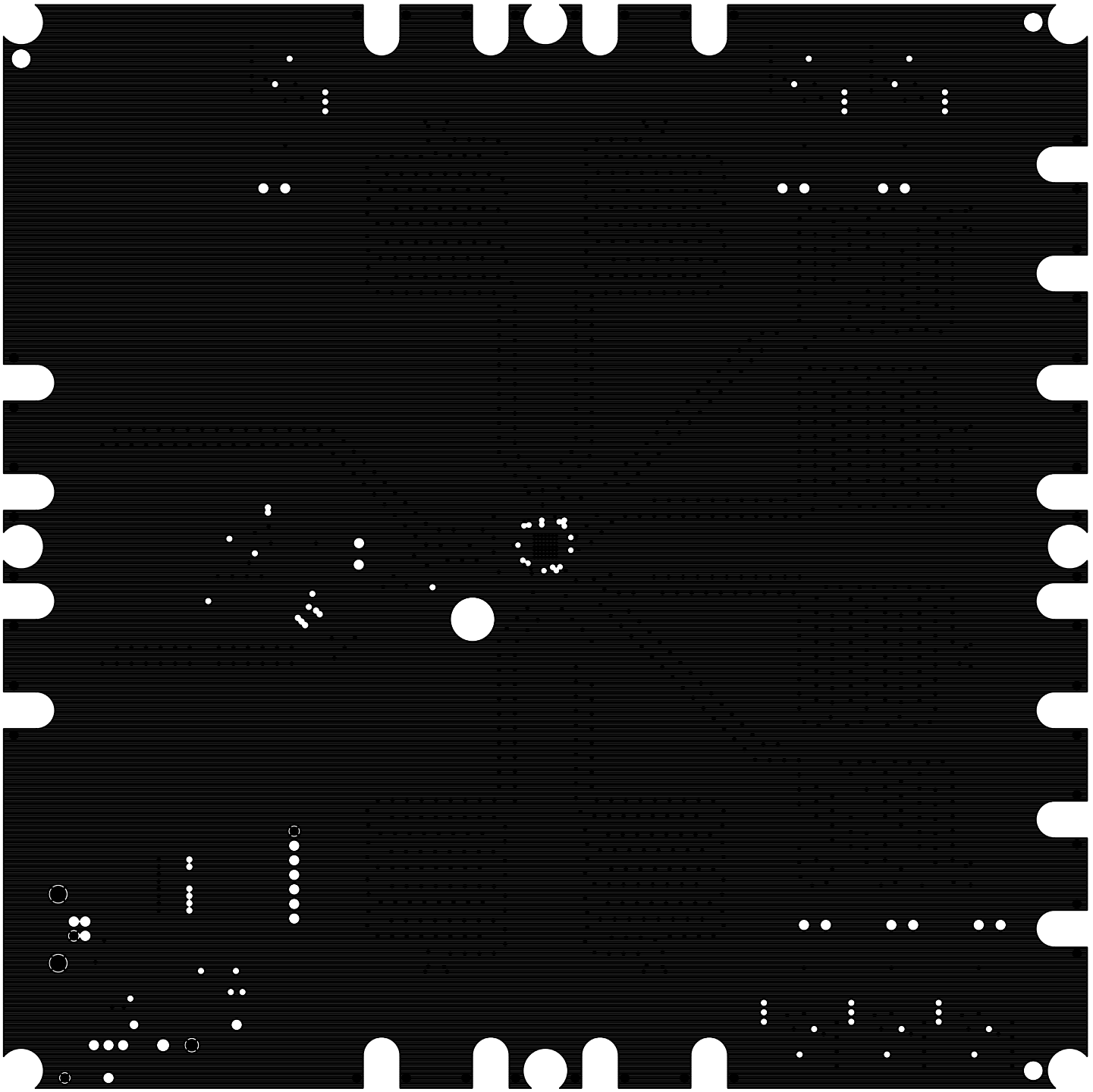
SECONDARY SILKSCREEN


SILICON LABS
SiLabs® Si53258-D02-AM-QFN40-EVB REV 1.0
PRIMARY SILKSCREEN

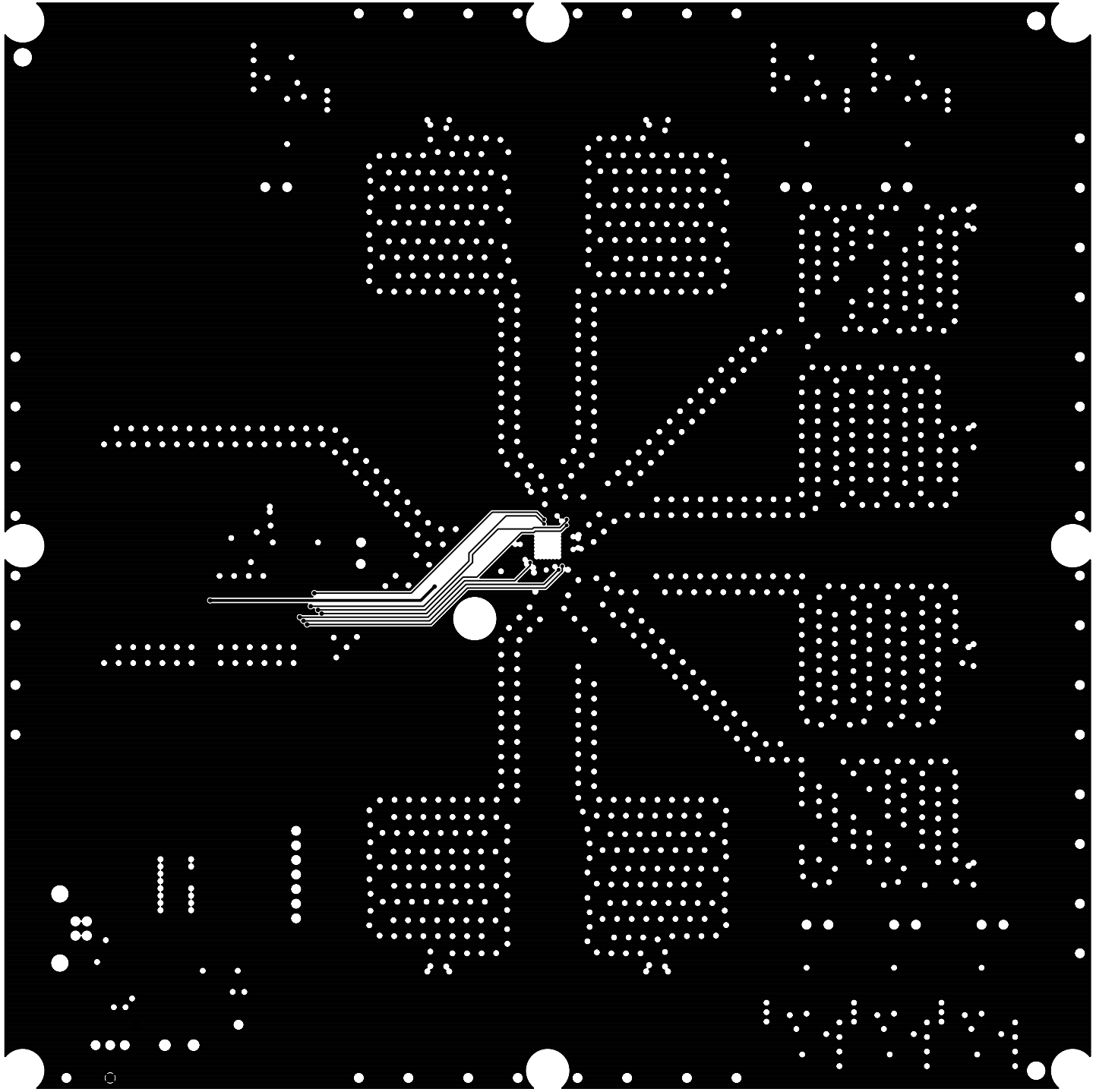


PRIMARY SOLDER MASK

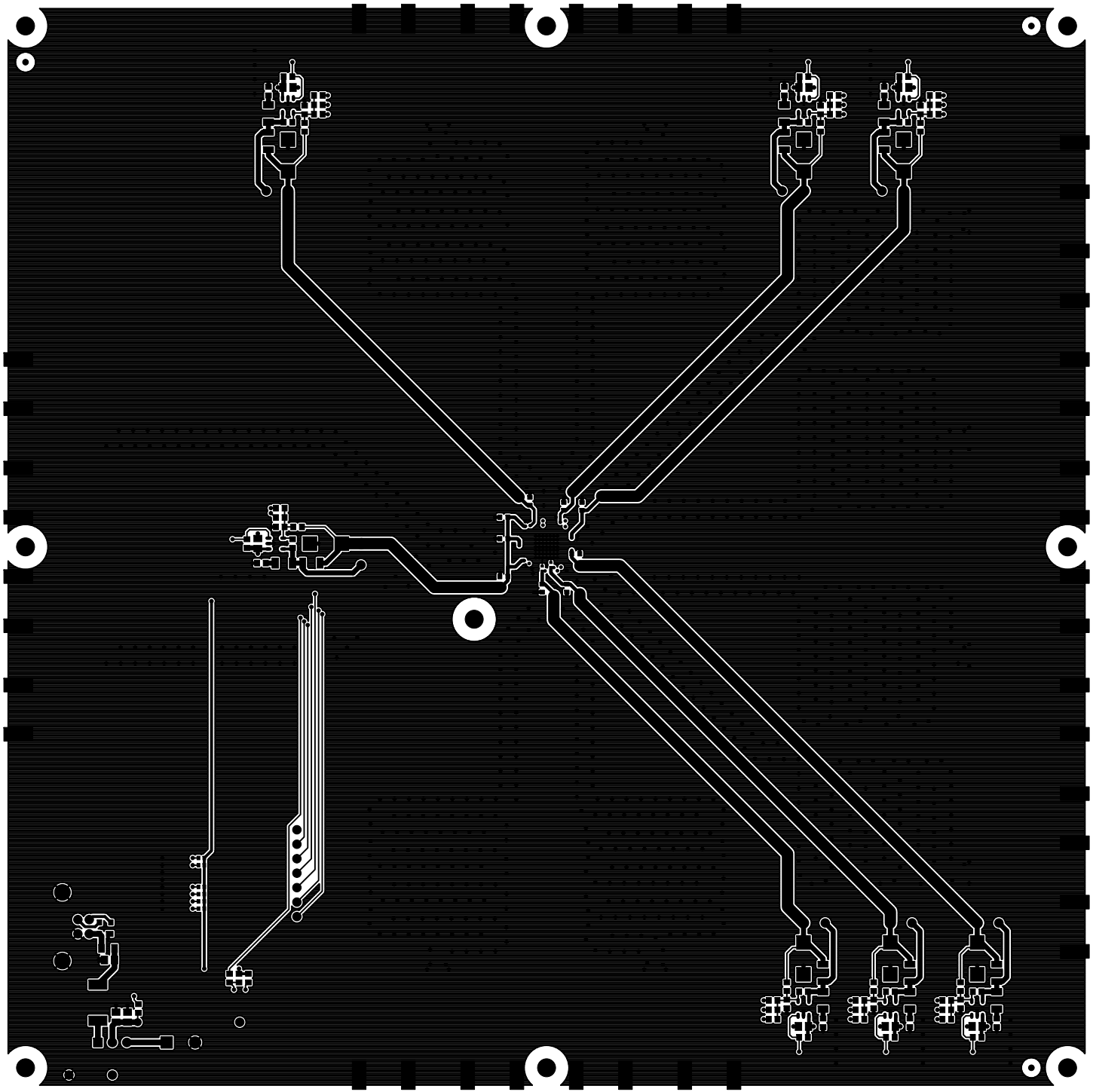
PRIMARY SIDE



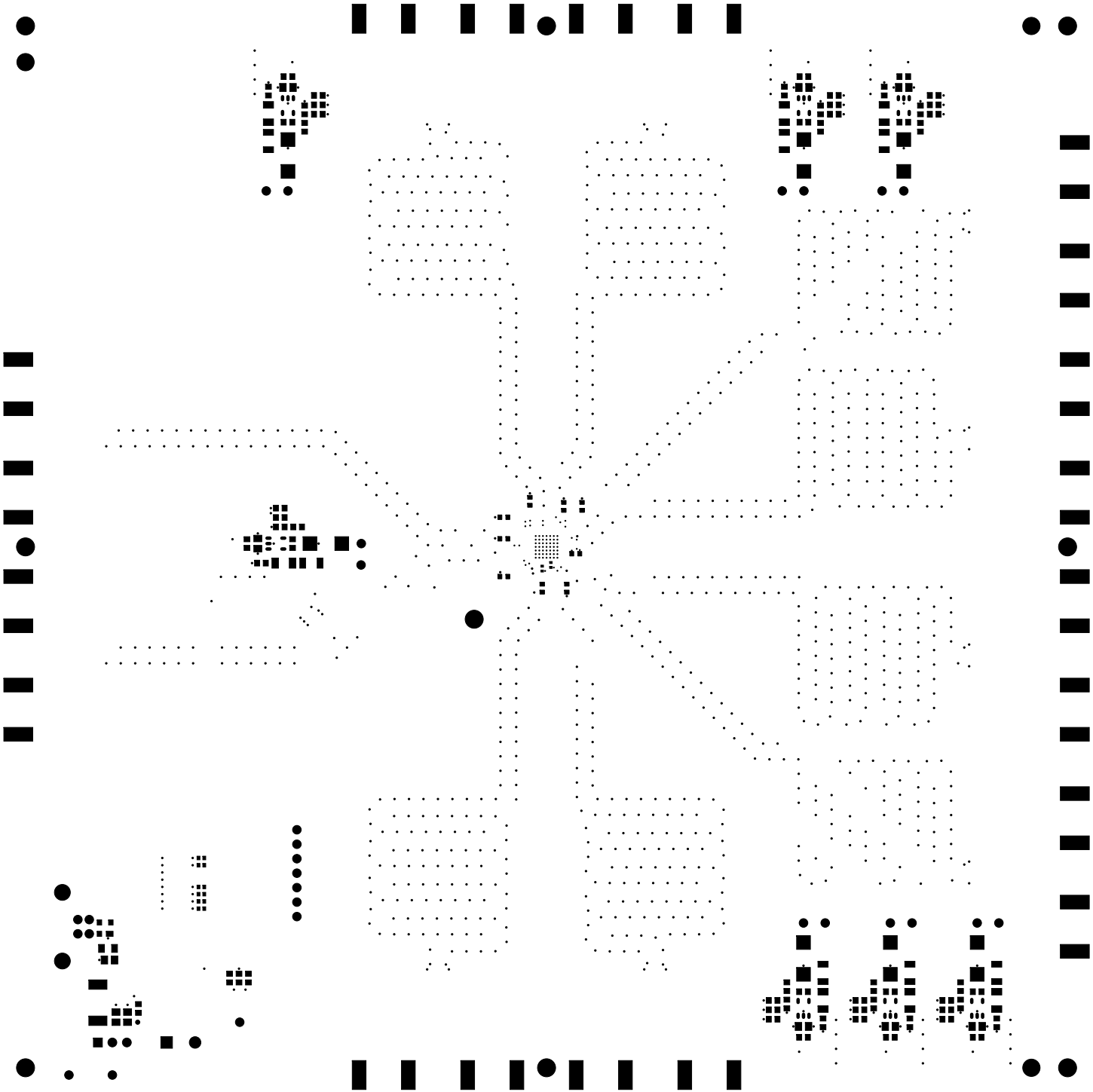
LAYER 02



LAYER 03

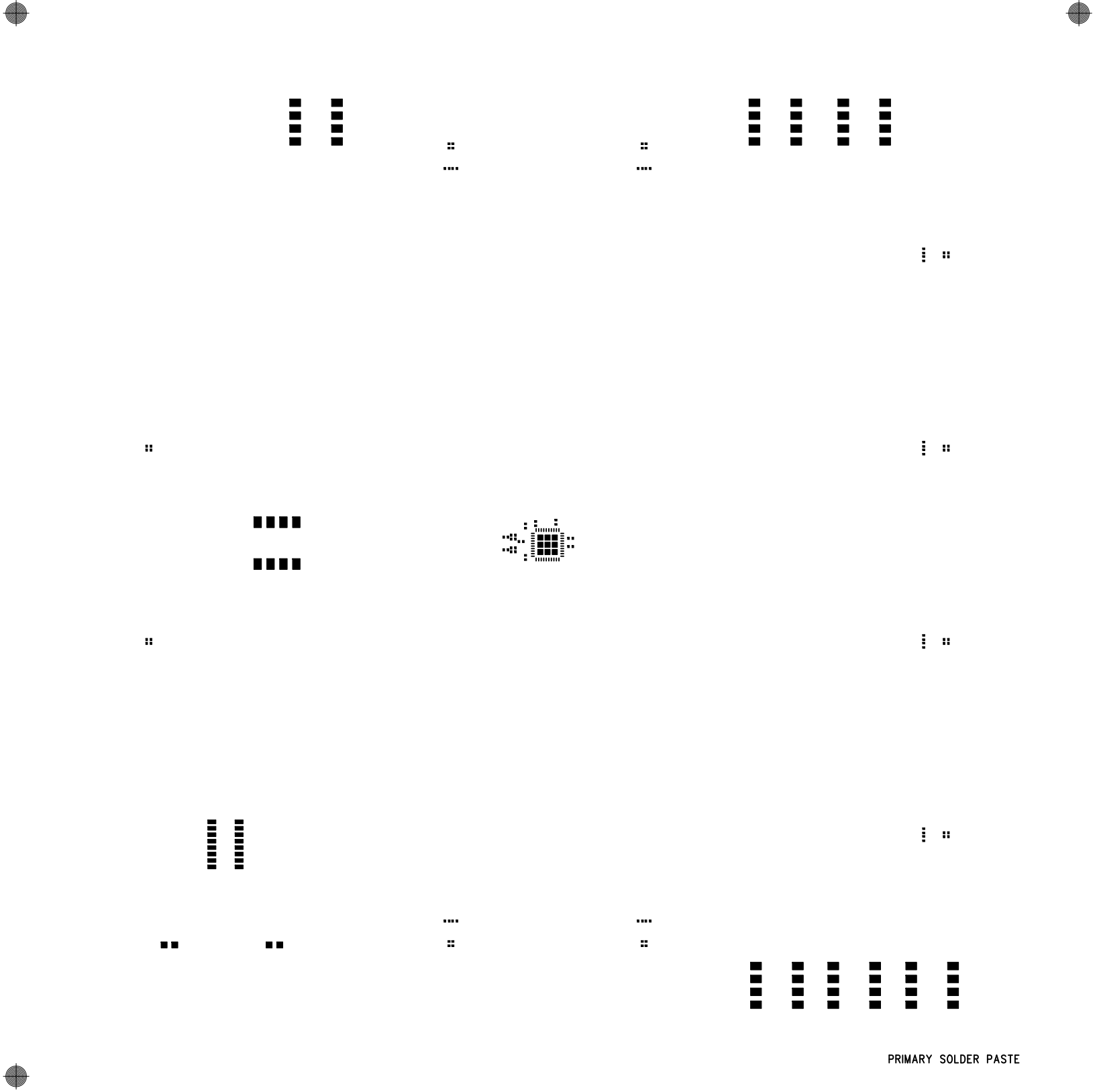


SECONDARY SIDE

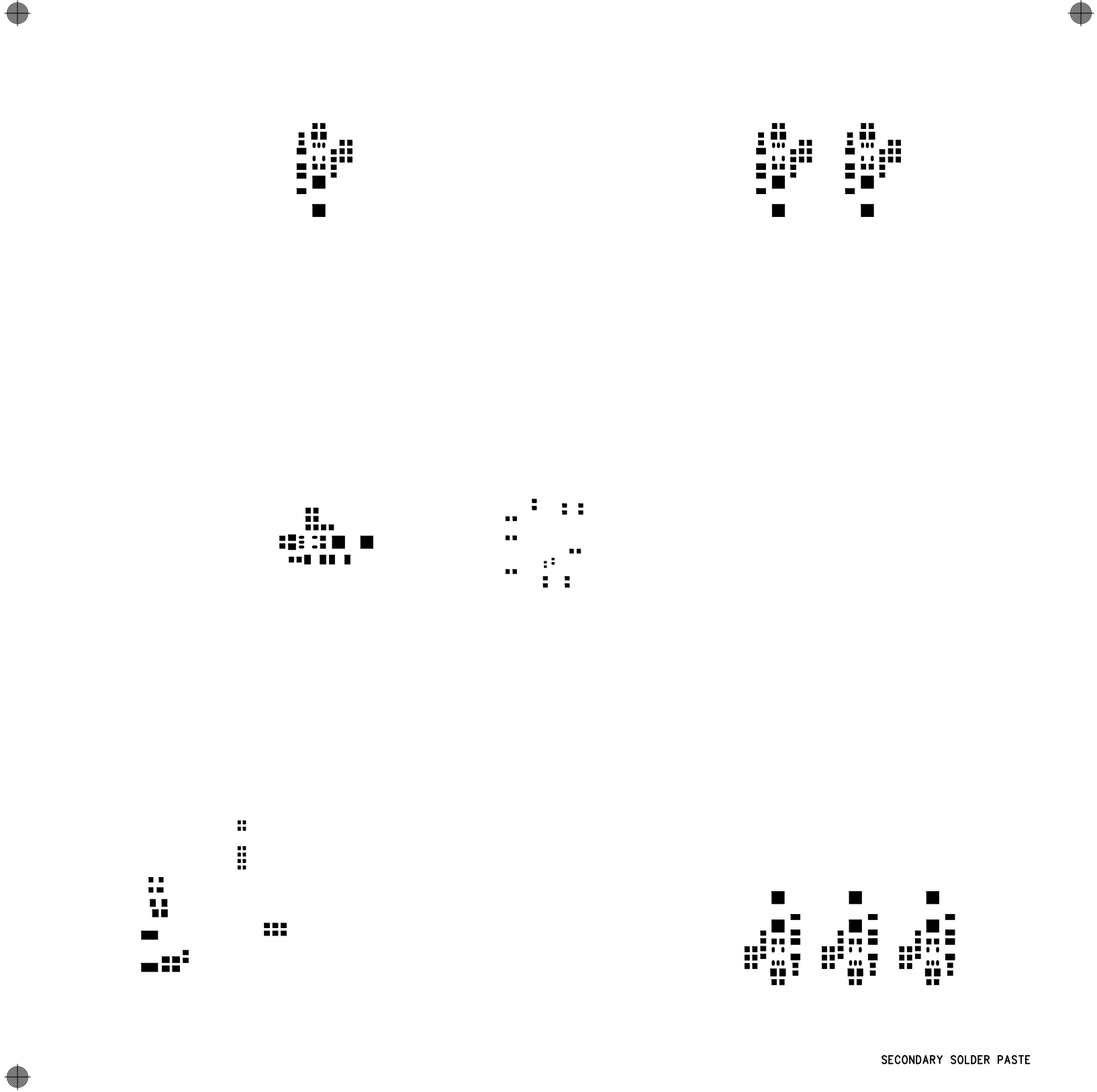


SECONDARY SOLDER MASK

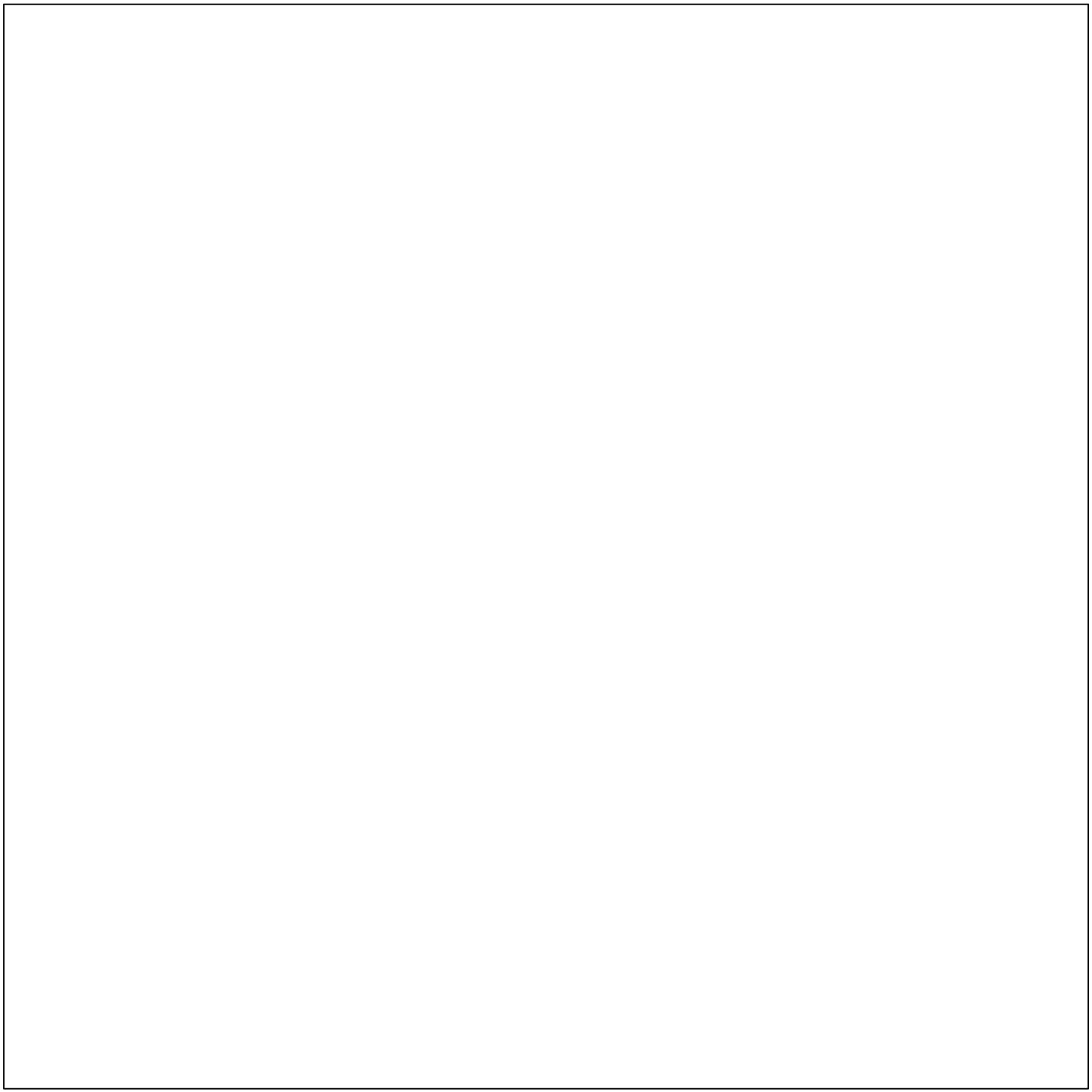
SECONDARY SILKSCREEN

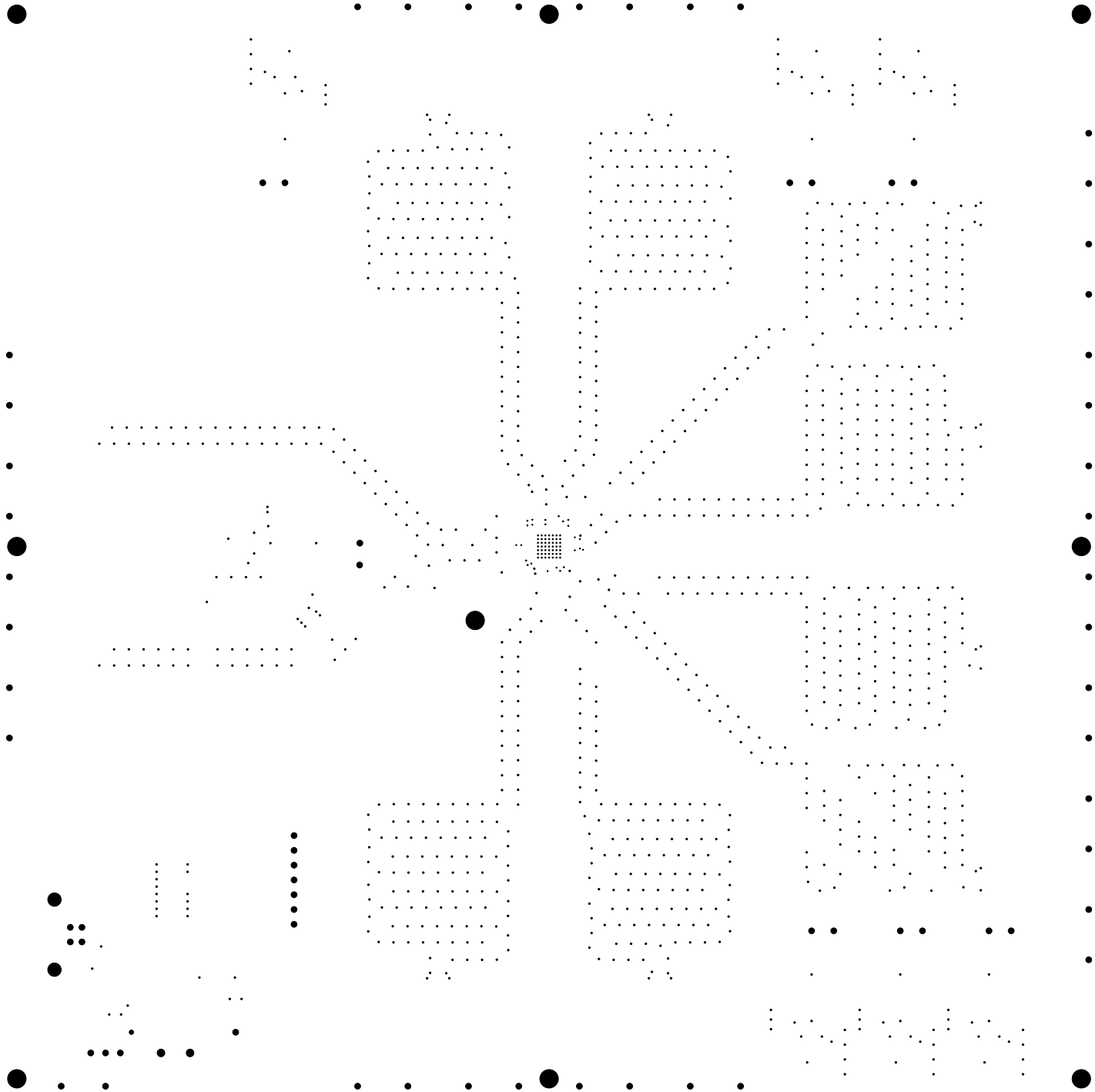


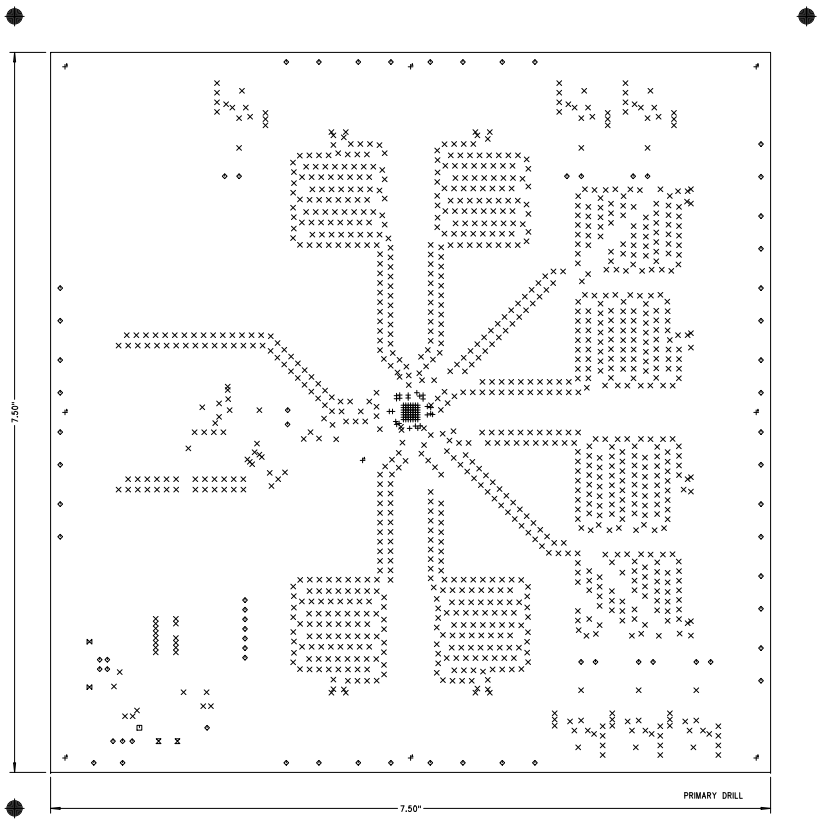
PRIMARY SOLDER PASTE



SECONDARY SOLDER PASTE







NOTES : UNLESS OTHERWISE SPECIFIED

1. MANUFACTURE IN ACCORDANCE WITH IPC-6012, TYPE 3, CLASS 2.
2. END PRODUCT FEATURES SHALL NOT VARY MORE THAN 20% FROM ARTWORK ORIGINALS.
3. LAMINATE AND PREPREG SHALL BE AS PER IPC-4101/26,83,98 WITH A DECOMPOSITION TEMPERATURE >= 345°C, COLOR, NATURAL.
4. COPPER WEIGHT SHALL BE 0.5 OZ./SQ. FT. BEFORE PLATING.
5. ALL PLATED THROUGH HOLES SHALL HAVE A MINIMUM OF 0.001" COPPER.
6. DRILL HOLE TOLERANCE AFTER PLATING SHALL BE ±0.003".
7. MINIMUM ANNULAR RING SHALL BE 0.001".
8. MINIMUM ANNULAR RING AT EMERGENT CONDUCTORS SHALL BE 0.003".
9. FINAL PCB THICKNESS SHALL BE 0.062" ±10%.
10. WARP/TWIST SHALL NOT EXCEED 1.0%
11. FINISH SHALL BE LPI, BLUE SMOBC, ENIG BOTH SIDES.
12. SILKSCREEN WITH NONCONDUCTIVE WHITE EPOXY INK.
13. EXTERNAL 6.0MIL TRACES TO BE 42.5 OHM Zo ±5%.
    EXTERNAL 26MIL TRACES TO BE 42.5 OHM Zo ±5% REF TO L03.

14. VENDOR TO PROVIDE PCB MICRO-SECTION OF COUPON AREA & TDR TEST REPORT.
15. REFERENCE ADDITIONAL FAB NOTES IN FILE README.TXT

LAYER STACKUP	FILE NAMES
PRIMARY SILKSCREEN	53258-D02-AM-QFN40-CEVB_PSS.PHO
PRIMARY SOLDERMASK	53258-D02-AM-QFN40-CEVB_PSM.PHO
PRIMARY SIDE/RF ROUTE	53258-D02-AM-QFN40-CEVB_PRI.PHO
370HR	2.8MIL THK
GROUND PLANE	53258-D02-AM-QFN40-CEVB_L02.PHO
370HR	8MIL THK
PWR PLANE	53258-D02-AM-QFN40-CEVB_L03.PHO
370HR	46.5MIL THK
SECONDARY SIDE	53258-D02-AM-QFN40-CEVB_SEC.PHO
SECONDARY SOLDERMASK	53258-D02-AM-QFN40-CEVB_SSM.PHO
SECONDARY SILKSCREEN	53258-D02-AM-QFN40-CEVB_SSS.PHO

0.062" THK

SCALE: NONE

SIZE	QTY	SYM	PLT	TOOL	TOL
0.008	73	+	P	1	+0/-0.008
0.012	1194	X	P	2	+0/-0.012
0.030	1	□	P	3	+/-0.003
0.040	71	◇	P	4	+/-0.003
0.052	2	⧖	P	5	+/-0.003
0.091	2	⋈	P	6	+/-0.003
0.125	9	A	N	7	+/-0.003

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES AND APPLY AFTER FINISH
DIMENSIONS IN BRACKETS [ ] ARE IN MILLIMETERS
INTERPRET DRAWING PER ML-D-1000
TOLERANCES
HOLE TOLERANCES PER 78027
DECIMALS .XX +/- .XXX +/-
ANGLES +/-
SURFACES MICROINCHES
PART TO BE FREE OF BURRS
BREAK EDGES MAX
BEND RADIUS MAX
BEND RELIEF MAX

DESIGN	TS	02JUL2019
LAYOUT	AA	02JUL2019

DO NOT SCALE DRAWING

COMPANY: SILICON LABS
400 W CESAR CHAVEZ ST.
AUSTIN, TX 78701
(512)416-8500
www.silabs.com

NAME: Si53258-D02-AM-QFN40-EVB . REV : 1.0

SIZE C | PART NUMBER: .

SCALE 1:1 | FABRICATION DRAWING | SHEET 1 OF 1