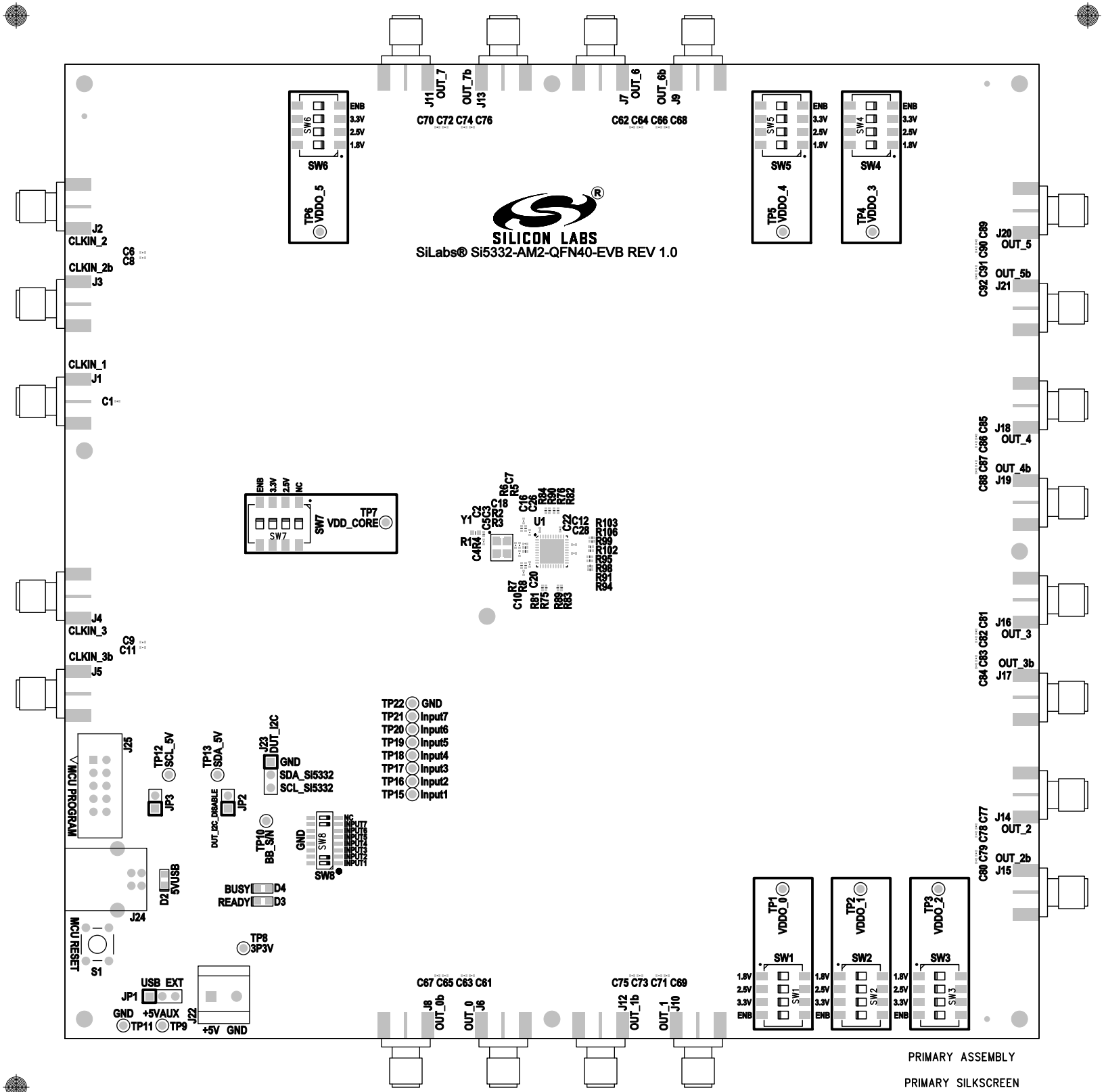
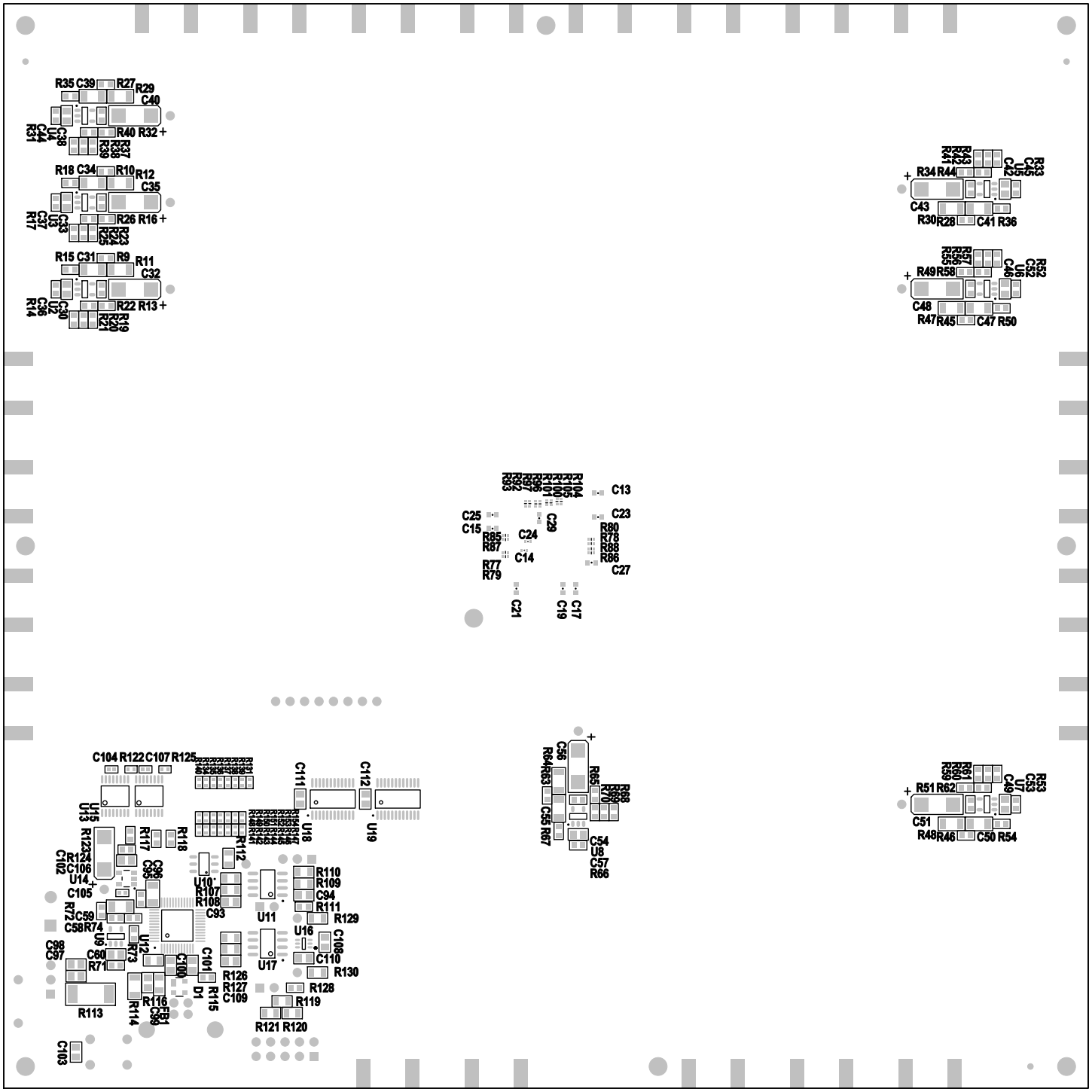


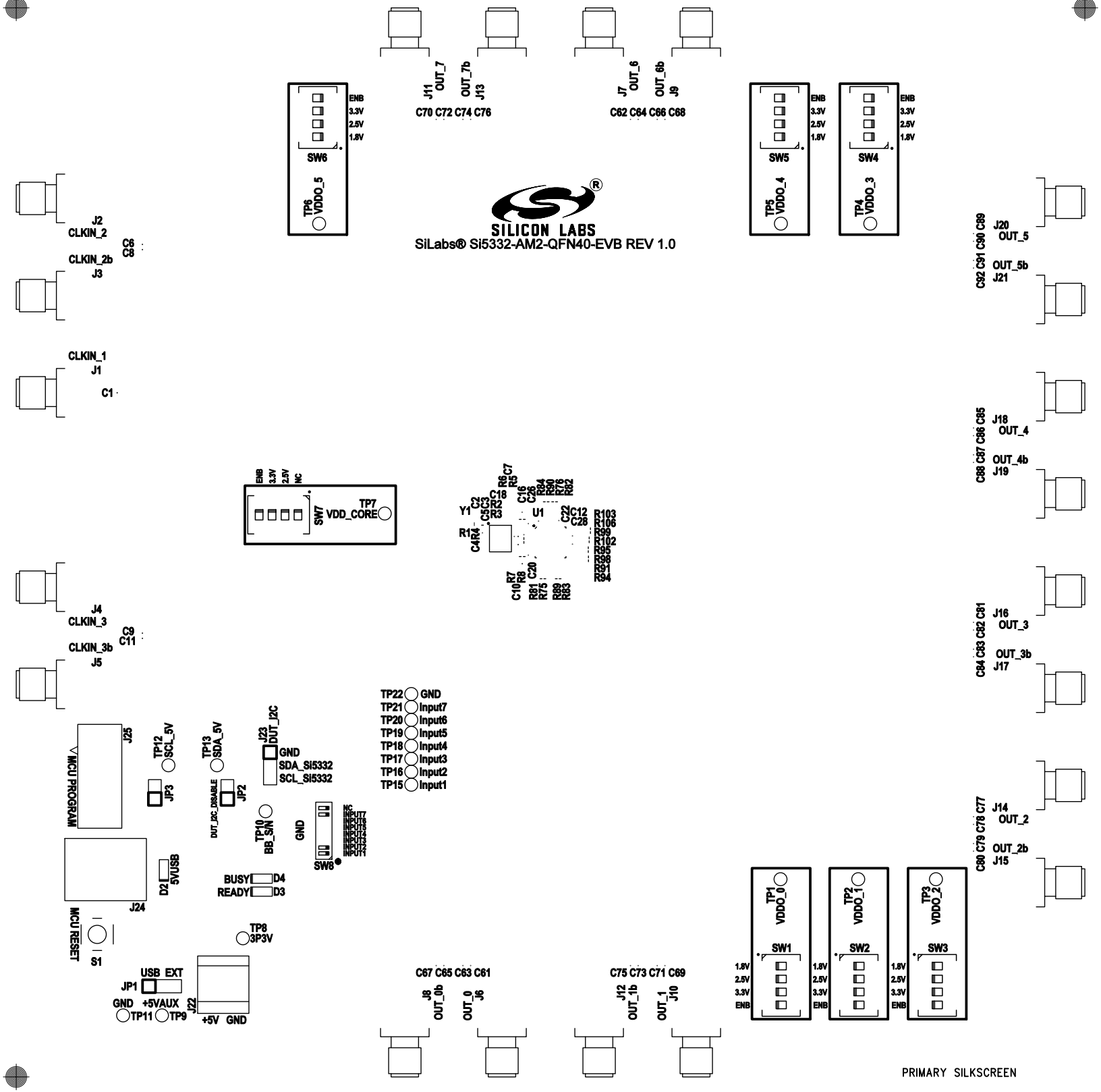
PRIMARY ASSEMBLY

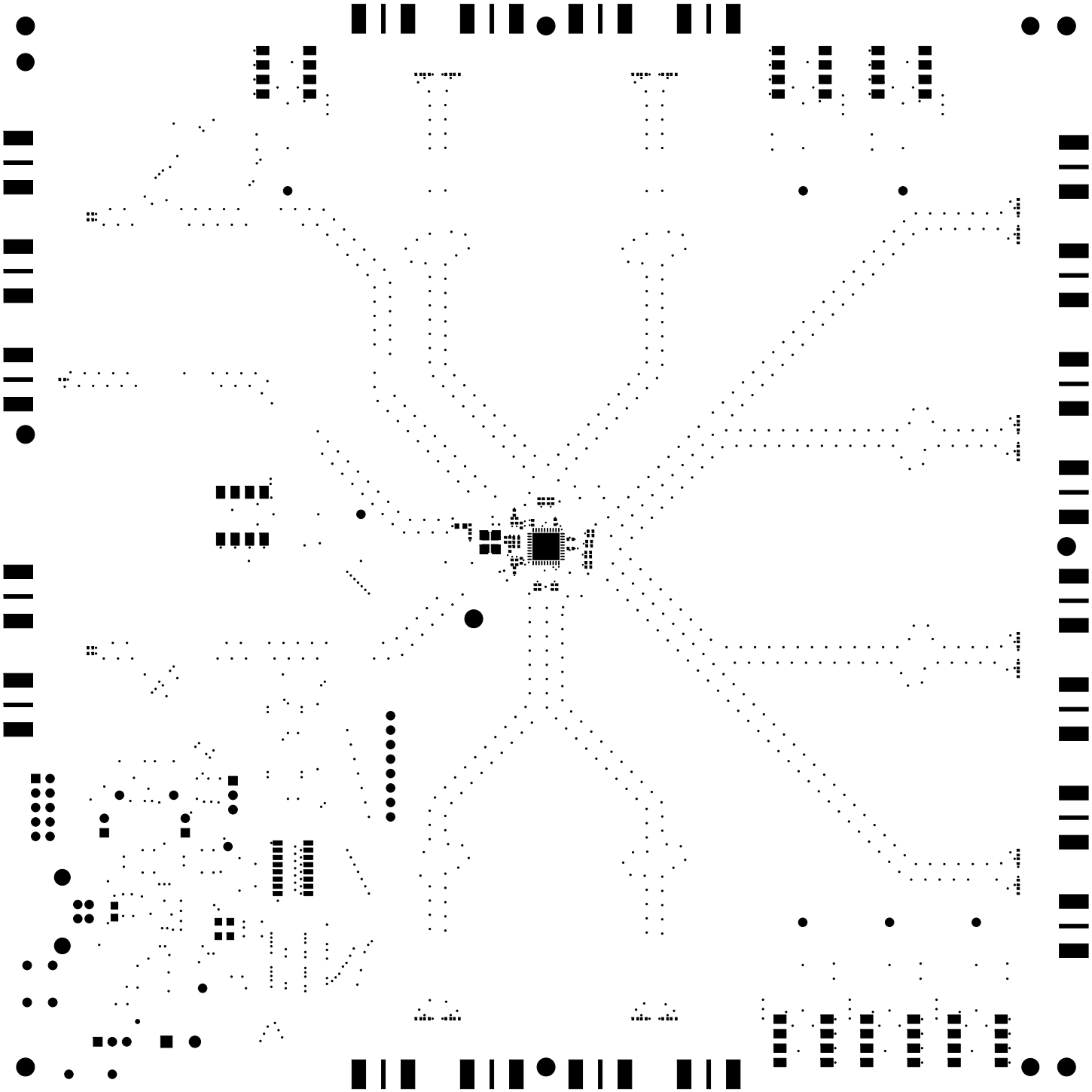
PRIMARY SILKSCREEN

SECONDARY SILKSCREEN

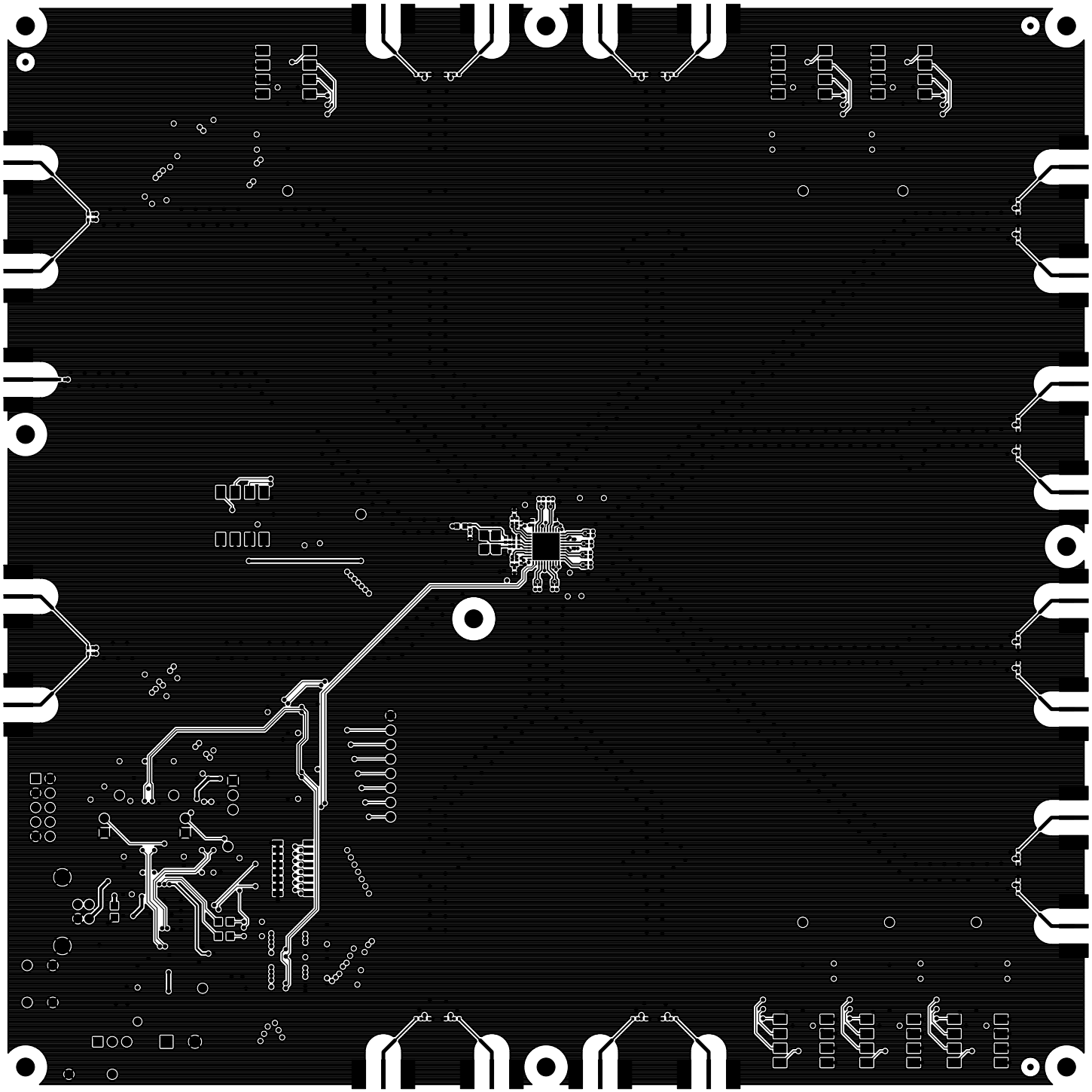
SECONDARY ASSEMBLY



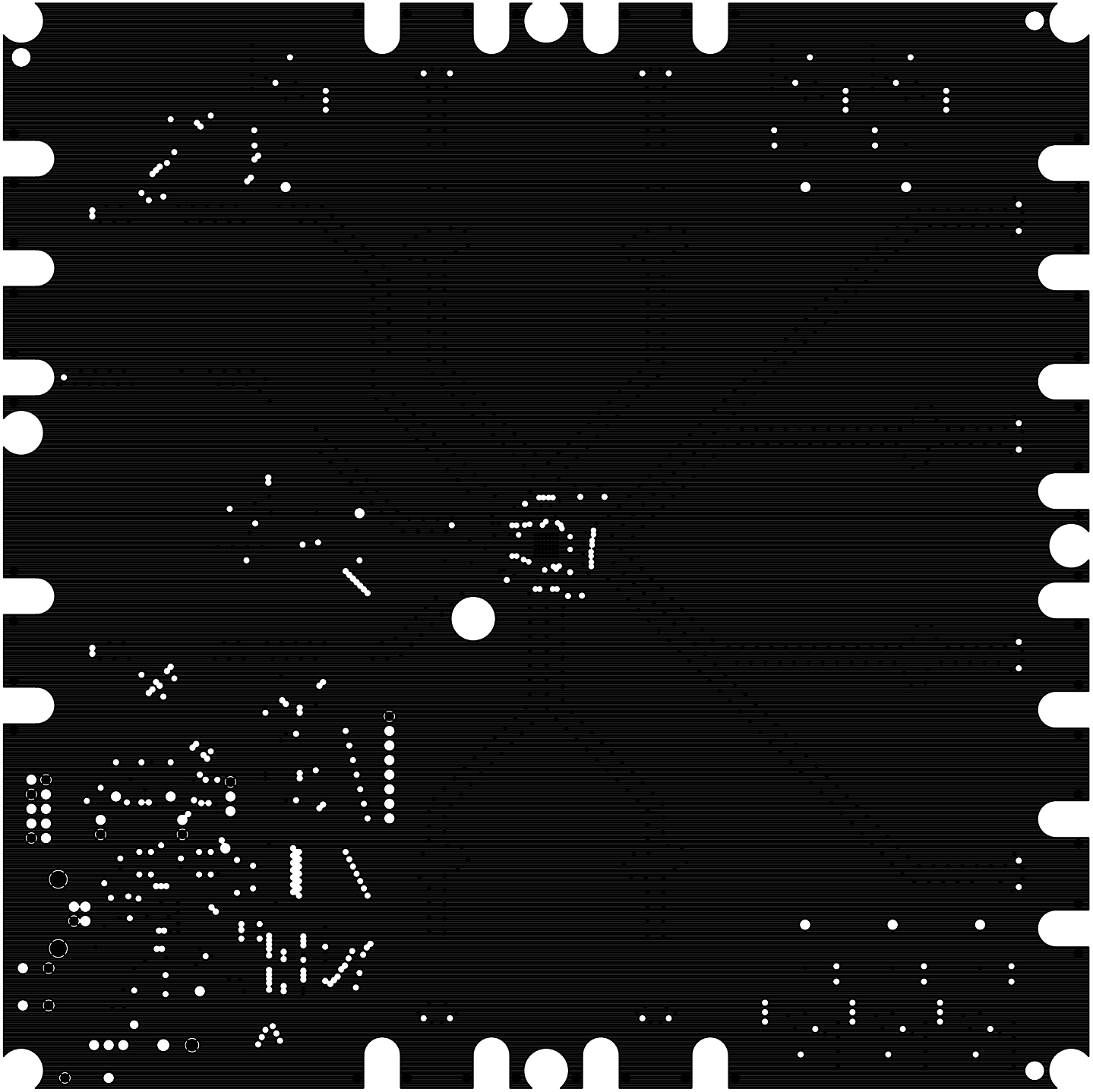

SILICON LABS
SiLabs® Si5332-AM2-QFN40-EVB REV 1.0
J11 OUT_7
OUT_7b J13
C70 C72 C74 C76
J7 OUT_6
OUT_6b J9
C62 C64 C66 C68
SW6
SW5
SW4
ENB
3.3V
2.5V
1.8V
TP6 VDDO_5
TP5 VDDO_4
TP4 VDDO_3
J2 CLKIN_2
C6
C8
CLKIN_2b J3
CLKIN_1 J1
C1
J20 OUT_5
C92 C91 C90 C89
OUT_5b J21
J18 OUT_4
C88 C87 C86 C85
OUT_4b J19
J16 OUT_3
C84 C83 C82 C81
OUT_3b J17
J14 OUT_2
C80 C79 C78 C77
OUT_2b J15
SW7
NC
TP7 VDD_CORE
Y1
U1
J4 CLKIN_3
C9
C11
CLKIN_3b J5
TP22 GND
TP21 Input7
TP20 Input6
TP19 Input5
TP18 Input4
TP17 Input3
TP16 Input2
TP15 Input1
J25
MCU PROGRAM
TP12 SCL_5V
TP13 SDA_5V
J23 DUT_I2C
GND
SDA_Si5332
SCL_Si5332
JP3
JP2
DUT_I2C_DISABLE
TP10 BB_S/N
GND
SW8
D2 5VUSB
J24
BUSY D4
READY D3
MCU RESET
S1
TP8 3P3V
USB EXT
JP1
GND +5VAUX
TP11 TP9
J22
+5V GND
C67 C65 C63 C61
J8 OUT_0b
OUT_0 J6
C75 C73 C71 C69
J12 OUT_1b
OUT_1 J10
TP1 VDDO_0
TP2 VDDO_1
TP3 VDDO_2
SW1
SW2
SW3
1.8V
2.5V
3.3V
ENB
PRIMARY SILKSCREEN



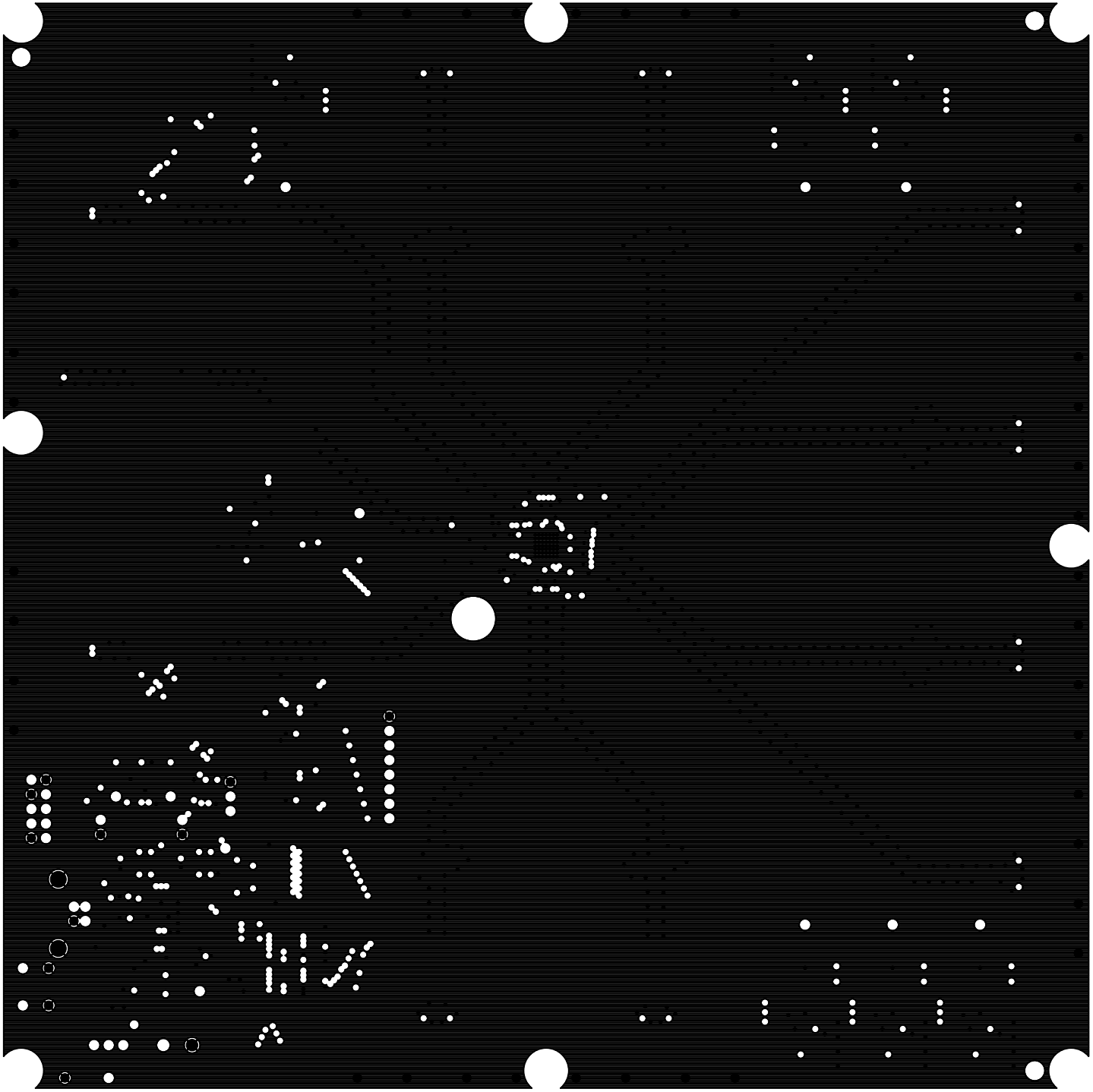
PRIMARY SOLDER MASK



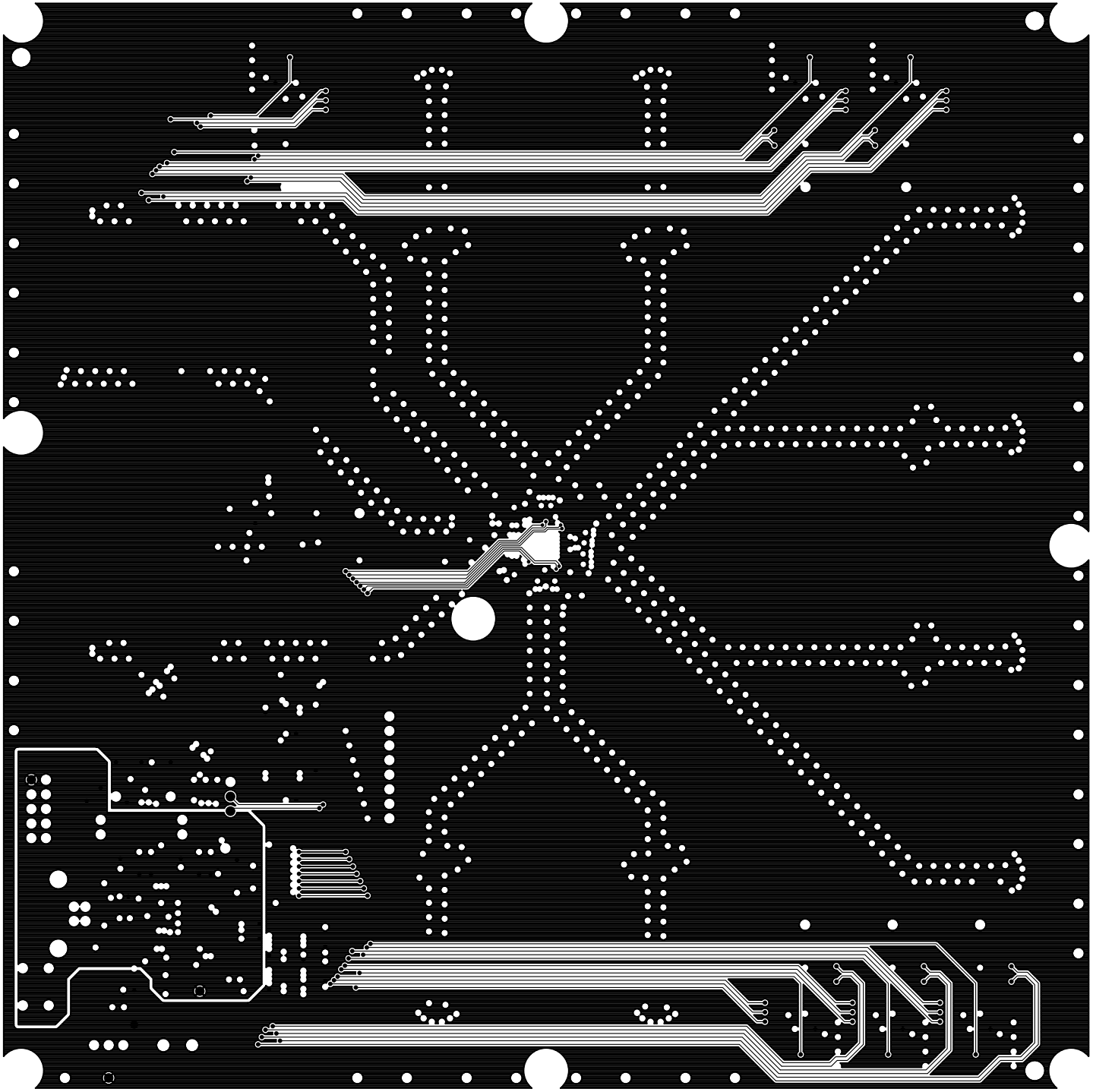
PRIMARY SIDE



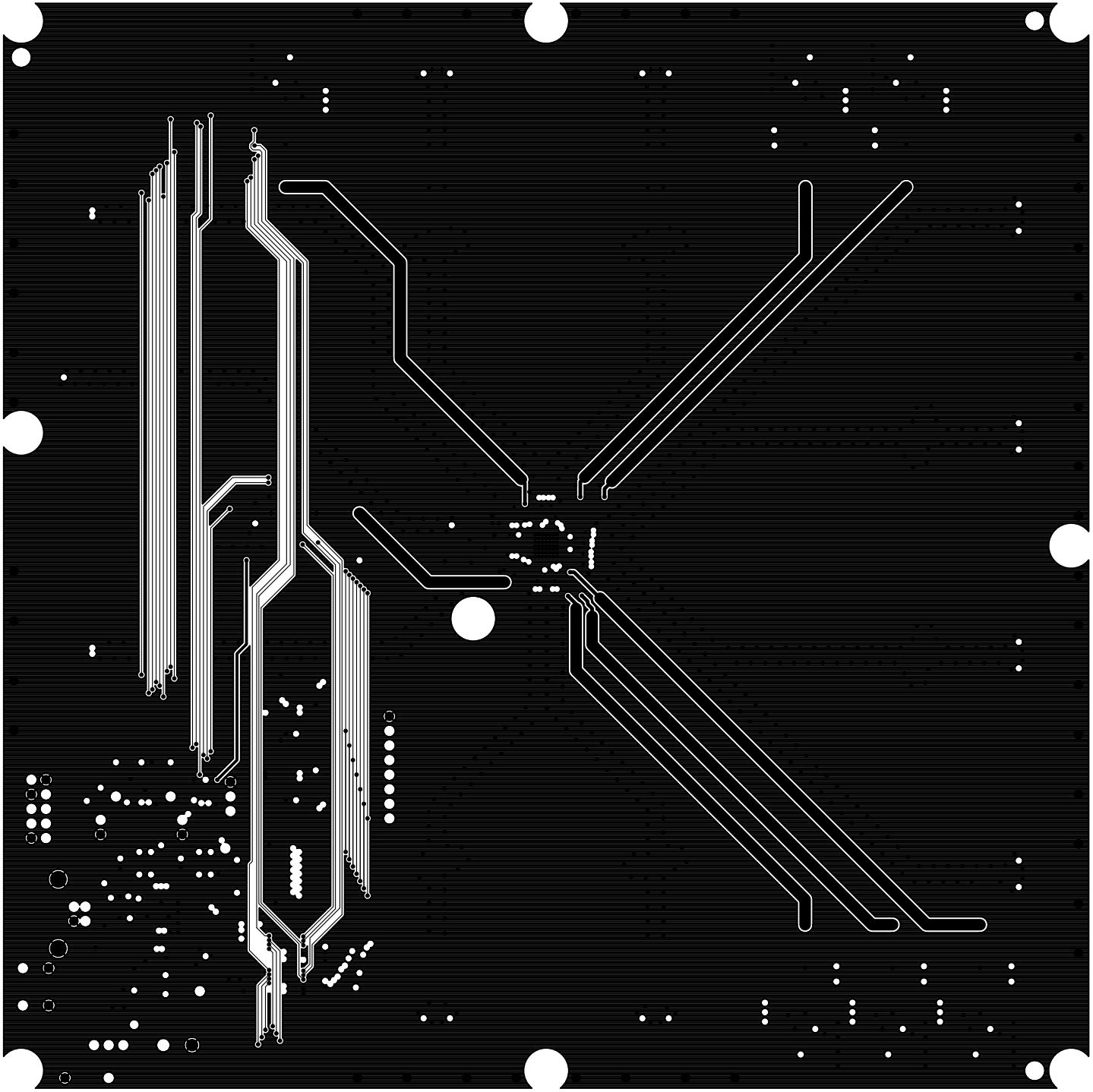
LAYER 02



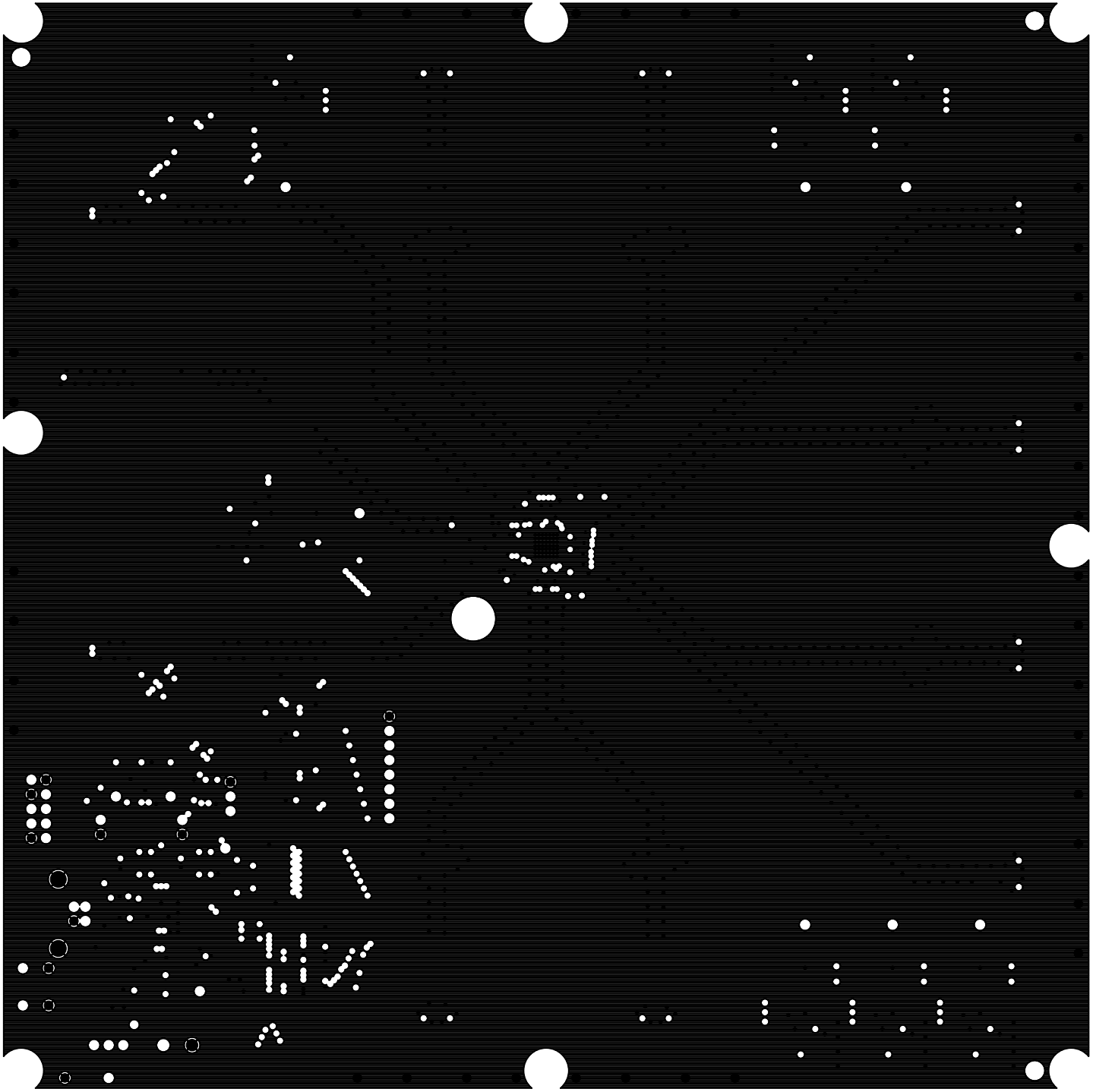
LAYER 03



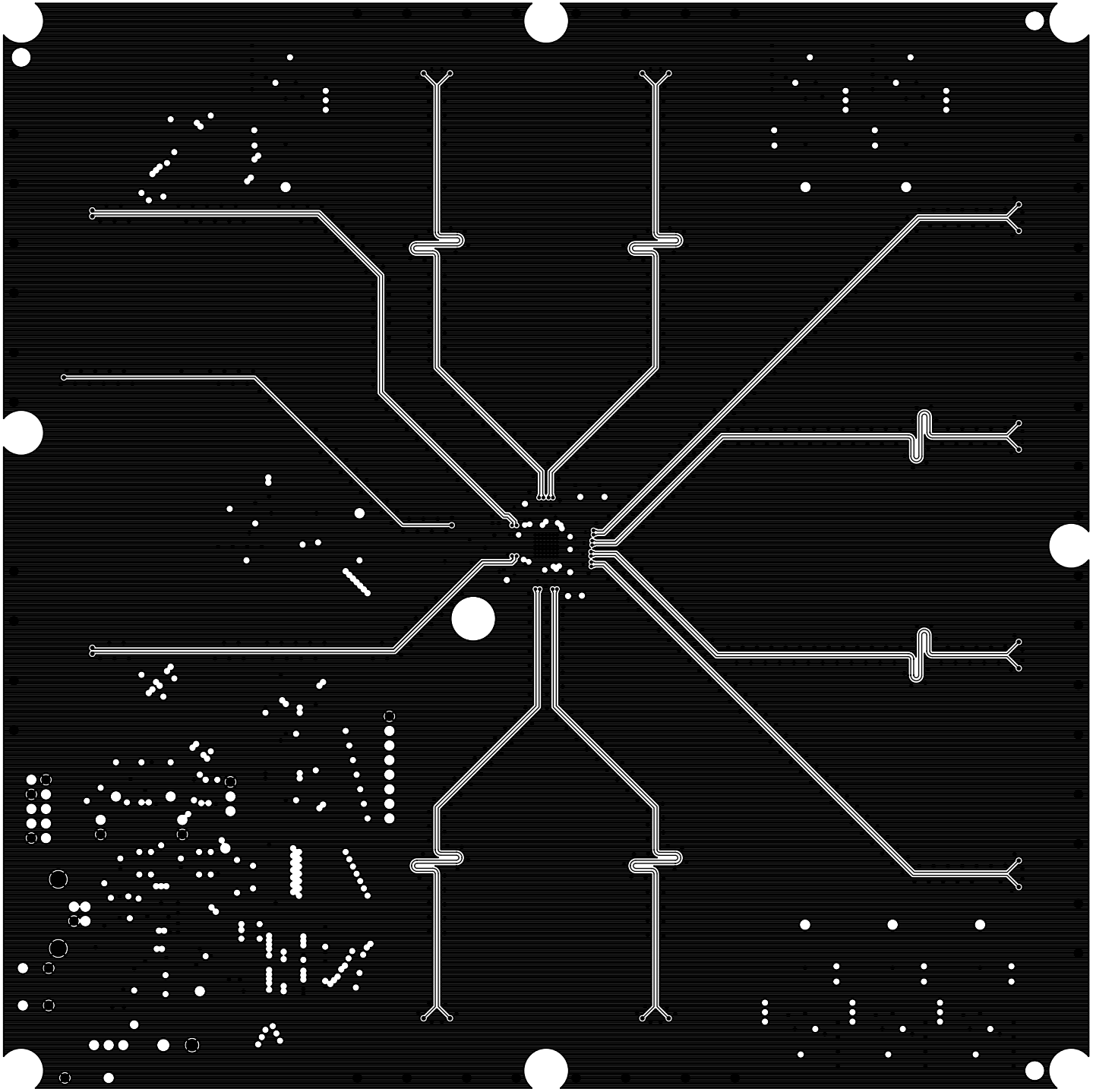
LAYER 04



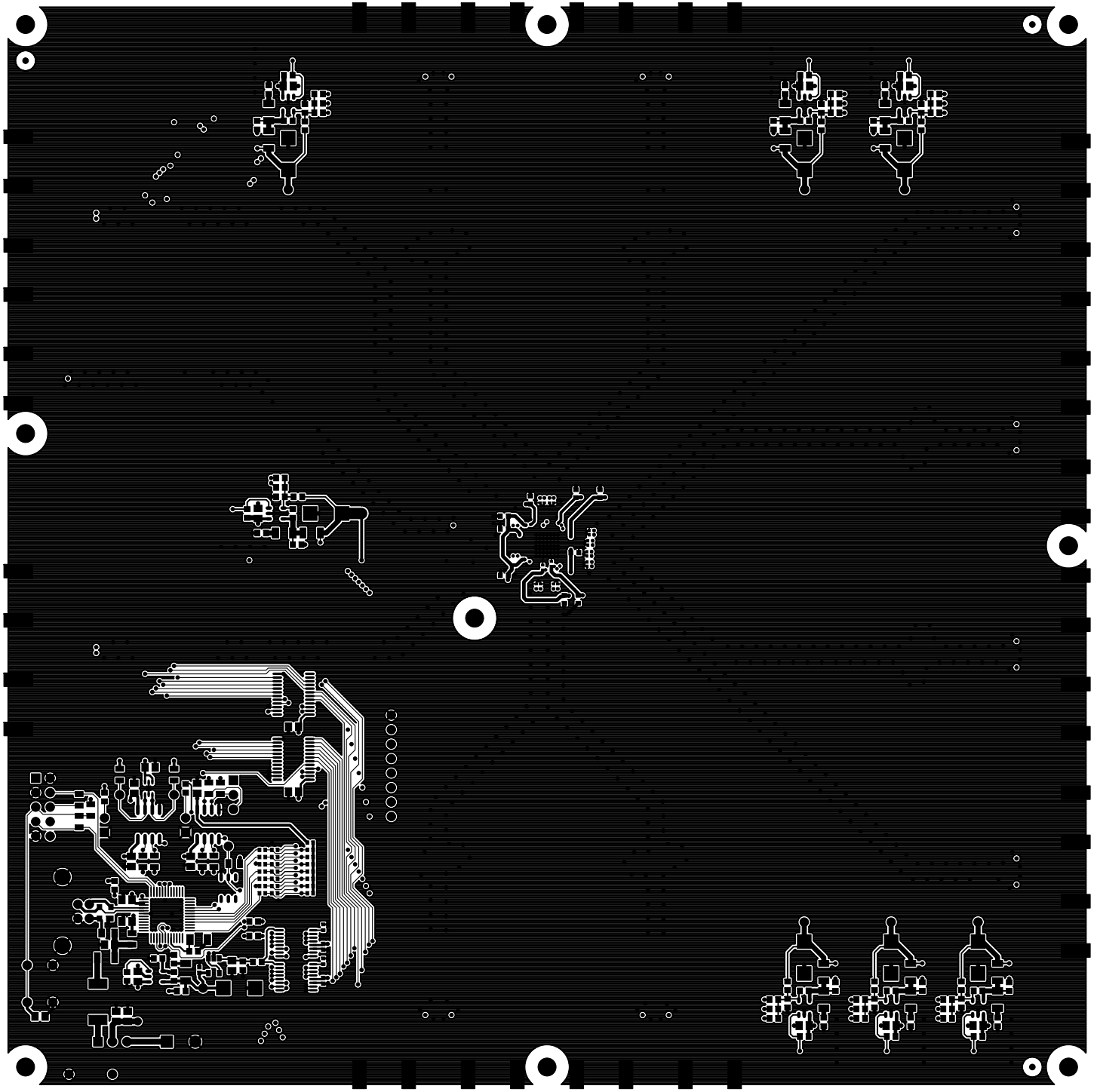
LAYER 05



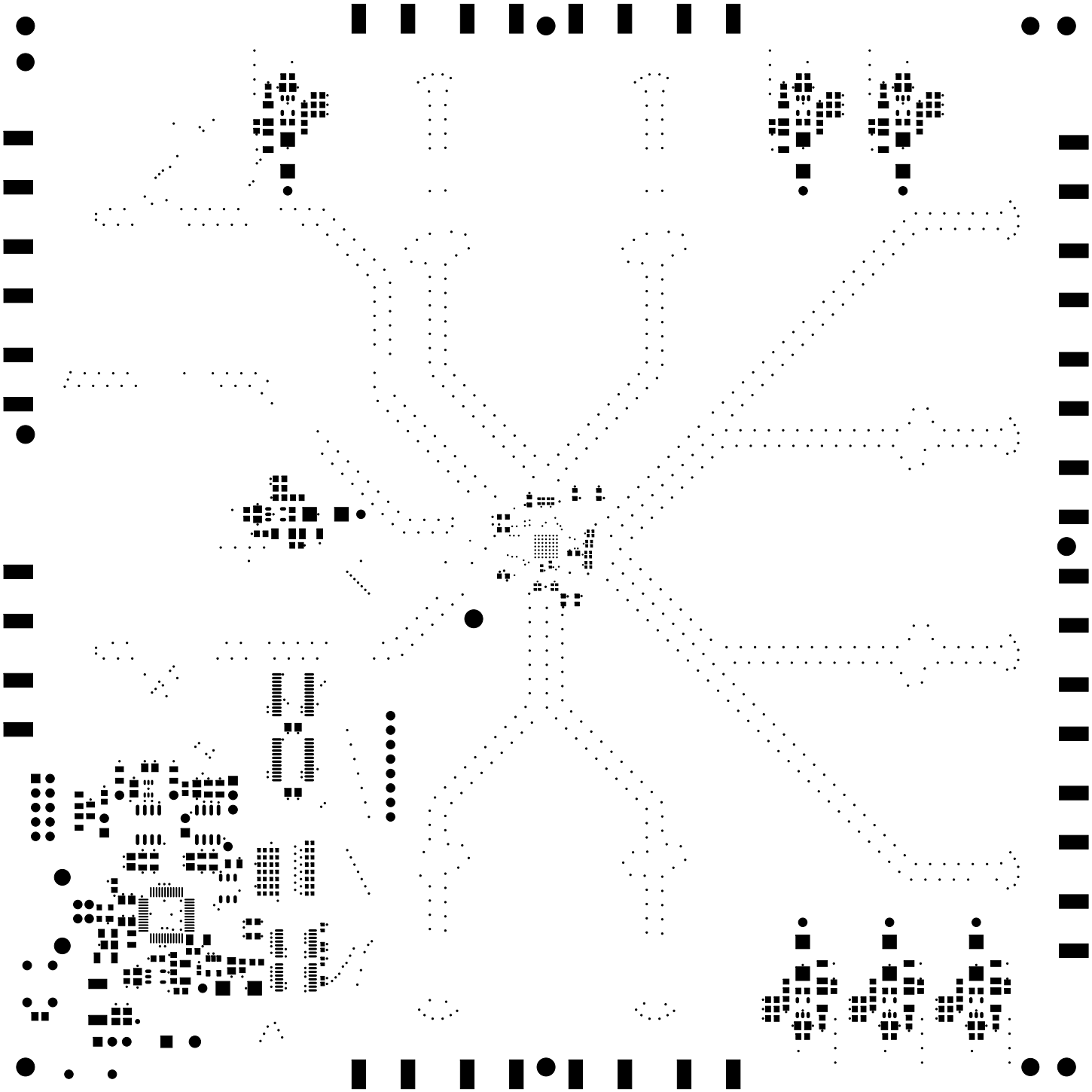
LAYER 06



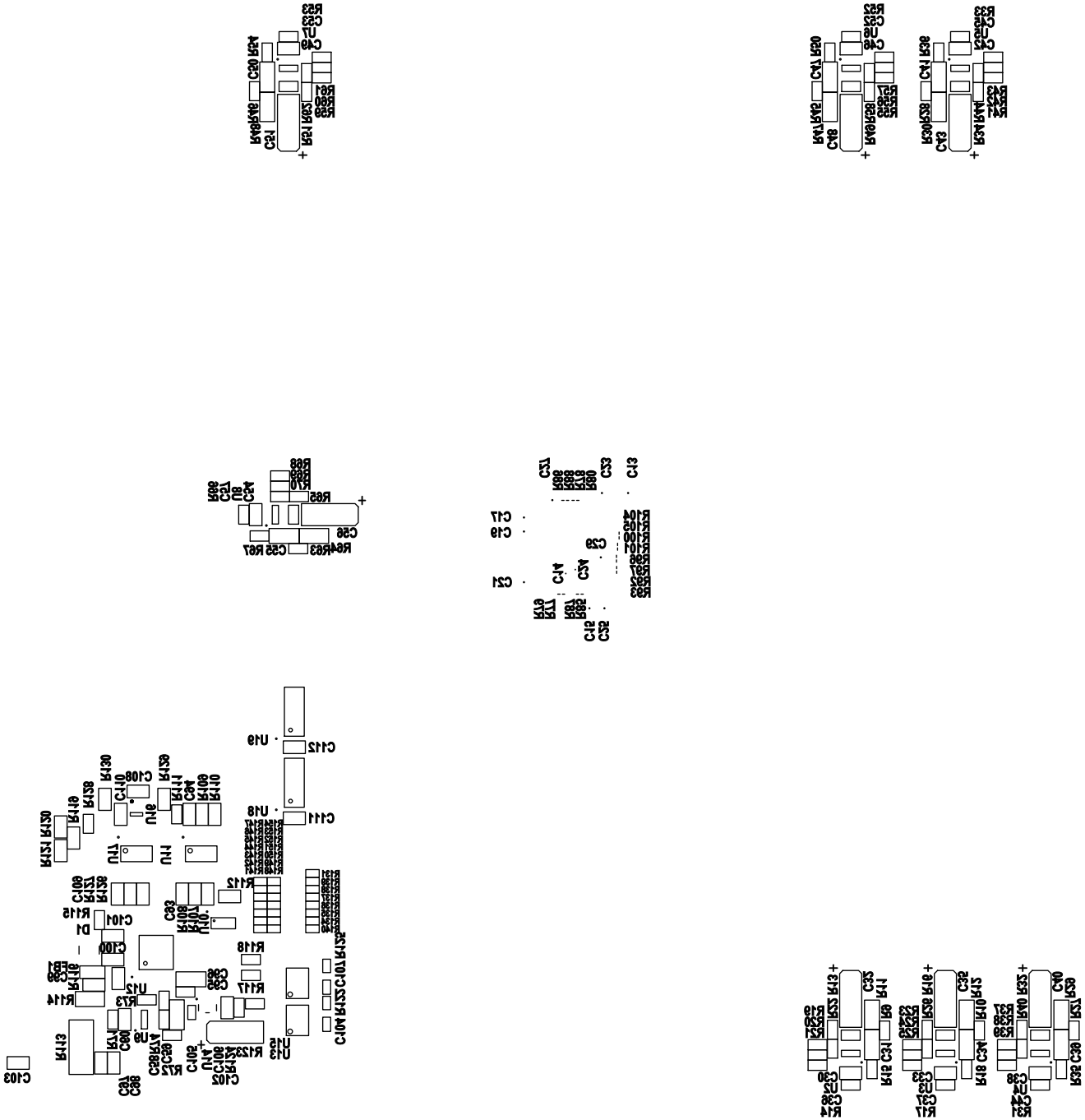
LAYER 07



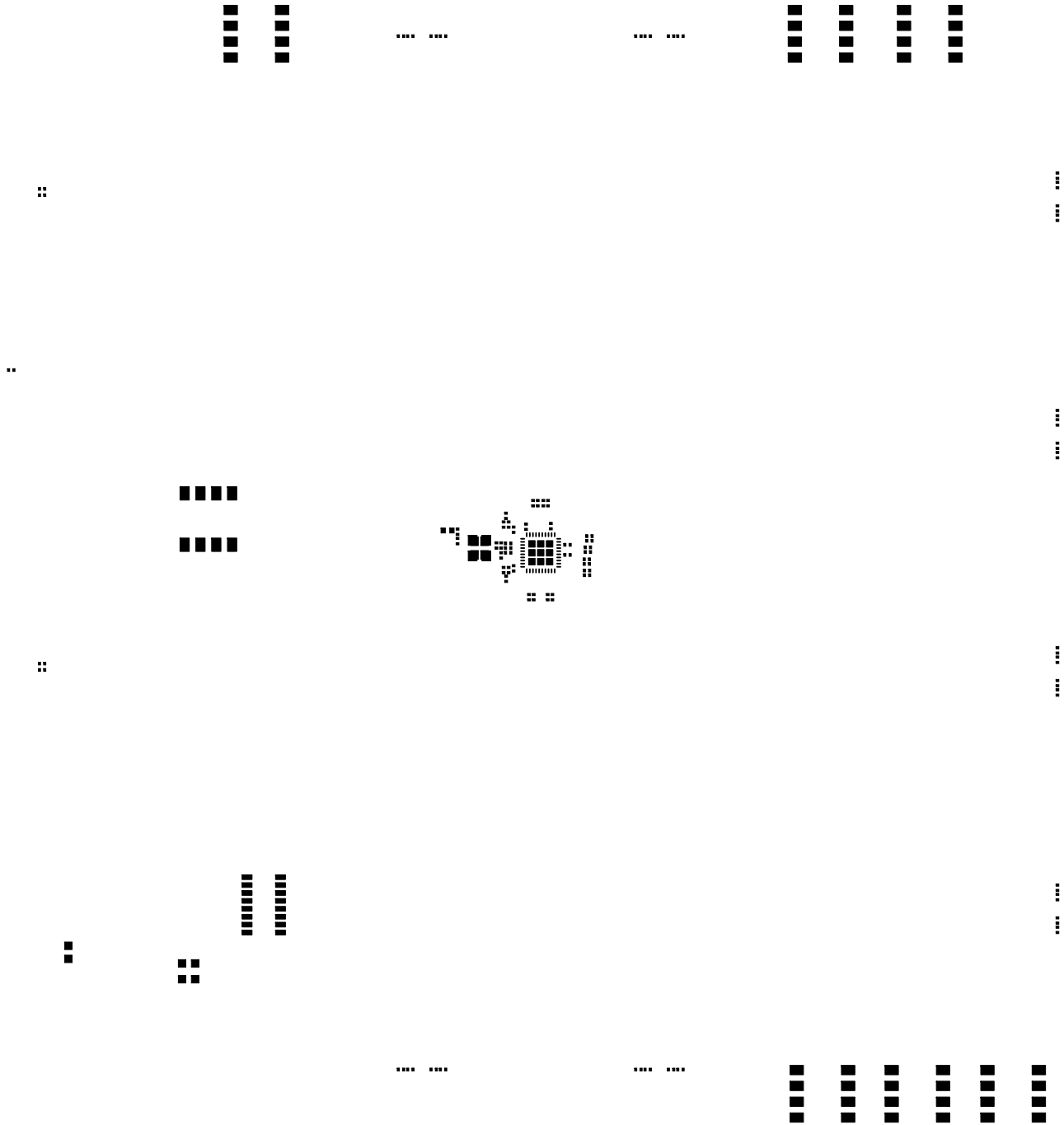
SECONDARY SIDE



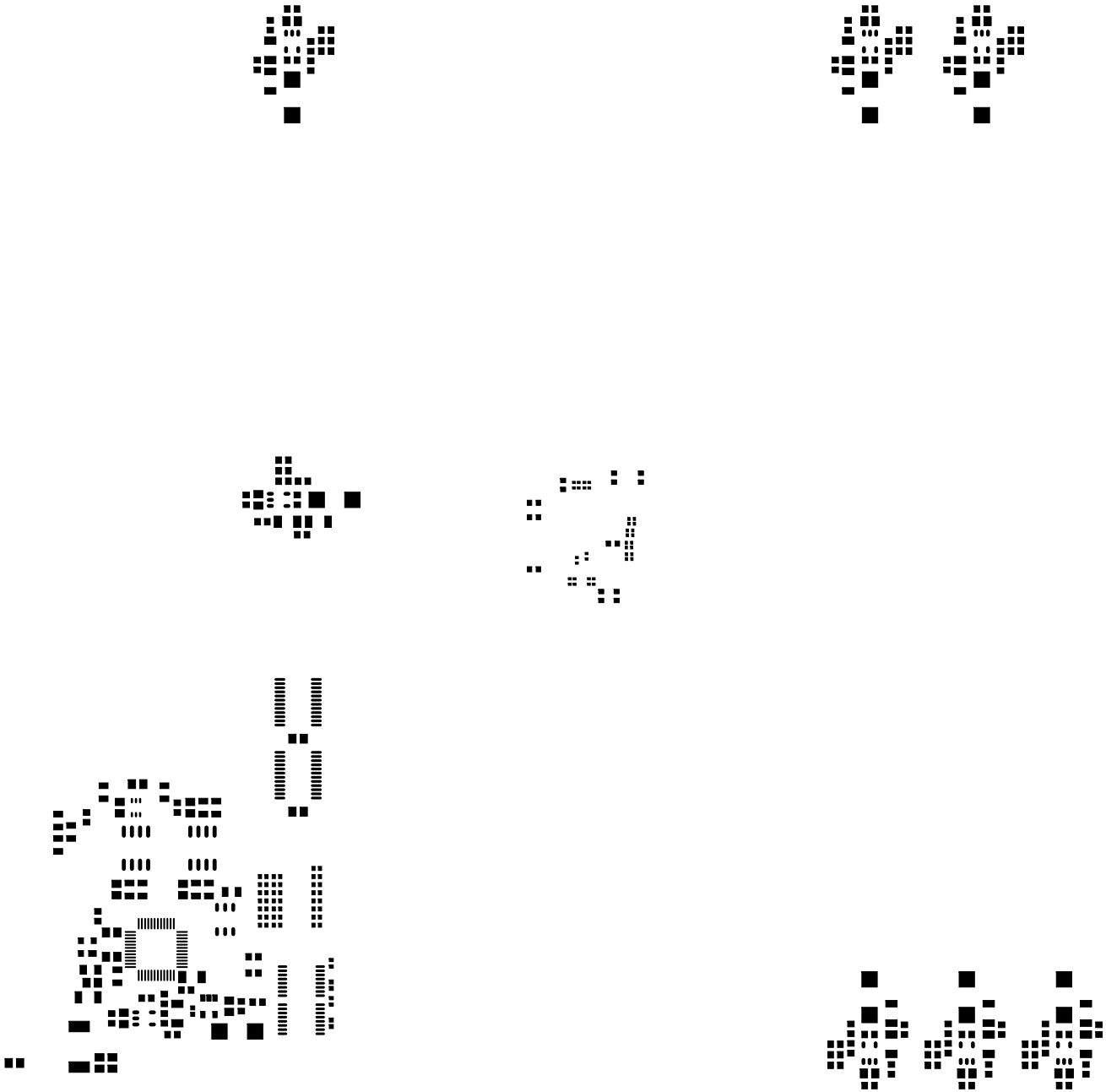
SECONDARY SOLDER MASK



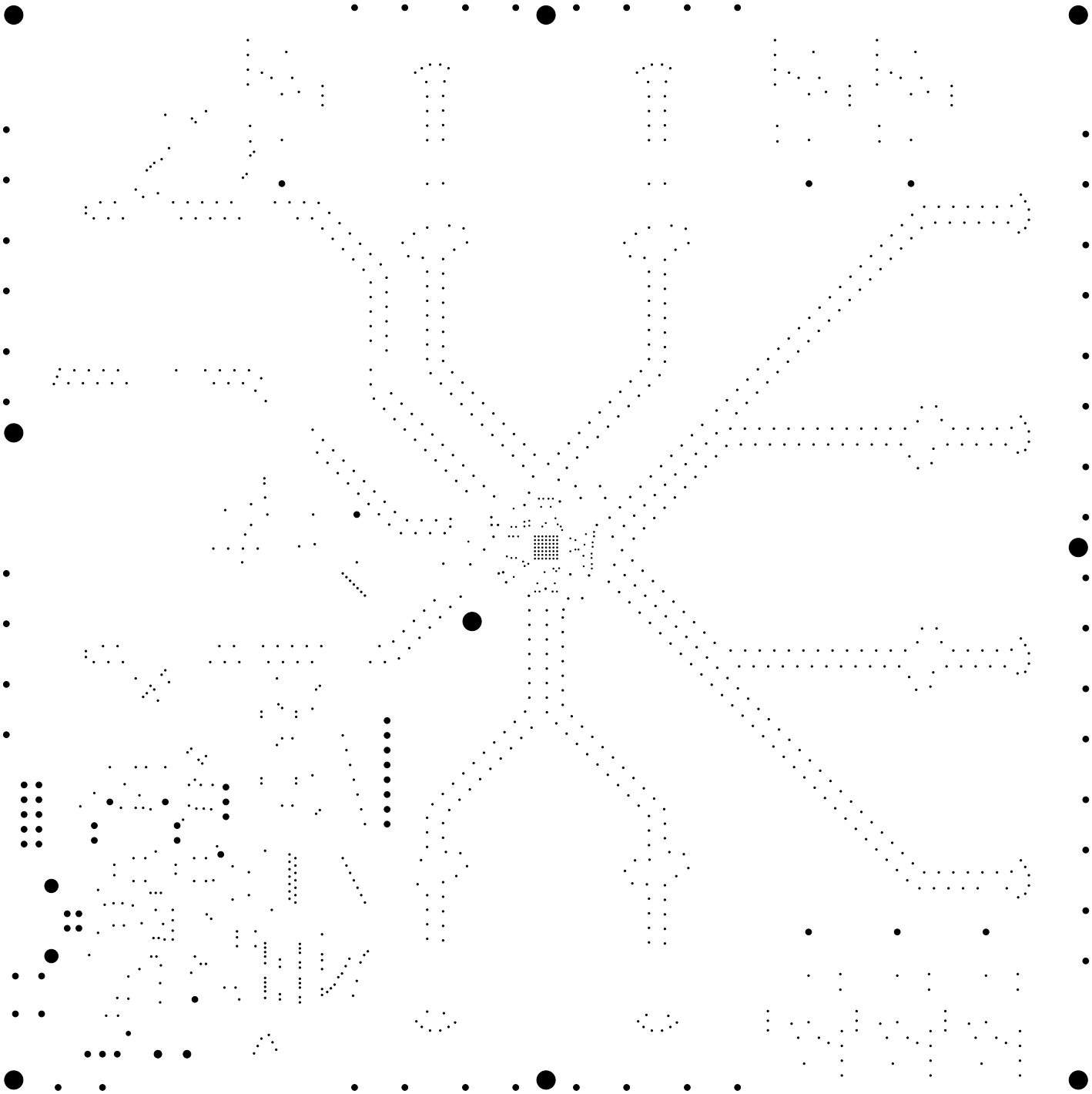
SECONDARY SILKSCREEN

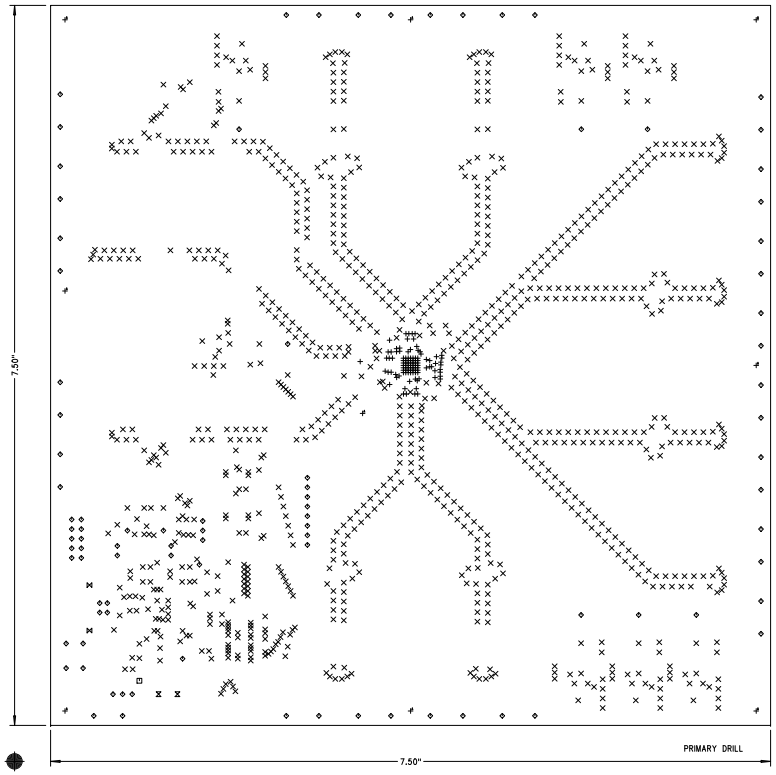


PRIMARY SOLDER PASTE



SECONDARY SOLDER PASTE





NOTES : UNLESS OTHERWISE SPECIFIED

1. MANUFACTURE IN ACCORDANCE WITH IPC-6012, TYPE 3, CLASS 2.
2. END PRODUCT FEATURES SHALL NOT VARY MORE THAN 20% FROM ARTWORK ORIGINALS.
* 3. LAMINATE AND PREPREG SHALL BE AS PER IPC-4101/26,83,98 WITH A DECOMPOSITION TEMPERATURE >= 345°C, COLOR, NATURAL.
4. COPPER WEIGHT SHALL BE 0.5 OZ./SQ. FT. BEFORE PLATING.
5. ALL PLATED THROUGH HOLES SHALL HAVE A MINIMUM OF 0.001" COPPER.
6. DRILL HOLE TOLERANCE AFTER PLATING SHALL BE ±0.003".
7. MINIMUM ANNULAR RING SHALL BE 0.001".
8. MINIMUM ANNULAR RING AT EMERGENT CONDUCTORS SHALL BE 0.003".
9. FINAL PCB THICKNESS SHALL BE 0.062" ±10%.
10. WARP/TWIST SHALL NOT EXCEED 1.0%
11. FINISH SHALL BE LPI, BLUE SMOBC, ENIG BOTH SIDES.
12. SILKSCREEN WITH NONCONDUCTIVE WHITE EPOXY INK.
13. INTERNAL 0.175MM TRACES TO BE 50 OHM Zo ±5%.
    EXTERNAL 0.275MM TRACES TO BE 50 OHM Zo. ±5%.
    EXTERNAL 0.660MM TRACES TO BE 50 OHM Zo ±5% REF TO L03.
14. VENDOR TO PROVIDE PCB MICRO-SECTION OF COUPON AREA & TDR TEST REPORT.
15. REFERENCE ADDITIONAL FAB NOTES IN FILE README.TXT

LAYER STACKUP	FILE NAMES
PRIMARY SILKSCREEN	5332-AM2-QFN40-CEVB_PSS.PHO
PRIMARY SOLDERMASK	5332-AM2-QFN40-CEVB_PSM.PHO
PRIMARY SIDE	5332-AM2-QFN40-CEVB_PRI.PHO
* 370HR	5.7MIL THK
GROUND PLANE	5332-AM2-QFN40-CEVB_L02.PHO
* 370HR	8MIL THK
GROUND PLANE	5332-AM2-QFN40-CEVB_L03.PHO
FR-4 IPC-4101/26,83,98	9.64MIL THK
DIG ROUTE/GND	5332-AM2-QFN40-CEVB_L04.PHO
FR-4 IPC-4101/26,83,98	8MIL THK
DIG ROUTE, VDDOx, GND	5332-AM2-QFN40-CEVB_L05.PHO
FR-4 IPC-4101/26,83,98	9.64MIL THK
GROUND PLANE	5332-AM2-QFN40-CEVB_L06.PHO
* 370HR	8MIL THK
RF ROUTE/GND	5332-AM2-QFN40-CEVB_L07.PHO
* 370HR	5.7MIL THK
SECONDARY SIDE	5332-AM2-QFN40-CEVB_SEC.PHO
SECONDARY SOLDERMASK	5332-AM2-QFN40-CEVB_SSM.PHO
SECONDARY SILKSCREEN	5332-AM2-QFN40-CEVB_SSS.PHO

0.062" THK

SCALE: NONE

SIZE	QTY	SYM	PLT	TOOL	TOL
0.008	106	+	P	1	+0/-0.008
0.012	1033	×	P	2	+0/-0.012
0.030	1	□	P	3	+/-0.003
0.040	91	◇	P	4	+/-0.003
0.052	2	⧖	P	5	+/-0.003
0.091	2	⋈	P	6	+/-0.003
0.125	9	A	N	7	+/-0.003

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES AND APPLY AFTER FINISH
DIMENSIONS IN BRACKETS [ ] ARE IN MILLIMETERS
INTERPRET DRAWING PER ML-D-1000
TOLERANCES
HOLE TOLERANCES PER 78027
DECIMALS .XX +/- .XXX +/- | ANGLES +/- | SURFACES MICROINCHES
PART TO BE FREE OF BURRS
BREAK EDGES MAX | BEND RADIUS MAX | BEND RELIEF MAX

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DESIGN	TS	26JAN2019
LAYOUT	AA	26JAN2019

DO NOT SCALE DRAWING

COMPANY: SILICON LABS
400 W CESAR CHAVEZ ST.
AUSTIN, TX 78701
(512)416-8500
www.silabs.com

NAME: Si5332-AM2-QFN40-EVB
REV : 1.0
SIZE C | PART NUMBER:
SCALE 1:1 | FABRICATION DRAWING | SHEET 1 OF 1