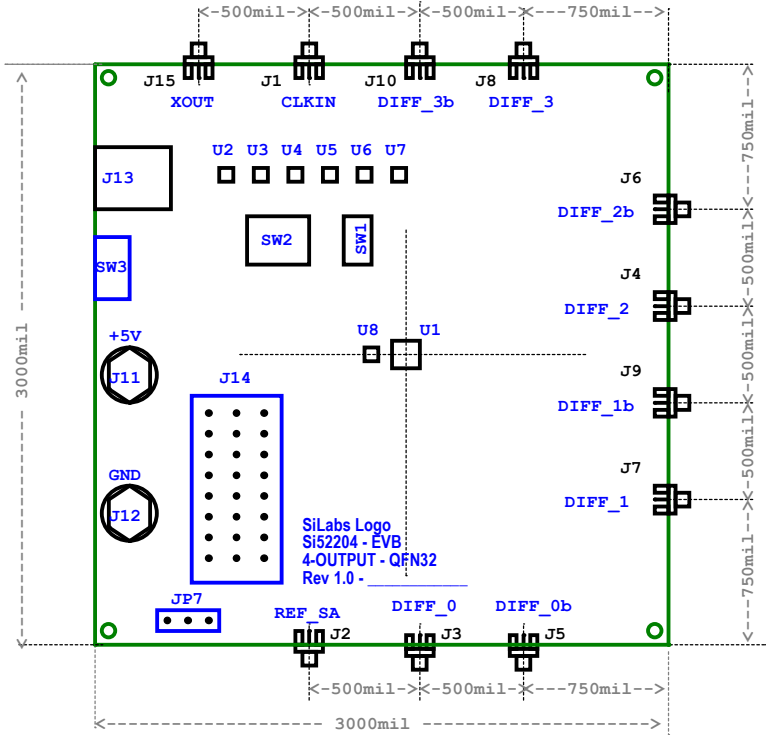


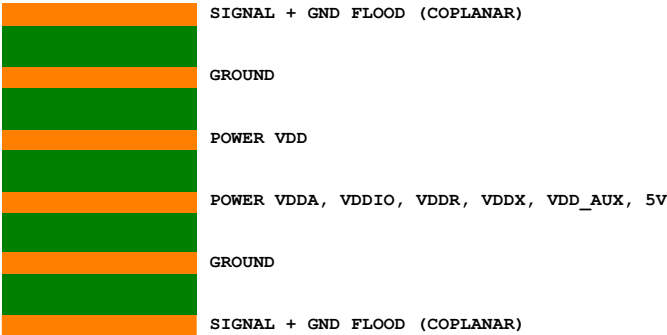
MECHANICAL & FABRICATION



BOARD MATERIAL:

- Use FR-406, DK=3.9
- Use 1.0oz copper thickness for power & ground planes and 0.5oz thickness for RF signal layers

6 BOARD LAYERS:



Total Board Thickness:
62 mil

DUT CONNECTIONS

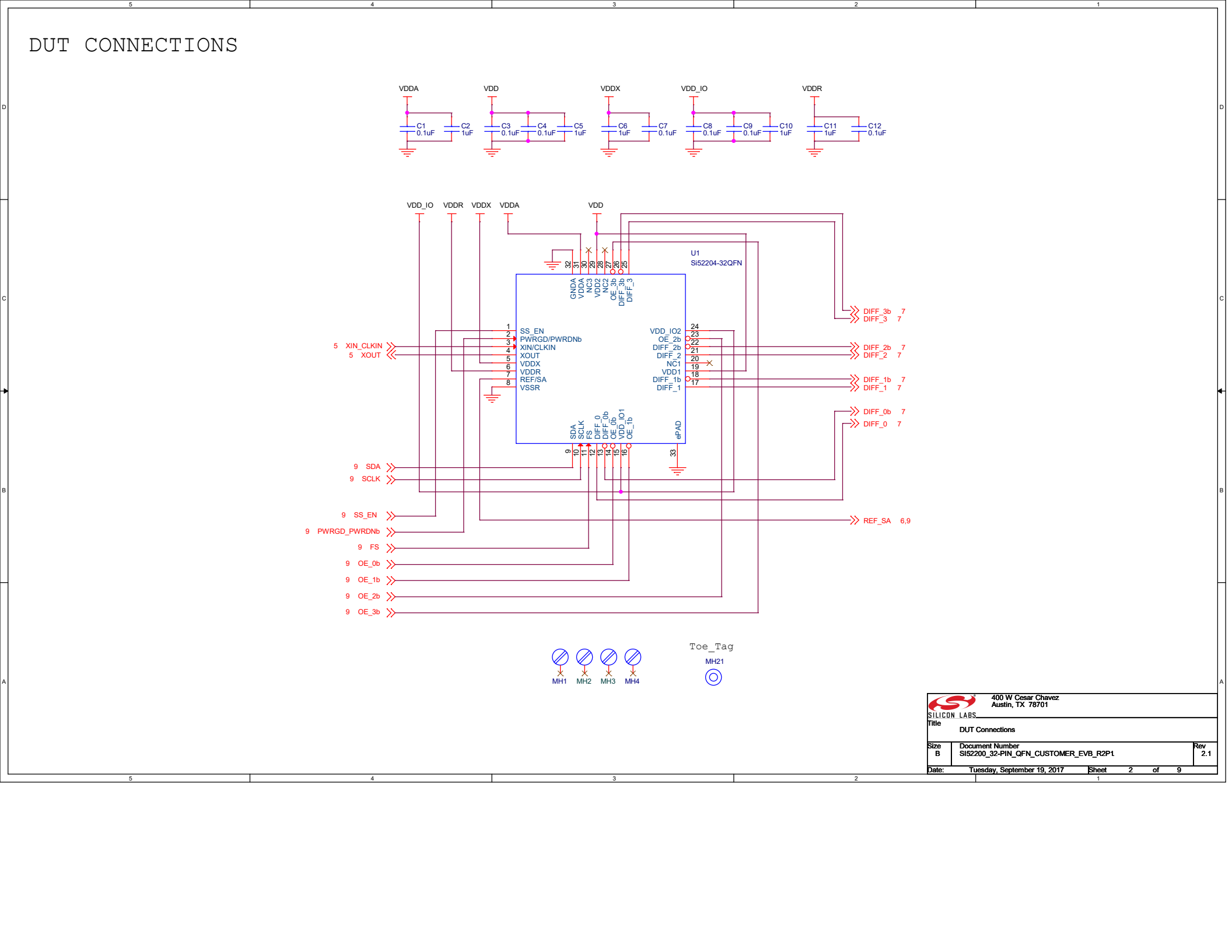
The diagram illustrates the internal pin connections of the Si52204-32QFN chip. The chip is shown with its pins numbered 1 through 33. The connections are as follows:

- Power Supply Pins:**
 - VDDA: Connected to pin 30.
 - VDD: Connected to pin 31.
 - VDDX: Connected to pin 28.
 - VDD_IO: Connected to pin 27.
 - VDDR: Connected to pin 26.
- Signal Pins:**
 - XIN_CLKIN: Connected to pin 1.
 - XOUT: Connected to pin 2.
 - SS_EN: Connected to pin 3.
 - PWRGD_PWRDNb: Connected to pin 4.
 - FS: Connected to pin 5.
 - OE_0b: Connected to pin 6.
 - OE_1b: Connected to pin 7.
 - OE_2b: Connected to pin 8.
 - OE_3b: Connected to pin 9.
- Differential Signal Pins:**
 - DIFF_0b: Connected to pin 10.
 - DIFF_1b: Connected to pin 11.
 - DIFF_2b: Connected to pin 12.
 - DIFF_3b: Connected to pin 13.
- Other Pins:**
 - NC1: Connected to pin 14.
 - NC2: Connected to pin 15.
 - NC3: Connected to pin 16.
 - NC4: Connected to pin 17.
 - NC5: Connected to pin 18.
 - NC6: Connected to pin 19.
 - NC7: Connected to pin 20.
 - NC8: Connected to pin 21.
 - NC9: Connected to pin 22.
 - NC10: Connected to pin 23.
 - NC11: Connected to pin 24.
 - NC12: Connected to pin 25.
 - NC13: Connected to pin 26.
 - NC14: Connected to pin 27.
 - NC15: Connected to pin 28.
 - NC16: Connected to pin 29.
 - NC17: Connected to pin 30.
 - NC18: Connected to pin 31.
 - NC19: Connected to pin 32.
 - NC20: Connected to pin 33.

External components and connections are shown at the bottom of the diagram:

- Capacitors: C1, C2, C3, C4, C5, C6, C7, C8, C9, C10, C11, C12.
- Temperature Sensor: MH21.
- Other components: MH1, MH2, MH3, MH4.

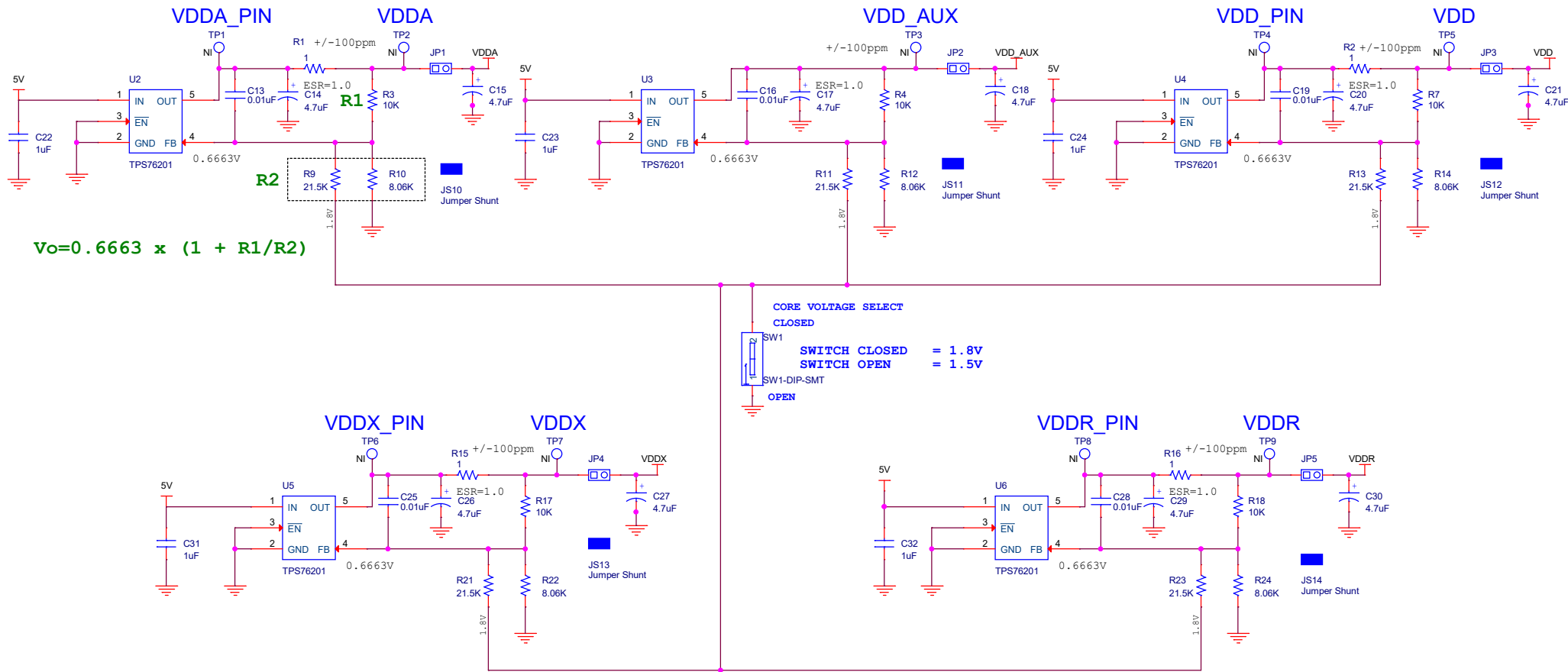
The diagram is titled "DUT CONNECTIONS" and is part of a document titled "Si52204-32QFN_CUSTOMERS_EVB_R2P1". The document is dated Tuesday, September 19, 2017, and is sheet 2 of 9.




100 mA Adjustable Voltage Regulator

Text in BLUE should
be added to TOP SILK

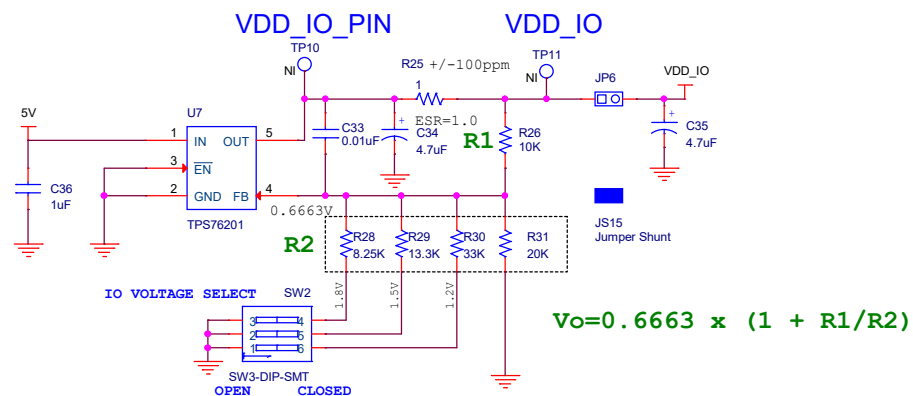
Group JP1:JP6 together



Identify Pin1 of all jumpers and IC's!

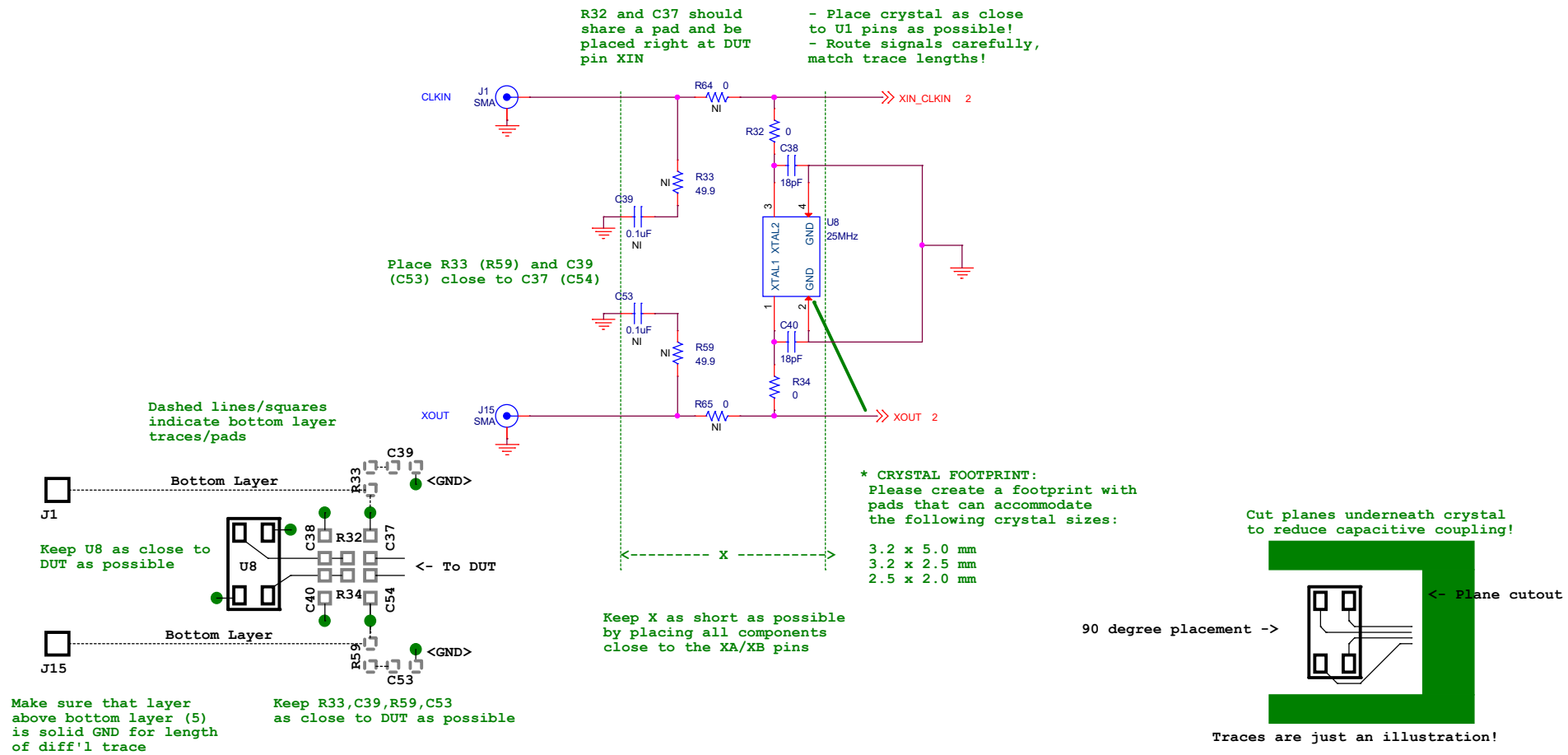
		400 W Cesar Chavez Austin, TX 78701	
SILICON LABS.		Title	
Size B		Output Voltage Regulators	
Document Number		Rev 2.1	
SI52200_32-PIN_QFN_CUSTOMER_EVB_R2P1		Date: Tuesday, September 19, 2017	
Sheet 3 of 9		1	

100 mA Adjustable Voltage Regulator

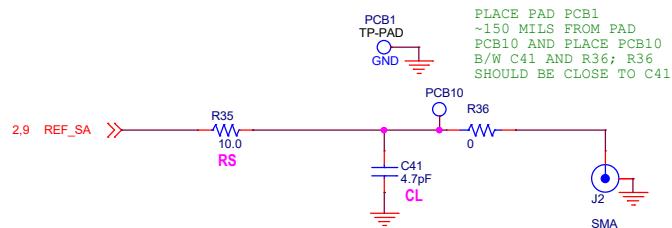


SW2-1	SW2-2	SW2-3	VDD_IO
OPEN	OPEN	OPEN	1.0V
CLOSED	OPEN	OPEN	1.2V
OPEN	CLOSED	OPEN	1.5V
OPEN	OPEN	CLOSED	1.8V

Crystal/Input Clock Connections



OUTPUT CONNECTIONS, PART 1

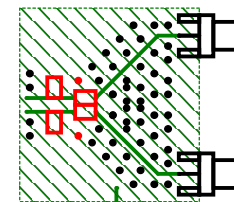


<- This is the only single-ended output

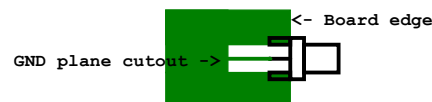
Place RS as close to the DUT pin as possible
Make total trace length = 5" (from DUT pin to CLoad);

Place isolation resistor right by load cap;

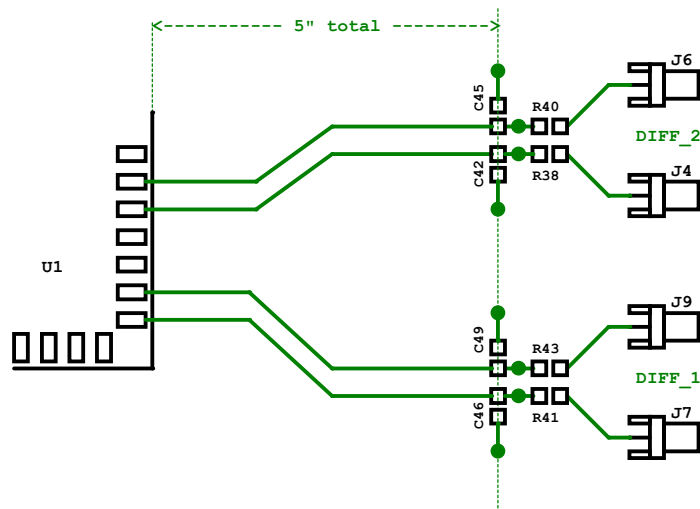
Flood top and bottom layers with copper as shown



SMA FOOTPRINT NOTE:
Make sure pad for center pin on SMA matches exactly
the actual width of the center pin in order to improve performance



A sufficient number of via holes connected
to ground should be used around all input/output
traces!

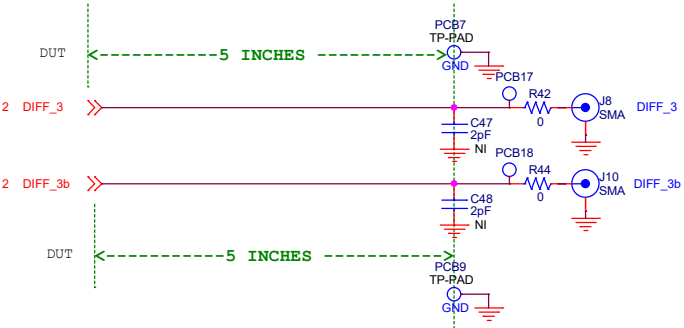
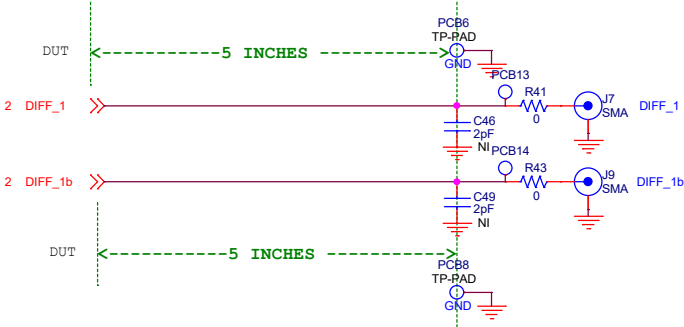
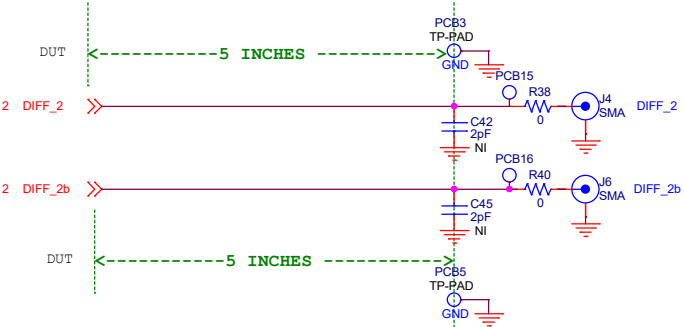
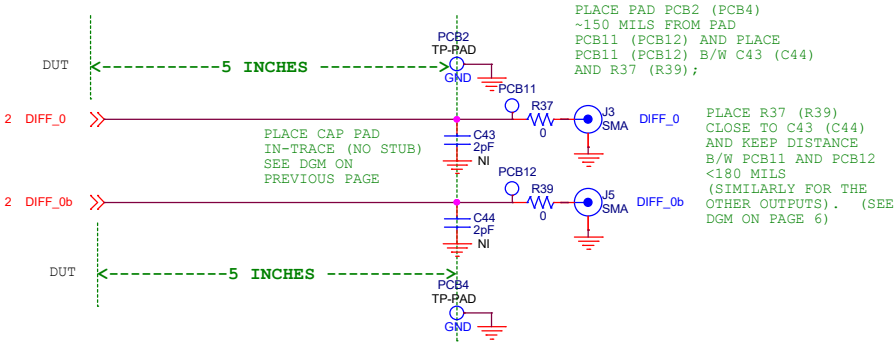


OUTPUT SIGNALS LAYOUT NOTES - APPLIES TO THIS PAGE AND NEXT PAGE AS WELL!
(Refer to image on left):

- ROUTING: route each differential pair loosely coupled. Serpentine to length and preserve symmetry on diff. pair. Keep distance b/w serpentine traces at least 5w apart and use arcs rather than 45's
- IMPEDANCE: all traces to have 50 ohms of controlled impedance
- In order to reduce capacitance please cut-out ground planes underneath the microstrip launches on the SMA connectors as needed
- GEOMETRY: maintain the trace symmetry across all output differential pairs
- TOPOLOGY: use microstrip for all traces
- COMPONENT PLACEMENT:
 - Separate each pair of SMA connectors by 500 mils between them (center to center, and also pair to pair)

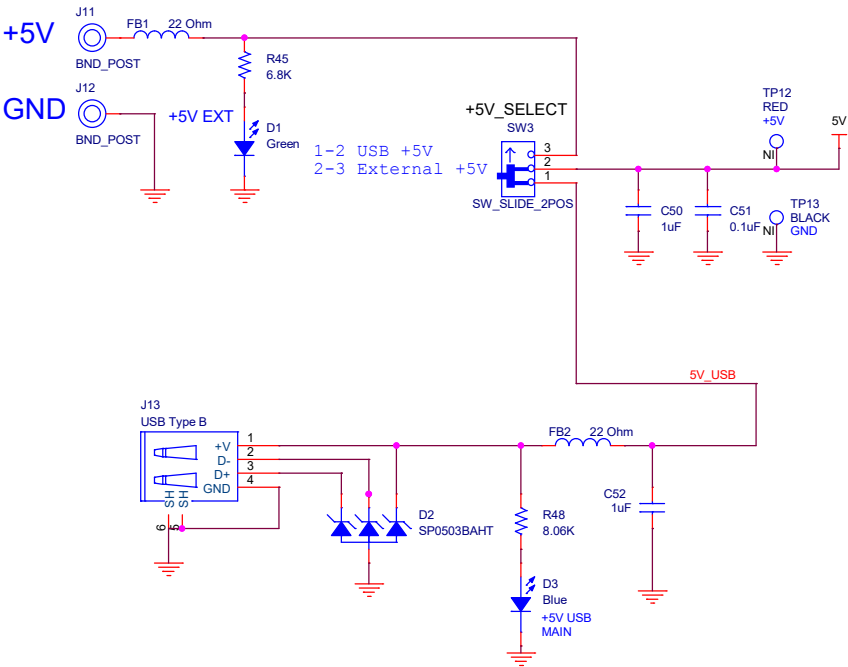
		400 W Cesar Chavez Austin, TX 78701
SILICON LABS.		
Title		
Output Connections		
Size	Document Number	Rev
B	SI52200_32-PIN_QFN_CUSTOMER_EVB_R2P1	2.1
Date:	Tuesday, September 19, 2017	Sheet 6 of 9

OUTPUT CONNECTIONS

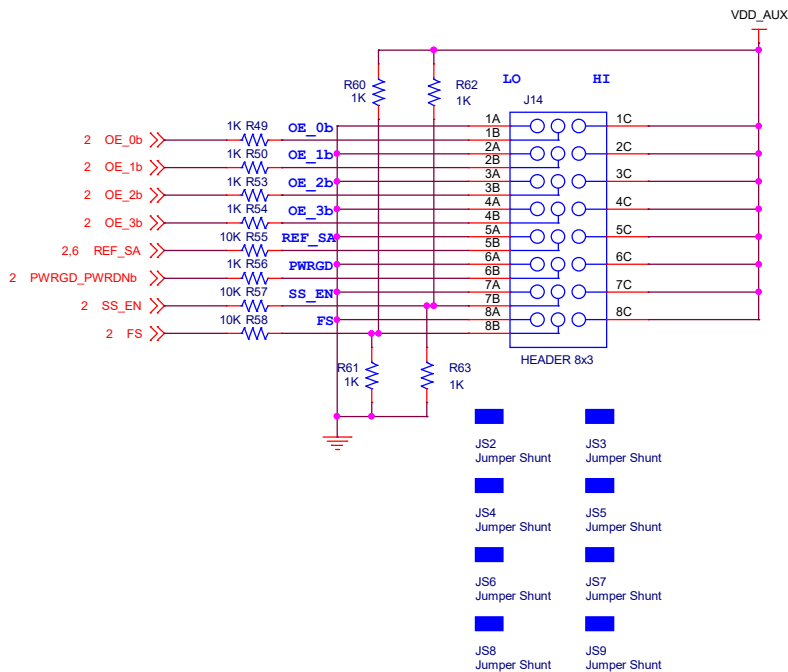


External Power

+5V Input Select



DC Inputs/I2C Access



	LO	NONE	HI
OE_0b	Enable	Enable	Disable
OE_1b	Enable	Enable	Disable
OE_2b	Enable	Enable	Disable
OE_3b	Enable	Enable	Disable
REF_SA	0xD2		0xD4
PWRGD	PWR DN	ACTIVE	ACTIVE
SS_EN	-0.25%	OFF	-0.50%
FS	100MHz	200MHz	133MHz

