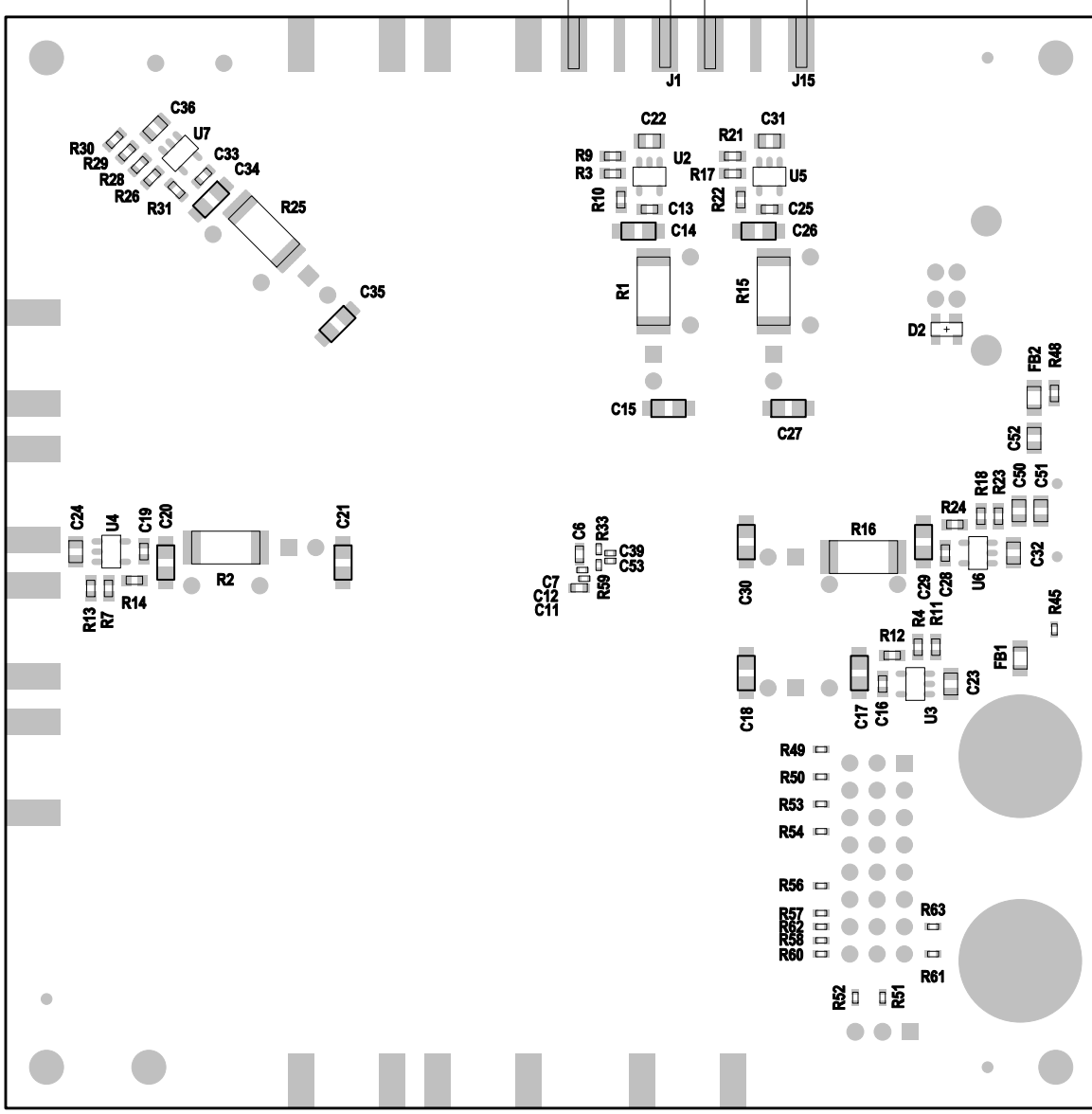
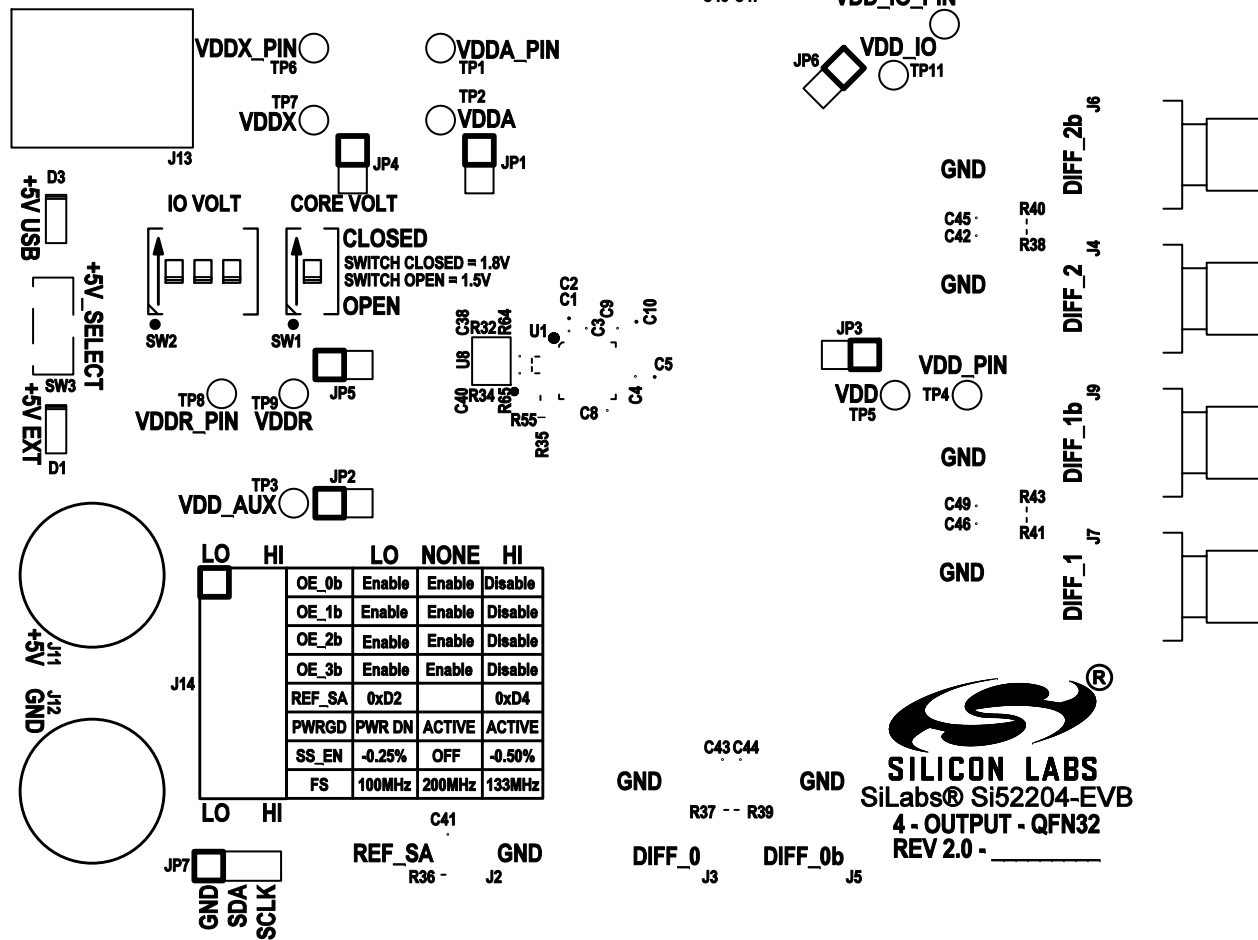


SECONDARY SILKSCREEN
SECONDARY SIDE



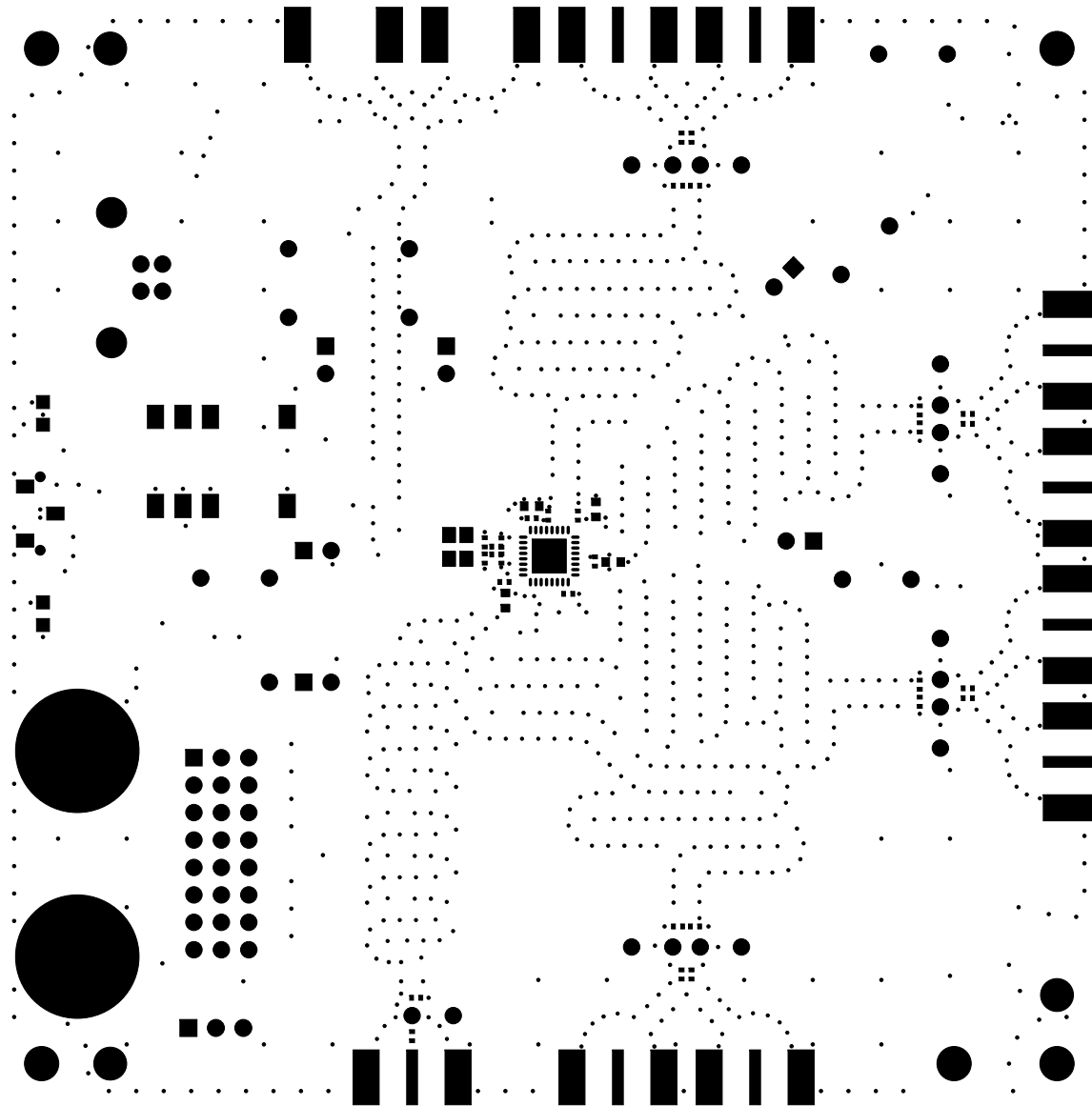


IO VOLT TABLE			
SW2-1	SW2-2	SW2-3	VDD_IO
OPEN	OPEN	OPEN	1.0V
CLOSED	OPEN	OPEN	1.2V
OPEN	CLOSED	OPEN	1.5V
OPEN	OPEN	CLOSED	1.8V

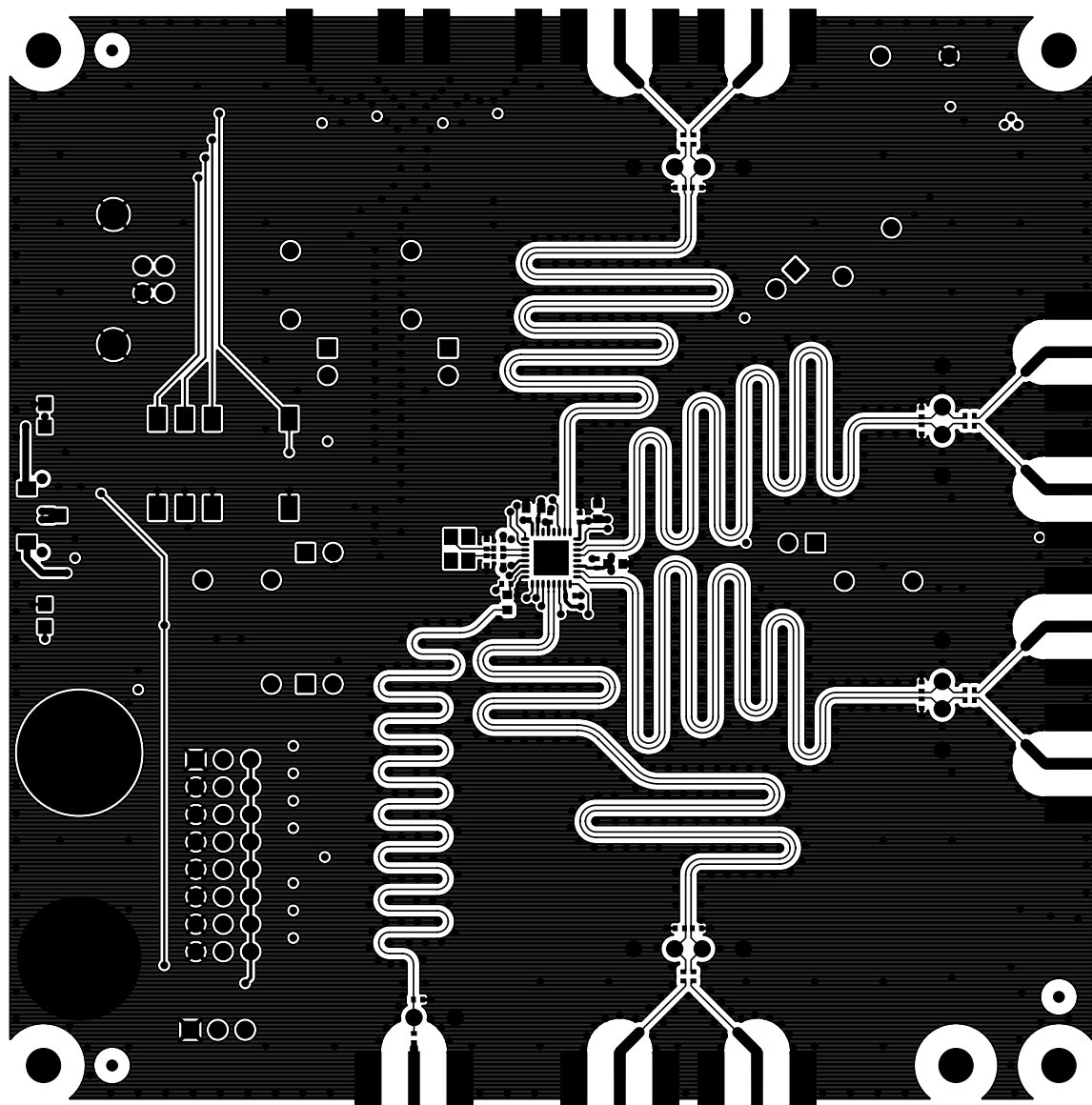



SILICON LABS
SiLabs® Si52204-EVB
4 - OUTPUT - QFN32
REV 2.0 - _____



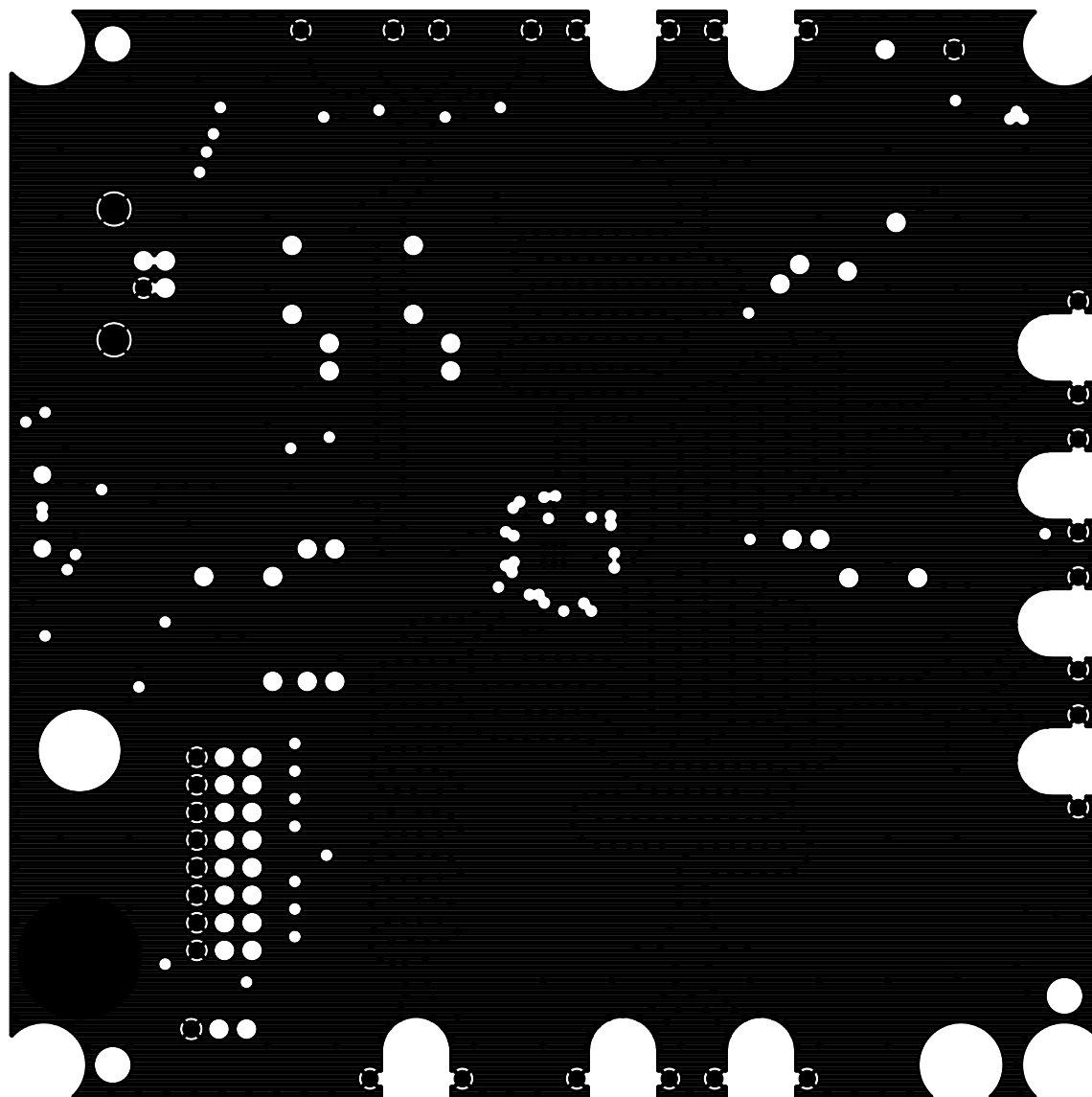


PRIMARY SOLDER MASK

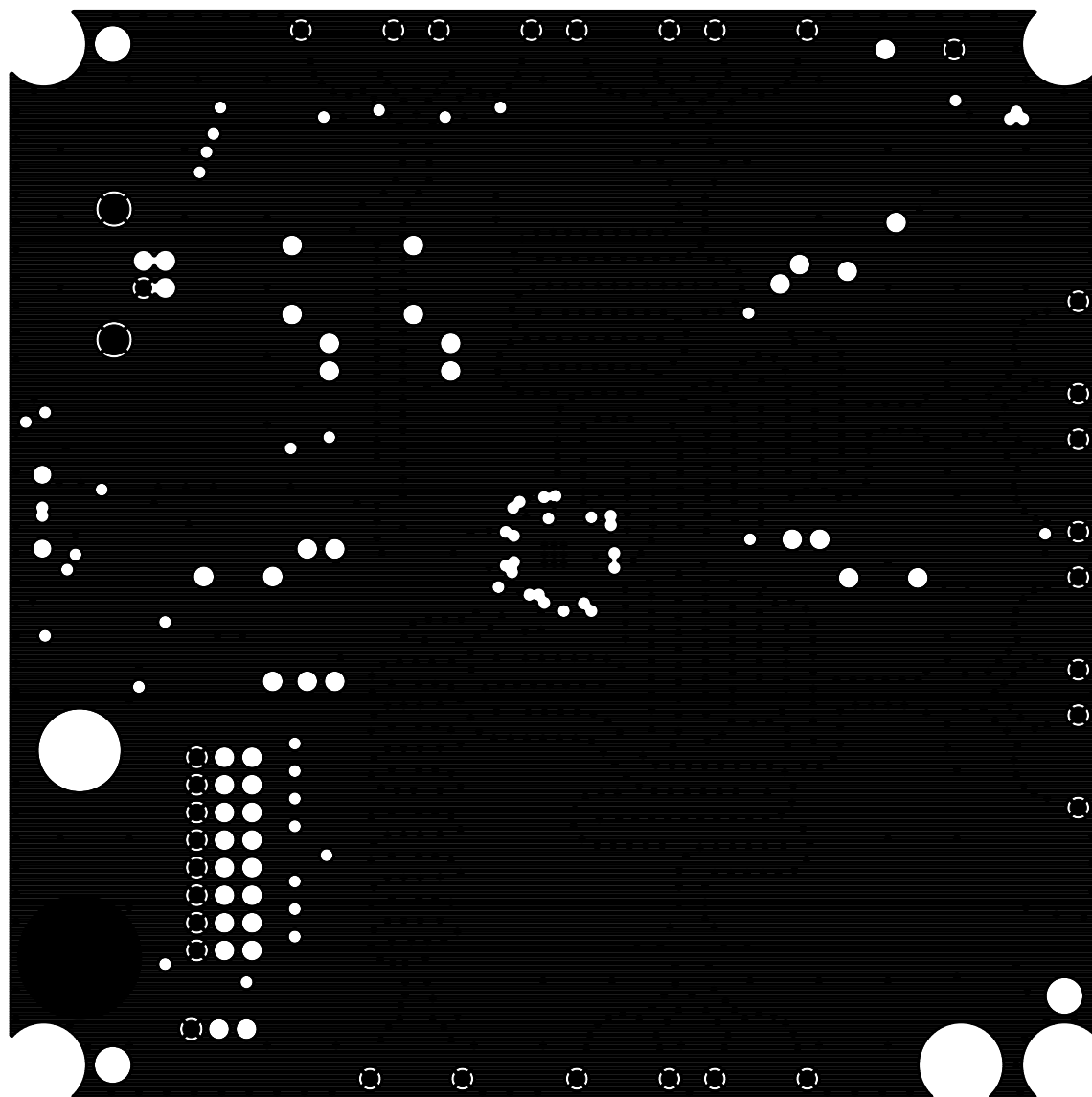


PRIMARY SIDE

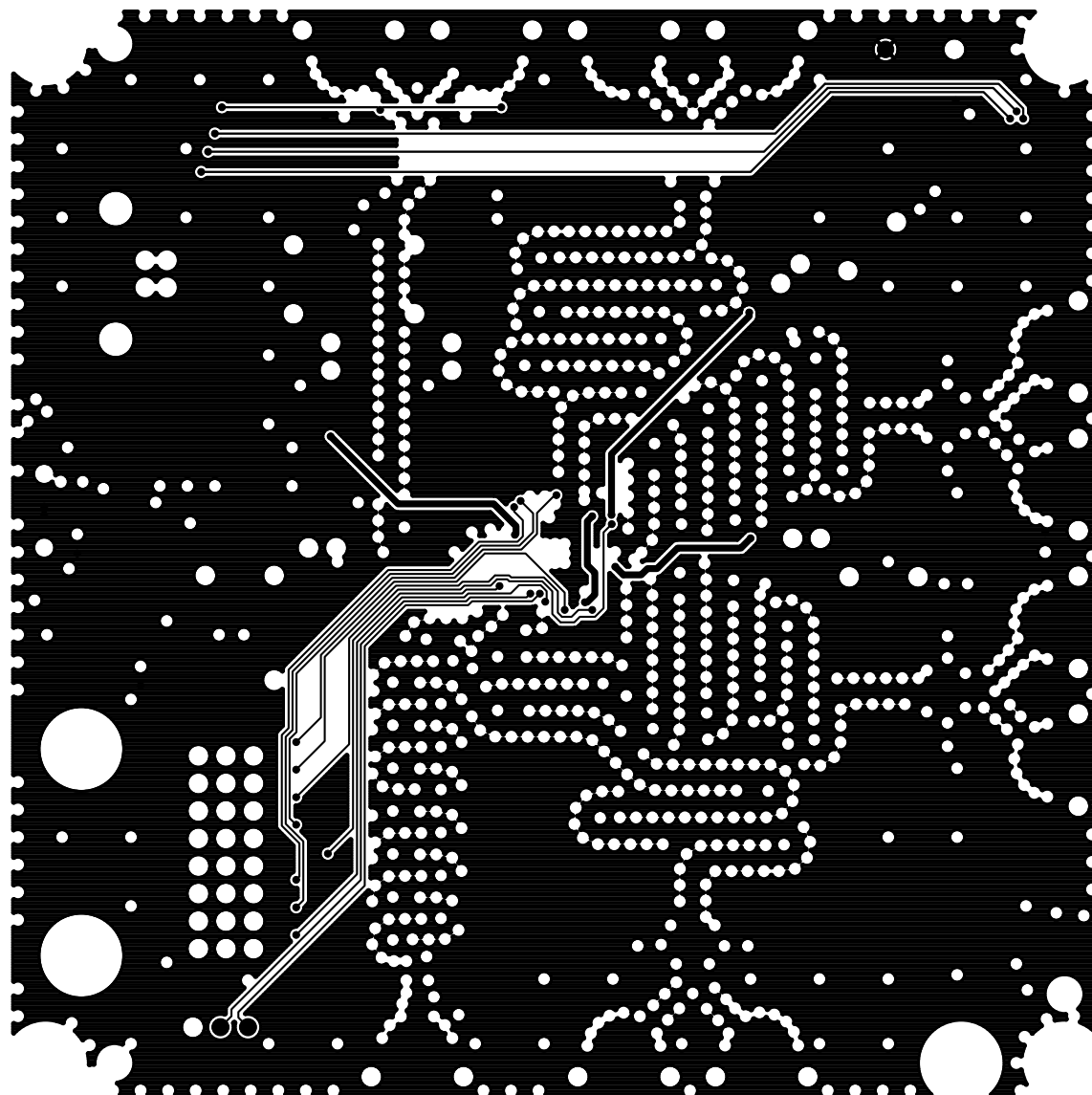




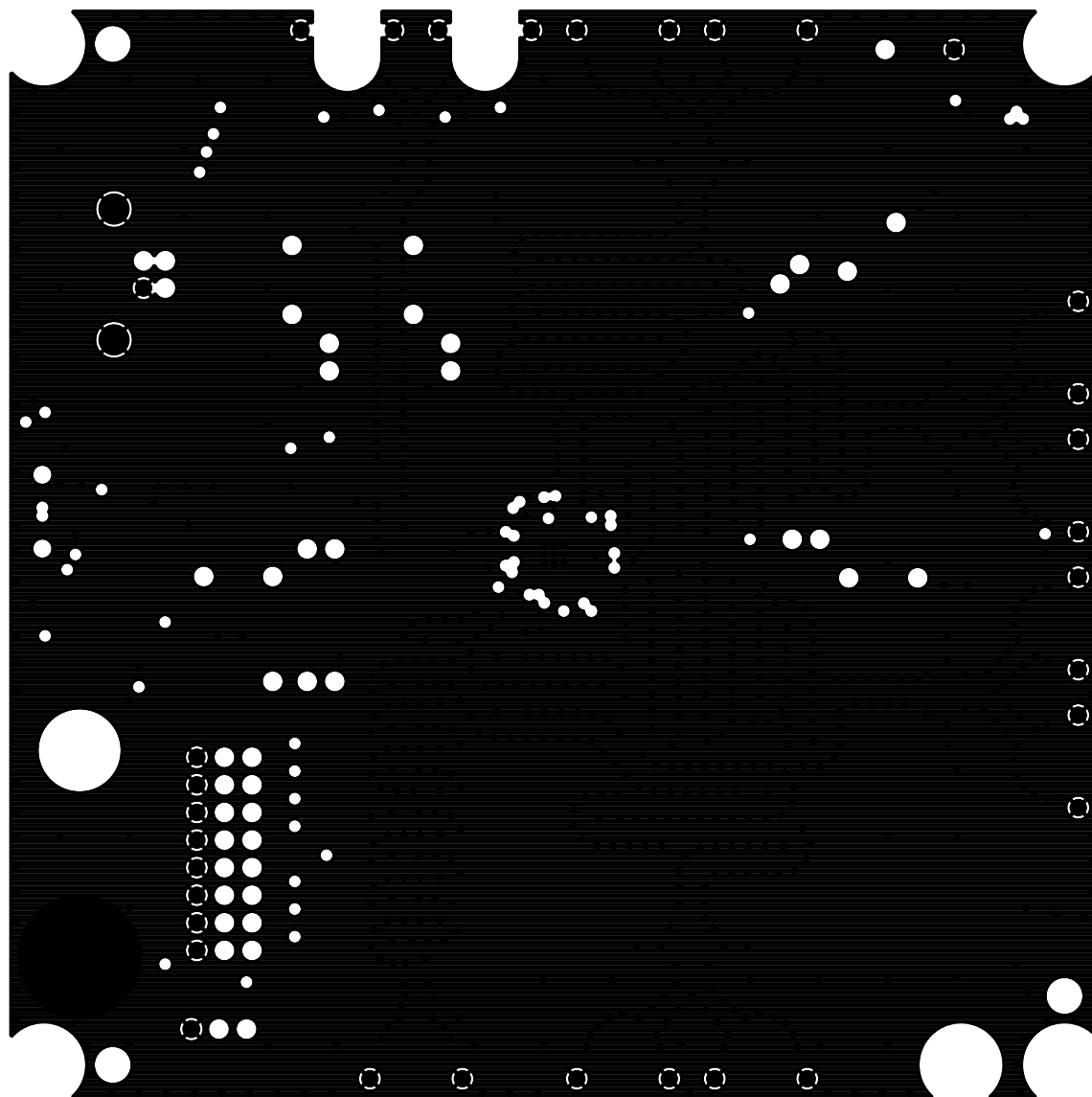
L02 (GROUND PLANE)



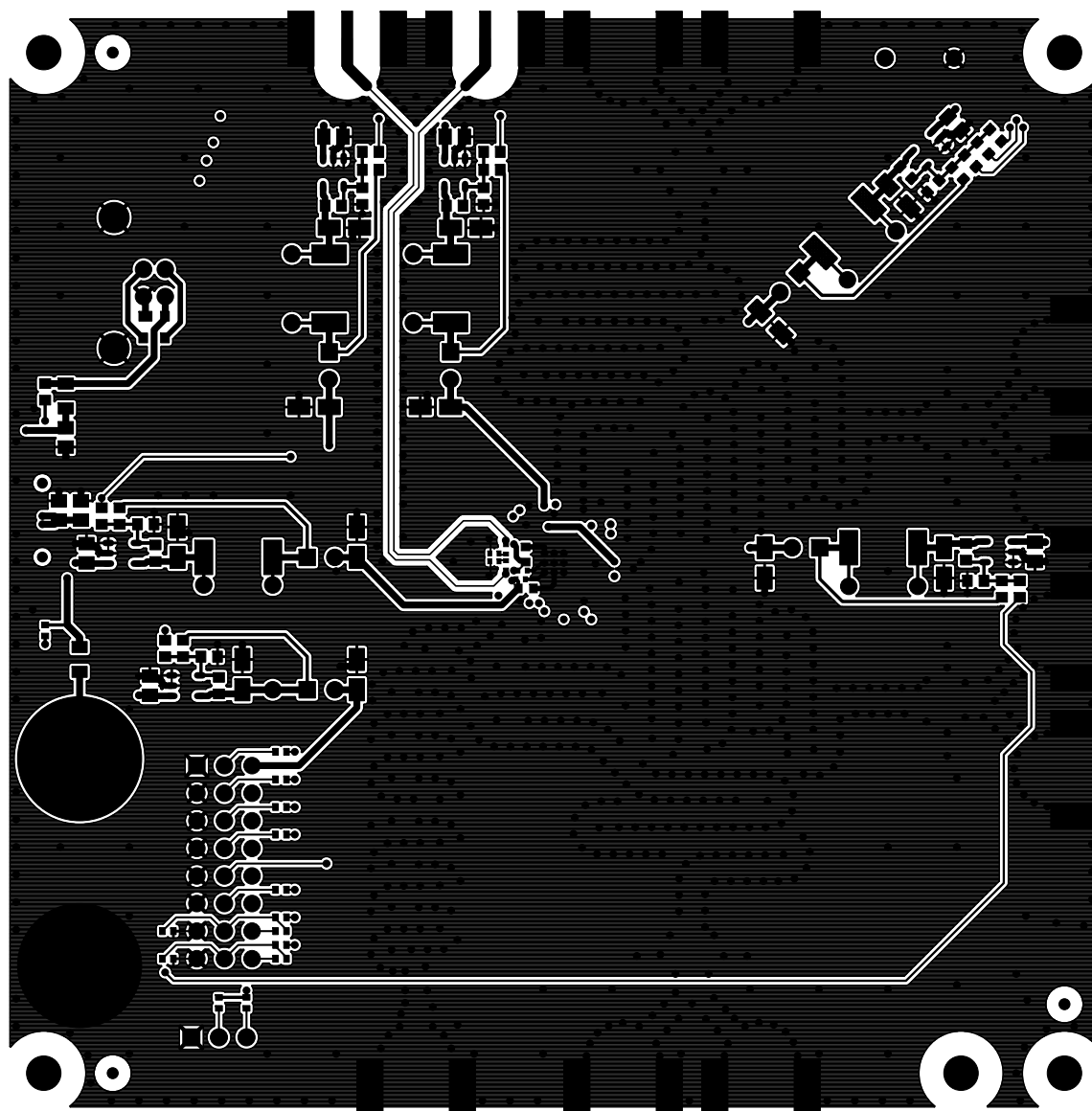
L03 (GROUND PLANE)



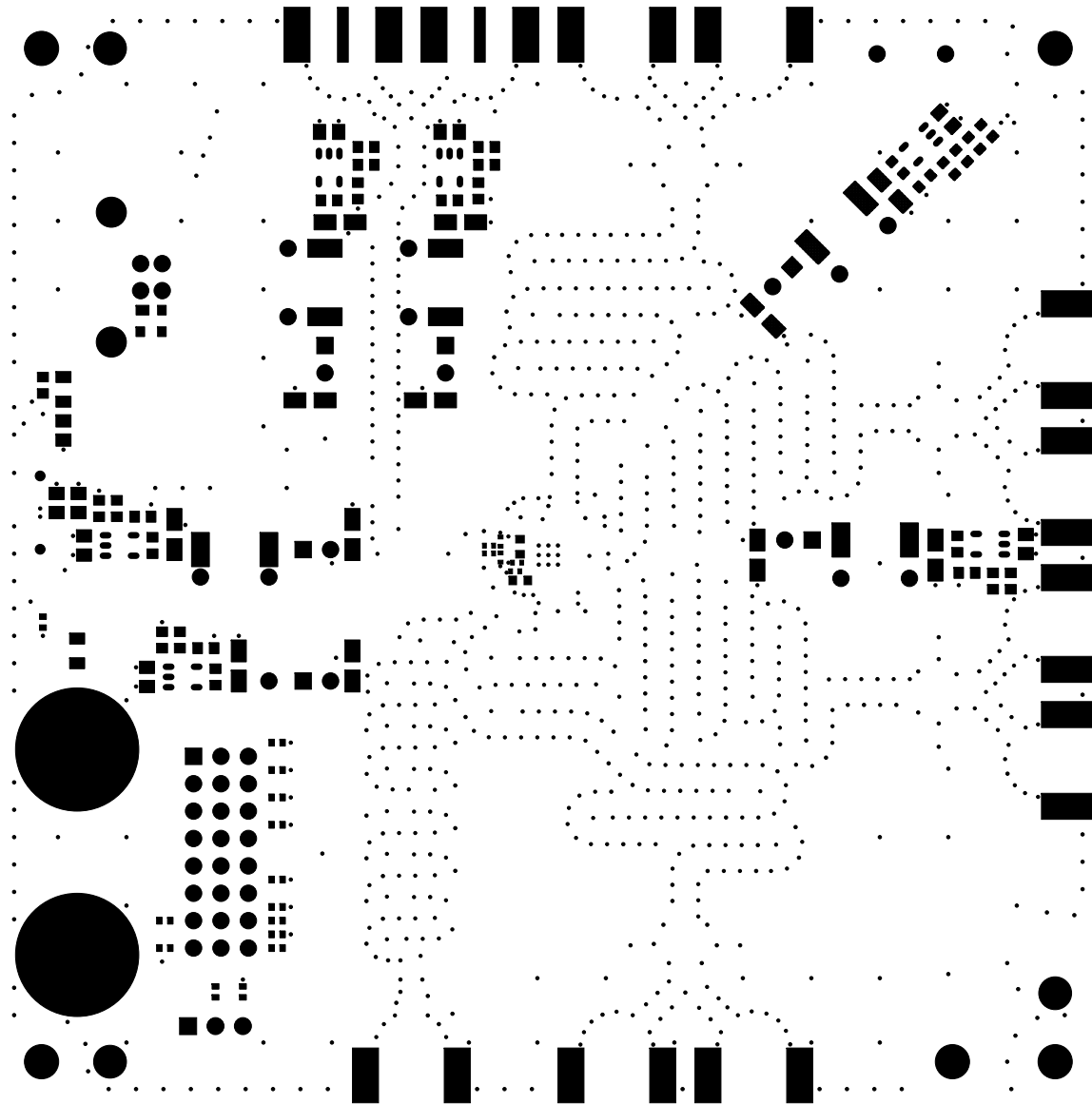
L04 (+5V/ROUTE)



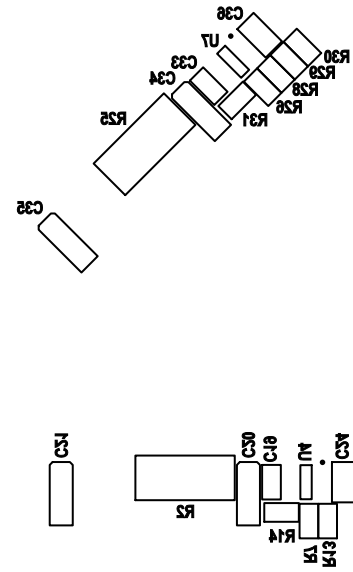
L05 (GROUND PLANE)



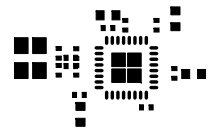
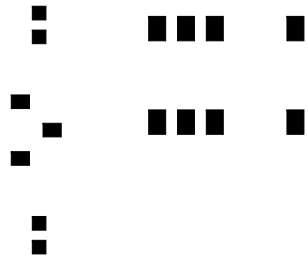
SECONDARY SIDE



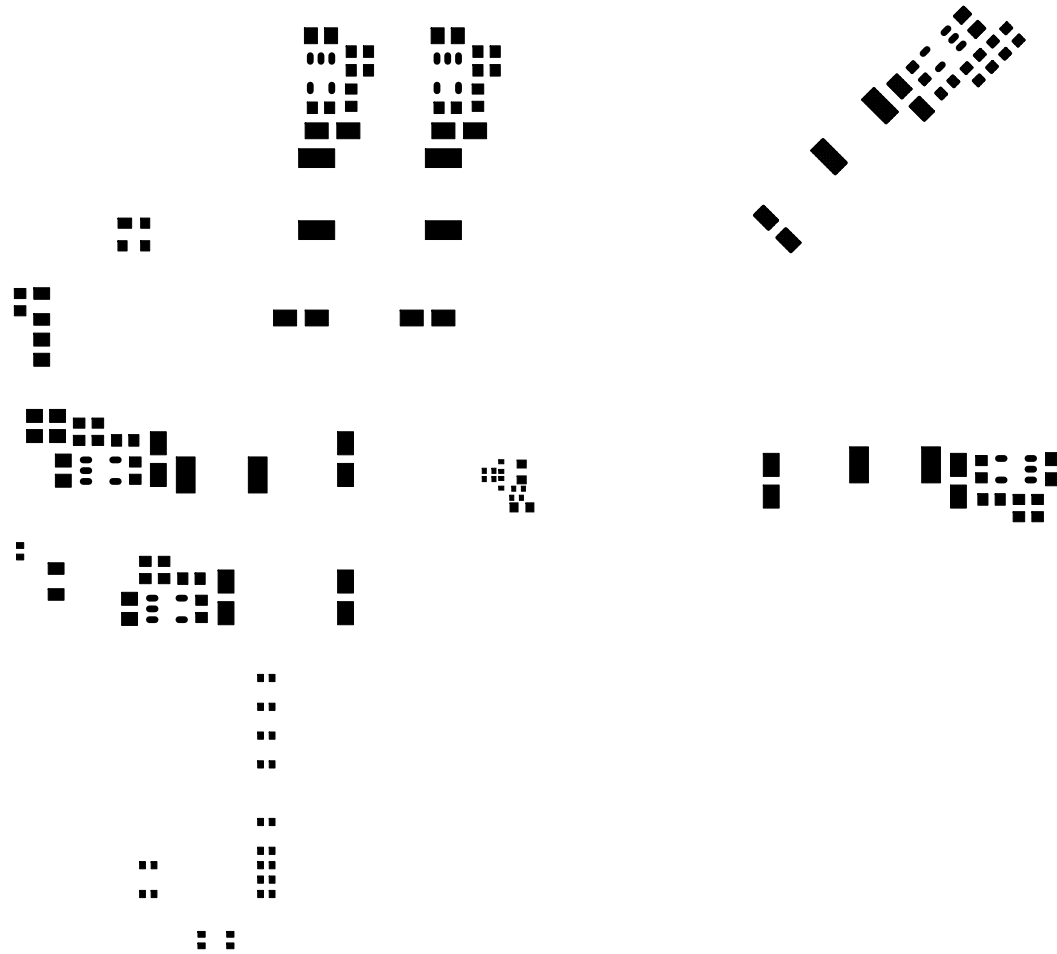
SECONDARY SOLDER MASK



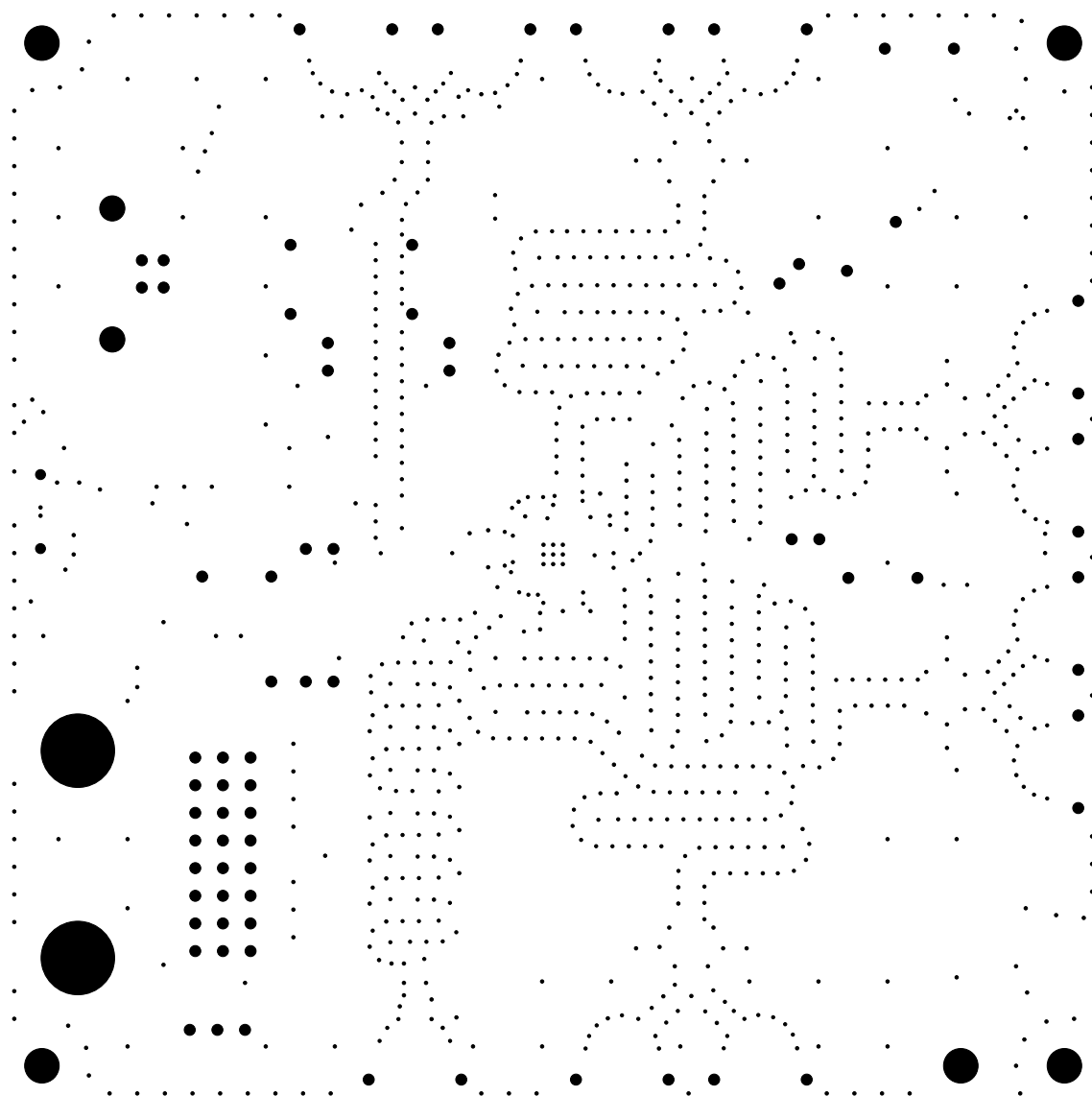
SECONDARY SILKSCREEN

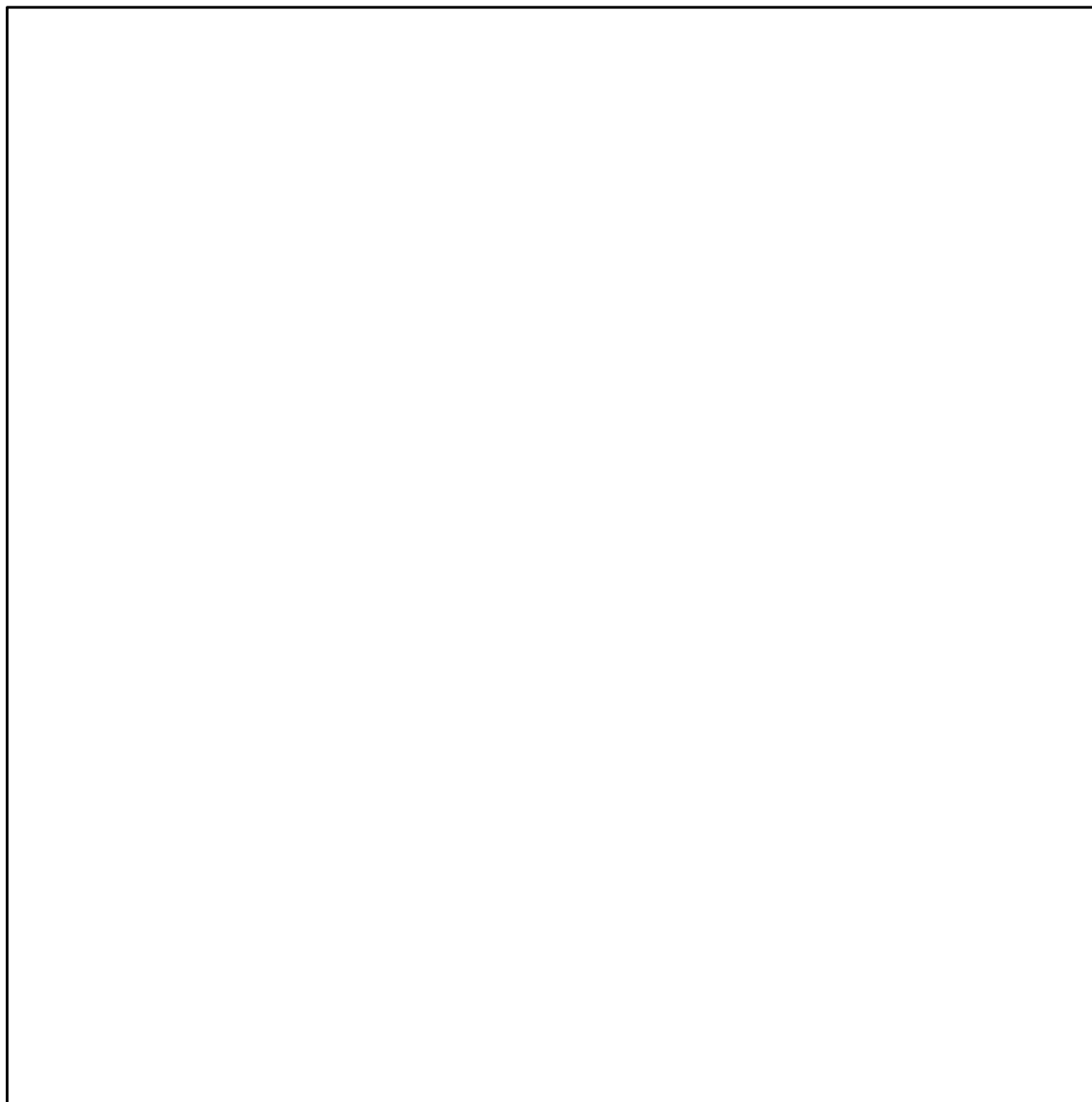


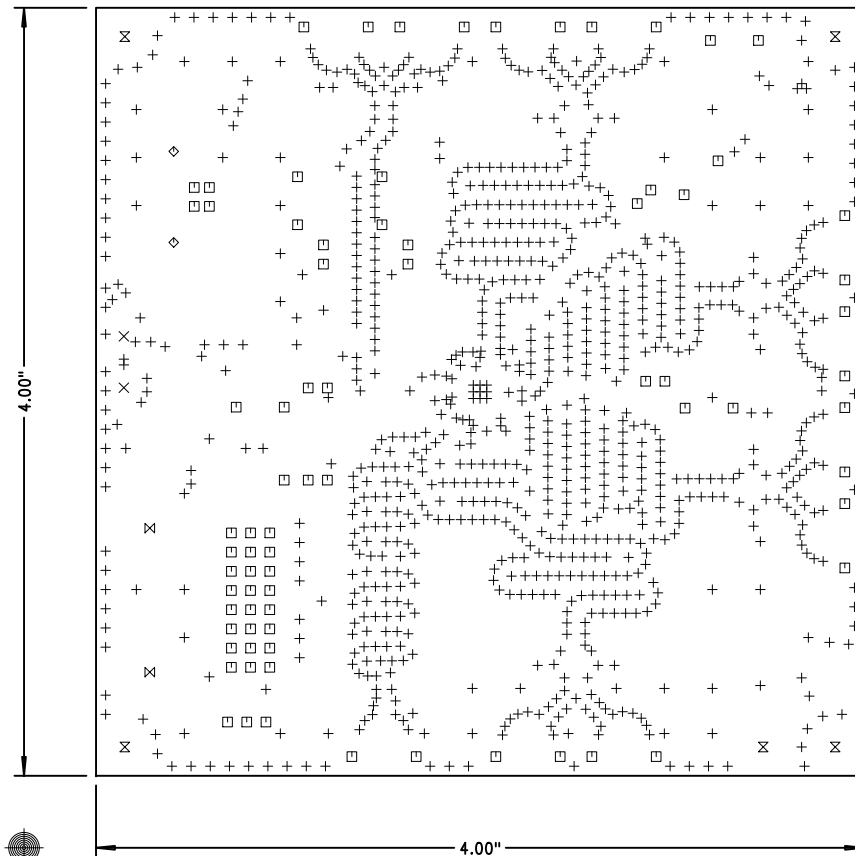
PRIMARY SOLDER PASTE



SECONDARY SOLDER PASTE







PRIMARY DRILL



NOTES : UNLESS OTHERWISE SPECIFIED

1. MANUFACTURE IN ACCORDANCE WITH IPC-6012, TYPE 3, CLASS 2.
2. END PRODUCT FEATURES SHALL NOT VARY MORE THAN 20% FROM ARTWORK ORIGINALS.
3. LAMINATE AND PREPREG SHALL BE AS PER IPC-4101/26,83,98 WITH A DECOMPOSITION TEMPERATURE $\geq 345^{\circ}\text{C}$, COLOR, NATURAL.
4. COPPER WEIGHT SHALL BE 1.0 OZ./SQ. FT. BEFORE PLATING.
5. ALL PLATED THROUGH HOLES SHALL HAVE A MINIMUM OF 0.001" COPPER.
6. DRILL HOLE TOLERANCE AFTER PLATING SHALL BE $\pm 0.003"$.
7. MINIMUM ANNULAR RING SHALL BE 0.001".
8. MINIMUM ANNULAR RING AT EMERGENT CONDUCTORS SHALL BE 0.003".
9. FINAL PCB THICKNESS SHALL BE 0.062" $\pm 10\%$.
10. WARP/TWIST SHALL NOT EXCEED 1.0%
11. FINISH SHALL BE LPI, BLUE S.M.O.B.C., BALANCE ENIG.
12. SILKSCREEN WITH NONCONDUCTIVE WHITE EPOXY INK.
13. VENDOR TO PROVIDE PCB MICRO-SECTION OF COUPON AREA & TDR TEST REPORT.
14. REFERENCE ADDITIONAL FAB NOTES IN FILE README.TXT

DO NOT ADJUST SPECIFIED GEOMETRIES WITHOUT NOTIFICATION.							
GERBER FILENAME	LAYER	SINGLE ENDED		DIFFERENTIAL		BASE	
		IMPEDANCE (OHMS)	TRACE WIDTH (MIL)	IMPEDANCE (OHMS)	TRACE WIDTH (MIL)	TRACE CAP (MM)	THICKNESS (INCH)

52200-QFN32_PSS.PHO PRIMARY SILKSCREEN


52200-QFN32_PSM.PHO PRIMARY SOLDER MASK

52200-QFN32_PRL.PHO	L01	PRIMARY (Signal)	50	0.15	100	0.15	0.35	0.5 oz	3.74MIL
52200-QFN32_L02.PHO	L02	PLANE (GND)	370HR					1.0 oz	14.00MIL
52200-QFN32_L03.PHO	L03	PLANE (GND)	370HR					1.0 oz	17.96MIL
52200-QFN32_L04.PHO	L04	PLANE (+5V/ROUTE)	370HR					1.0 oz	14.00MIL
52200-QFN32_L05.PHO	L05	PLANE (GND)	370HR					1.0 oz	3.74MIL
52200-QFN32_SEC.PHO	L06	SECONDARY (Signal)	50	0.15	100	0.15	0.35	0.5 oz	

52200-QFN32_SSM.PHO SECONDARY SOLDER MASK

52200-QFN32_SSS.PHO SECONDARY SILKSCREEN

SIZE	QTY	SYM	PLT	TOOL	TOL
0.012	968	+	P	1	+0/-0.012
0.036	2	×	N	2	+/-0.003
0.040	78	□	P	3	+/-0.003
0.091	2	◇	P	4	+/-0.003
0.125	5	⊗	N	5	+/-0.003
0.266	2	⊗	P	6	+/-0.003

UNLESS OTHERWISE SPECIFIED			THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND SHALL NOT BE DUPLICATED OR USED FOR ANY PURPOSE OTHER THAN THAT FOR WHICH PROVIDED OR DISCLOSED IN WHOLE OR IN PART, WITHOUT THE WRITTEN CONSENT OF SILICON LABORATORIES, INC..		COMPANY:		
DIMENSIONS ARE IN INCHES AND APPLY AFTER FINISH					 400 W Cesar Chavez AUSTIN, TX 78701 (512)416-8500 www.silabs.com		
INTERPRET DRAWING PER MIL-D-1000							
TOLERANCES							
HOLE TOLERANCES PER 78027			NAME:		Si52204-EVB	REV : 2.0	
DECIMALS .XX +/- .XXX +/-			ANGLES +/-			SURFACES MICROINCHES	
PART TO BE FREE OF BURRS			DESIGN		SIZE		
BREAK EDGES			BEND RADIUS		PART NUMBER:		
BEND RELIEF			LAYOUT		A		
DO NOT SCALE DRAWING			SCALE 1:1		FABRICATION DRAWING		
SHEET 1 OF 1							