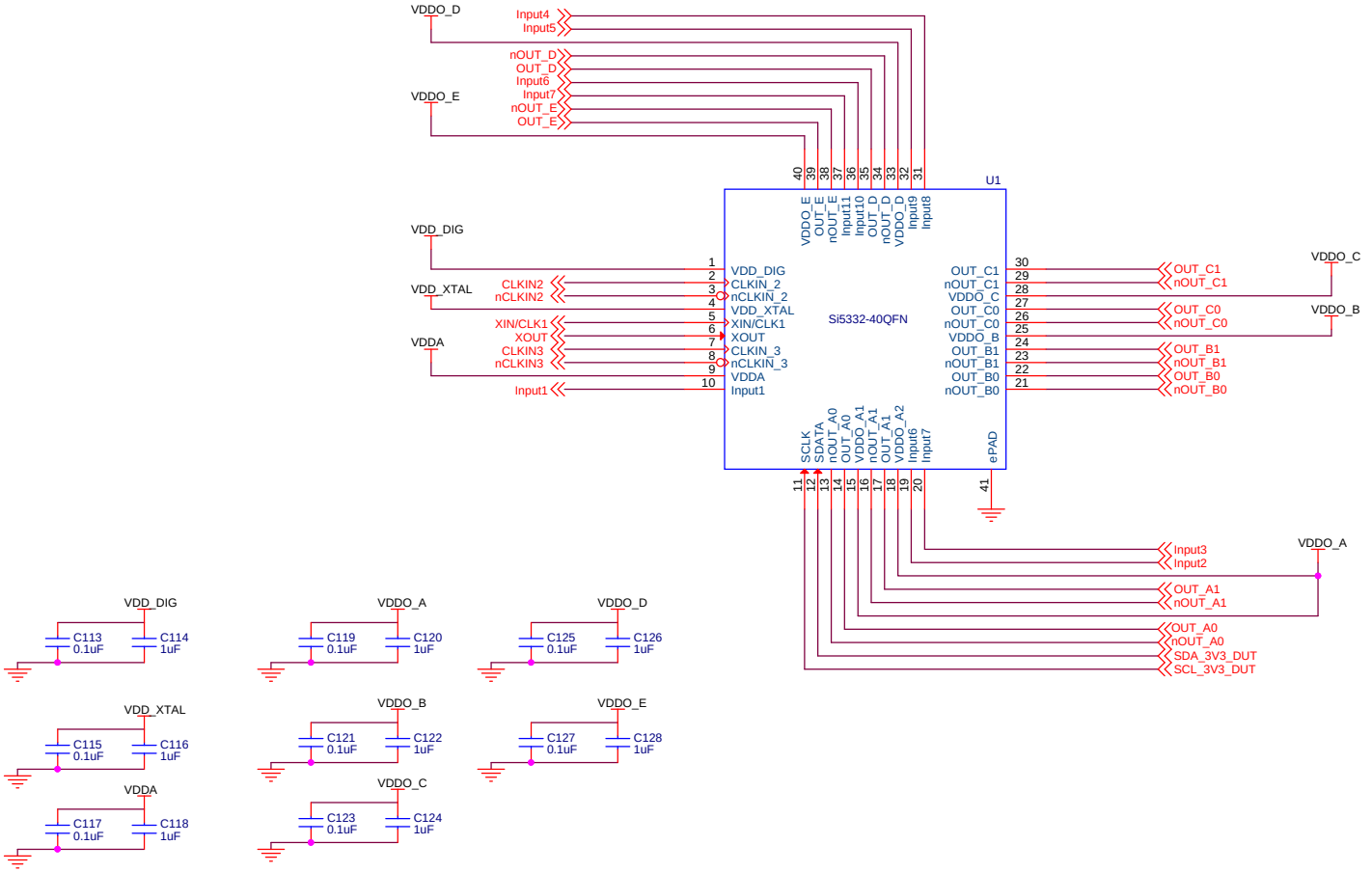
# DUT CONNECTIONS




| | | |
|---|---|---|
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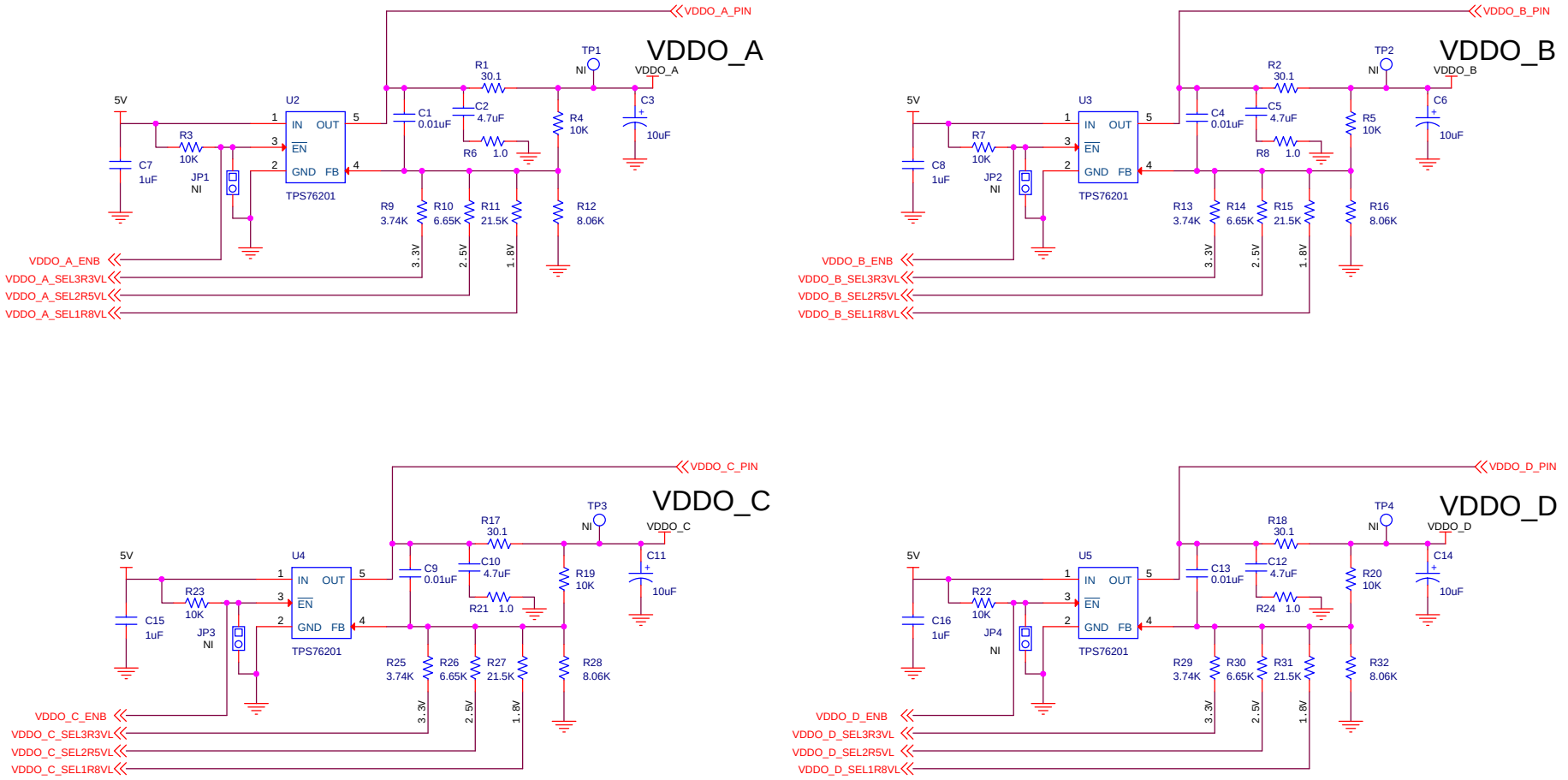
| Title | DUT Connections | |
| Size B | Document Number<br>SI5332-40-PIN-QFN-DUT-CUST-EVB-REV1 . | Rev 1.0 |
| Date: Tuesday, April 18, 2017 | Sheet 1 of 13 | |

# 100 mA Adjustable Voltage Regulator





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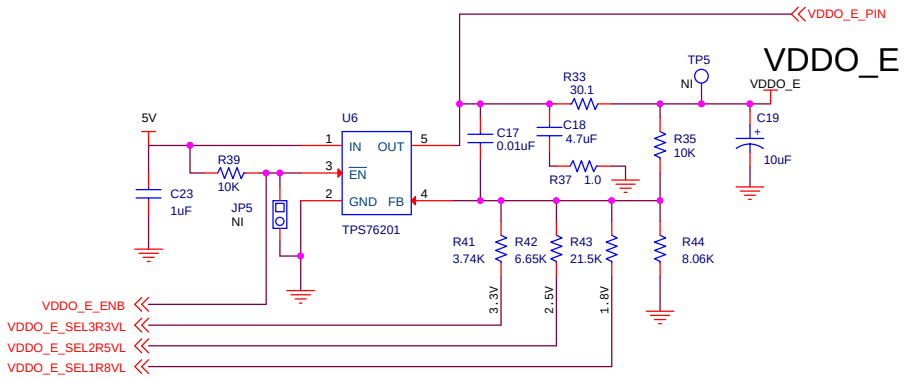
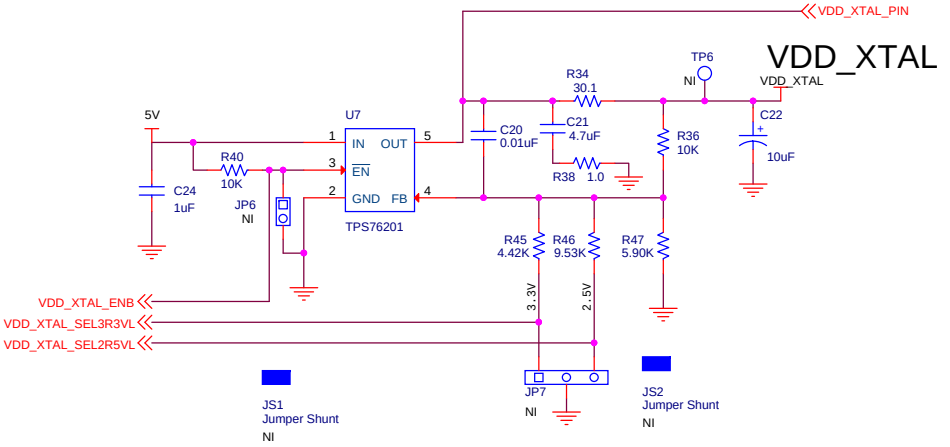
Title: Output Voltage Regulators

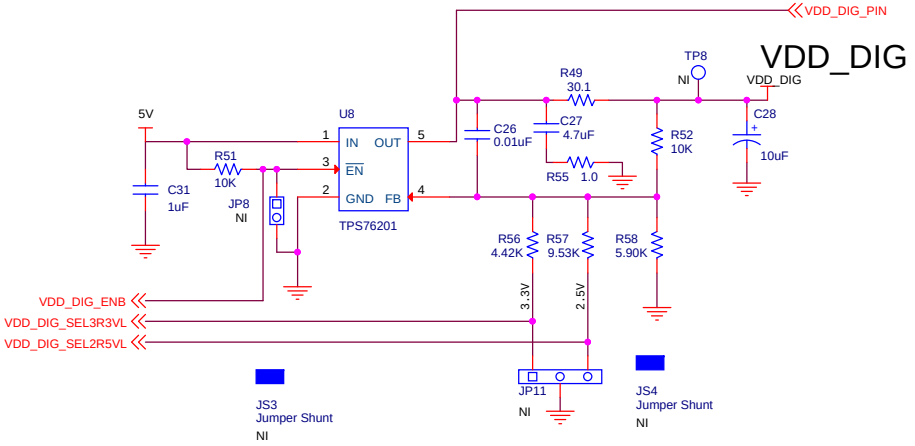
| Size | Document Number | Rev |
|---|---|---|
| B | SI5332-40-PIN-QFN-DUT-CUST-EVB-REV1 . | 1.0 |

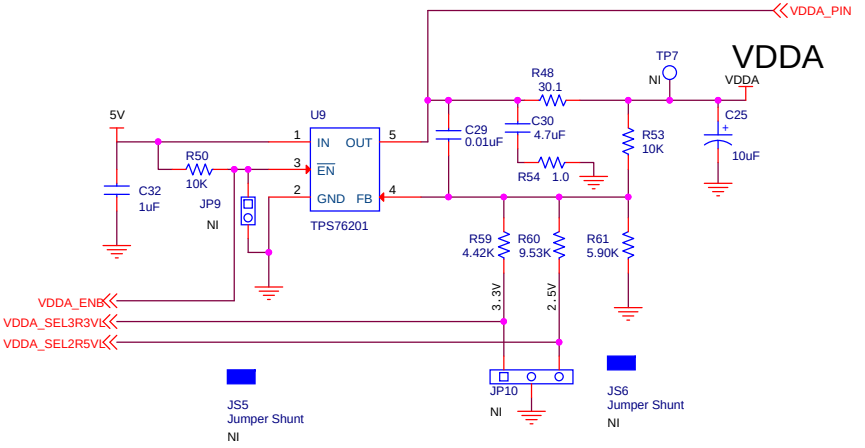
Date: Wednesday, April 12, 2017 Sheet 2 of 13

# 100 mA Adjustable Voltage Regulator





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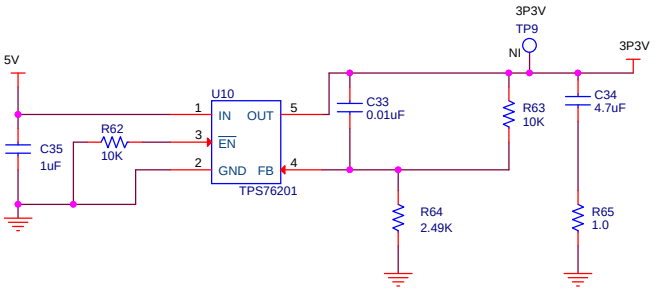
Title: Other Voltage Regulators

| Size | Document Number | Rev |
|---|---|---|
| B | SI5332-40-PIN-QFN-DUT-CUST-EVB-REV1 . | 1.0 |

Date: Wednesday, April 12, 2017 Sheet 3 of 13

# Fixed 3.3V 100 mA Voltage Regulator
# (Enabled, no current measurement supported.)




3P3V (In Schematic)
3P3V (Board Silkscreen)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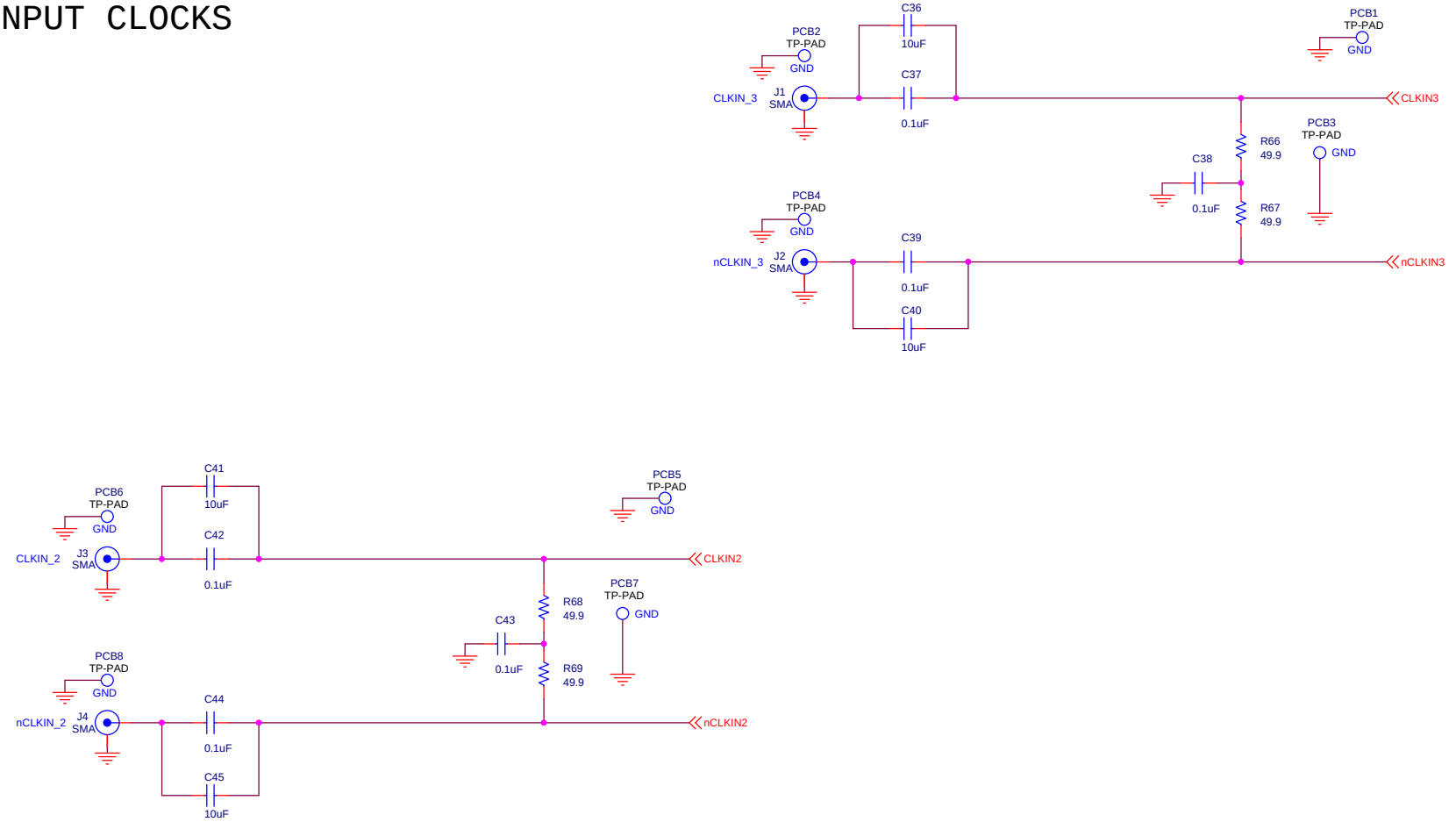
| | | |
|---|---|---|
| Title | 3P3V Fixed Voltage Regulator | |
| Size B | Document Number SI5332-40-PIN-QFN-DUT-CUST-EVB-REV1 . | Rev 1.0 |
| Date: Wednesday, April 12, 2017 | Sheet 4 of 13 | |

# INPUT CLOCKS





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Title
Input Clock Configuration

| Size | Document Number | Rev |
|---|---|---|
| B | SI5332-40-PIN-QFN-DUT-CUST-EVB-REV1 . | 1.0 |

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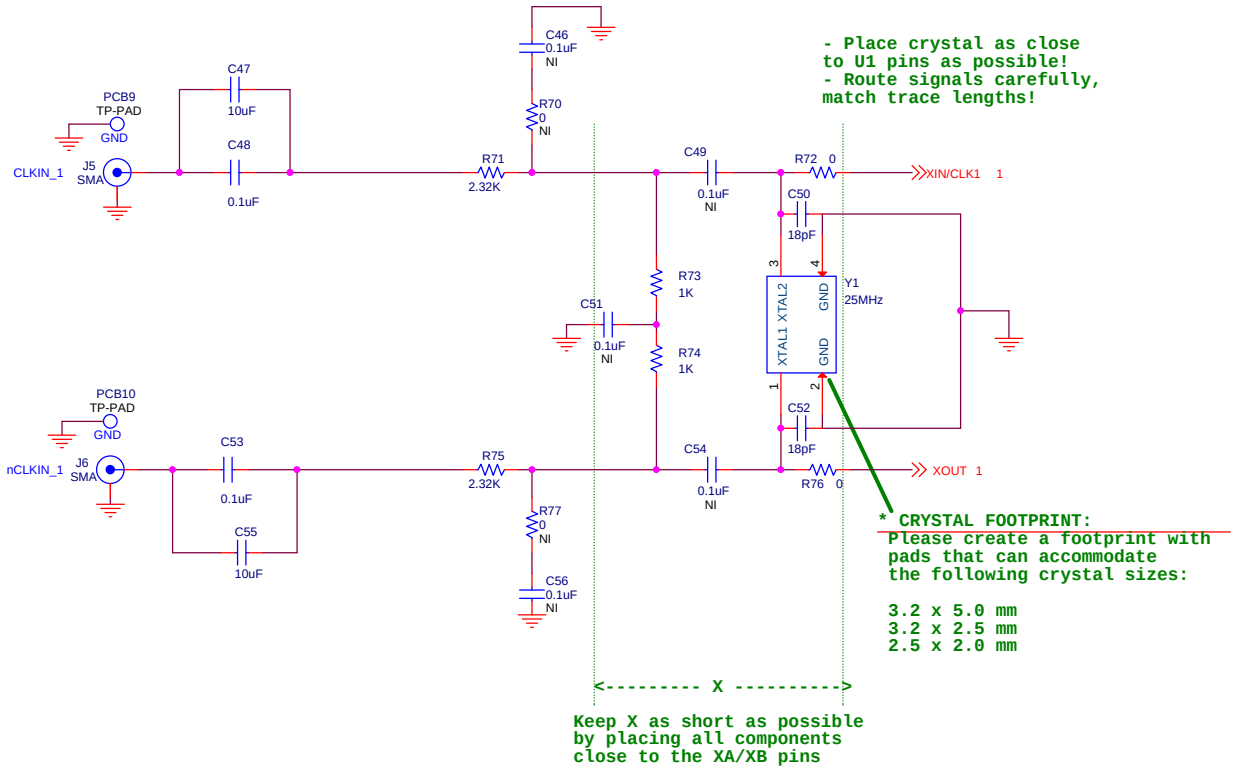
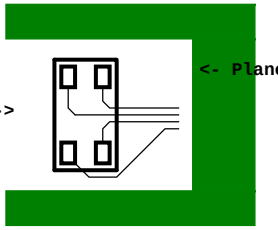
# Crystal Input Connections




Cut planes underneath crystal
to reduce capacitive coupling!




Traces are just an illustration!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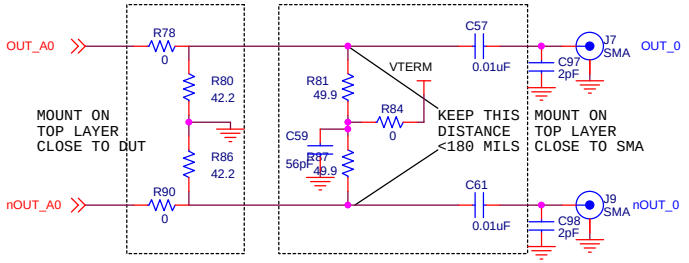
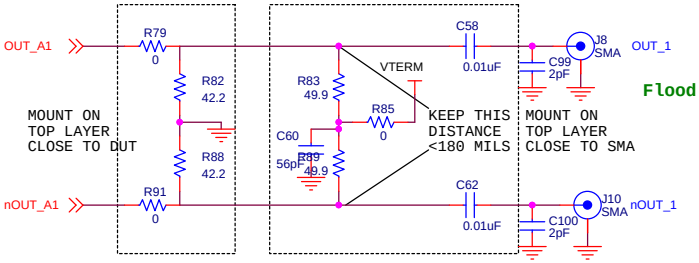
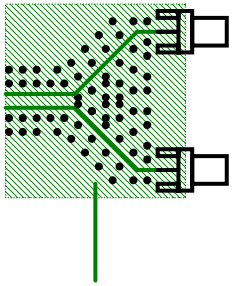
| Title | | |
|---|---|---|
| Crystal Input Connections | | |
| Size B | Document Number SI5332-40-PIN-QFN-DUT-CUST-EVB-REV1 . | Rev 1.0 |
| Date: Tuesday, April 18, 2017 | Sheet 6 of 13 | |

# OUTPUT CONNECTIONS, PART 1

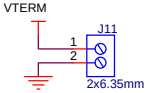


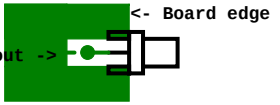




Flood top and bottom layers with copper as shown

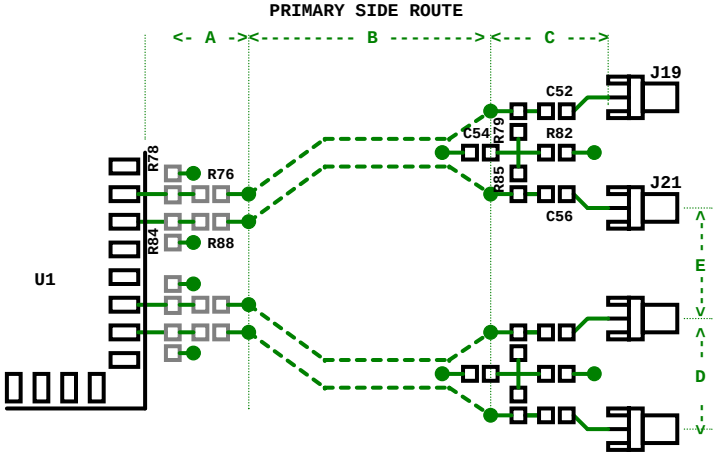


SMA FOOTPRINT NOTE:
Make sure pad for center pin on SMA matches exactly
the actual width of the center pin in order to improve performance




A sufficient number of via holes connected
to ground should be used around all input/output
traces!




OUTPUT SIGNALS LAYOUT NOTES - APPLIES TO THIS PAGE AND NEXT PAGE AS WELL!
(Refer to image on left):

- ROUTING: route each differential pair losely coupled. Trombone only when absolutely necessary and preserve symmetry on diff. pair. Keep bending at a minimum

- IMPEDANCE: all traces to have 50 ohms of controlled impedance
  - In order to reduce capacitance please cut-out ground planes underneath the microstrip launches on the SMA connectors as needed

- BANDWIDTH: all traces need a bandwidth of 9 GHz! (20-80% RT ~ 25ps)

- GEOMETRY: maintain the trace symmetry across all output differential pairs

- TOPOLOGY: use microstip for SMA-to-trace and DUT-to-resistor launches, stripline for rest of traces

- COMPONENT PLACEMENT:
  - Separate each pair of SMA connectors by 750 mils between them (center to center, and also pair to pair) on flat edge, and by 785 mils on arc edge

- DIMENSIONS:
  - Use via-in-pad to drop to bottom layer to place termination resistors (49.9) and decoupling cap;
  - Make trace <A> as short as possible, then use via after resistor to launch into inner layer
  - Match trace length <B> on all output signals. Use shortest possible length
  - Make <C> and <F> distances as short as possible
  - Keep <D> at 0.75" (750 mils) on flat edge, 0.785" on arc edge

- LAYERS:
  - Top Layer: microstrips for SMA to components and DUT-to-snub resistor (953);
  - Layer 7: striplines for <B> traces
  - Bottom Layer: termination Res's (49.9) and decoupling cap;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| Title | Output Connections | |
|---|---|---|
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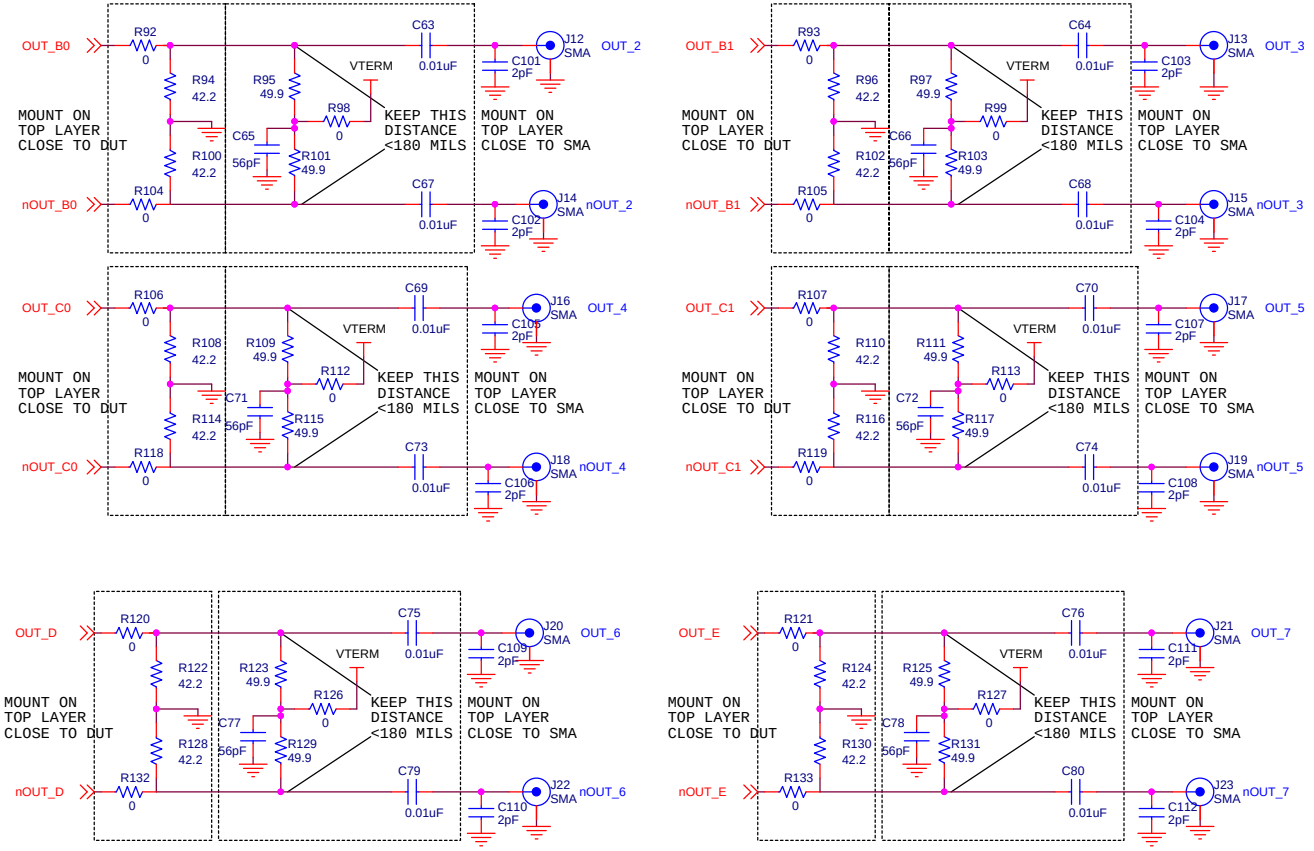
| Date: Wednesday, April 12, 2017 | Sheet 7 of 13 | |

# OUTPUT CONNECTIONS, PART 2

| FORMAT | R572/573 | R515/516 | R524/525 | R526/527 | VTERM_x |
|---|---|---|---|---|---|
| LVDS(DC) | NI | 0 | 49.9 | 0 | NI |
| LVDS(AC) | NI | 0.01uF | 49.9 | 0 | NI |
| HCSL(EXT) | 49.9 | 0 | NI | 0 | NI |
| LVPECL(DC) | NI | 0 | 49.9 | 0 | VDDOx-2 |
| CMOS(33) | NI | 27 | 4pF | 0 | GND |
| CMOS(25) | NI | 20 | 4pF | 0 | GND |

SEE PREVIOUS PAGE FOR LAYOUT INSTRUCTIONS!





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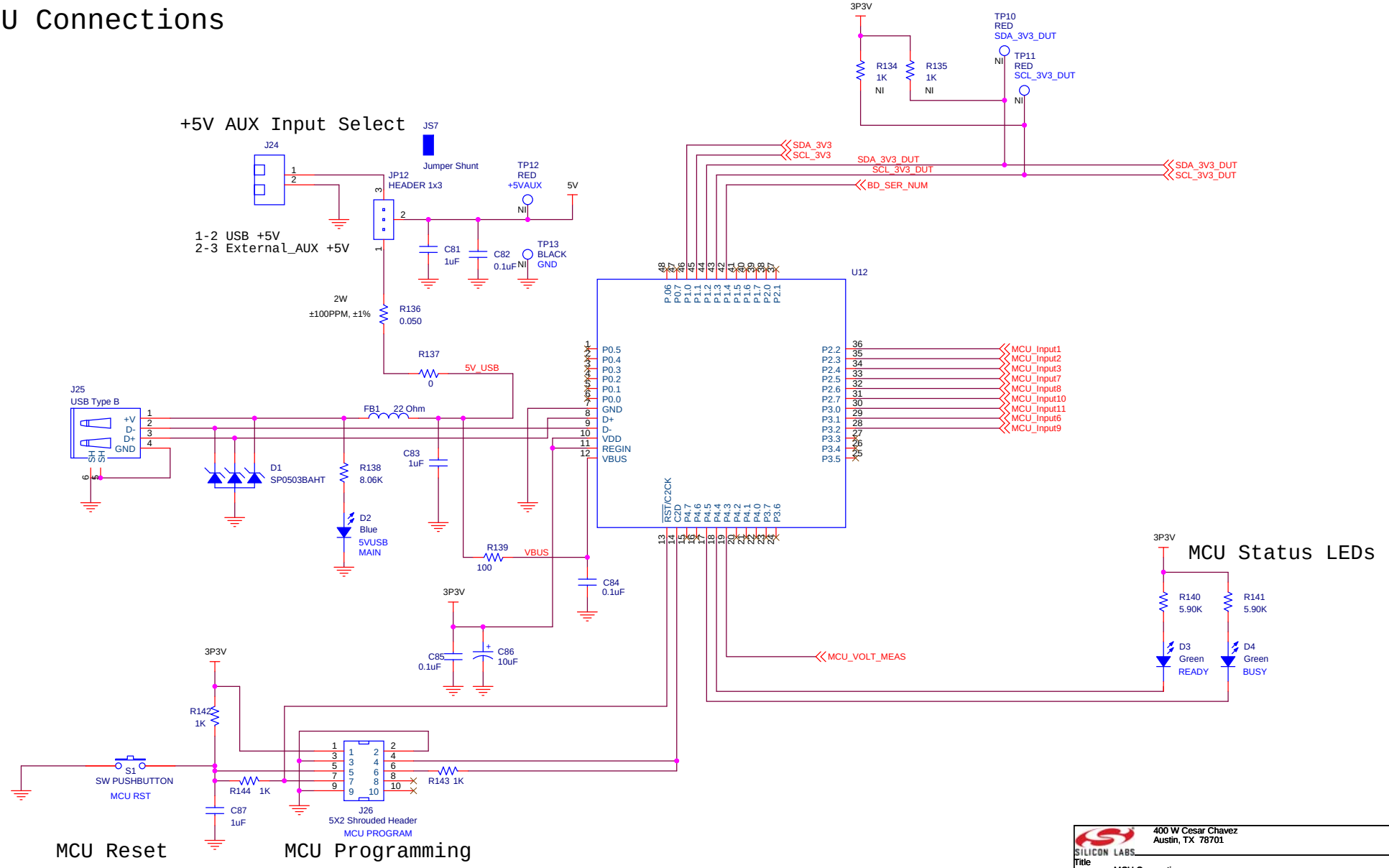
Title: Output Connections

| Size | Document Number | Rev |
|---|---|---|
| B | SI5332-40-PIN-QFN-DUT-CUST-EVB-REV1 . | 1.0 |

Date: Wednesday, April 12, 2017 Sheet 8 of 13

# MCU Connections




| | | |
|---|---|---|
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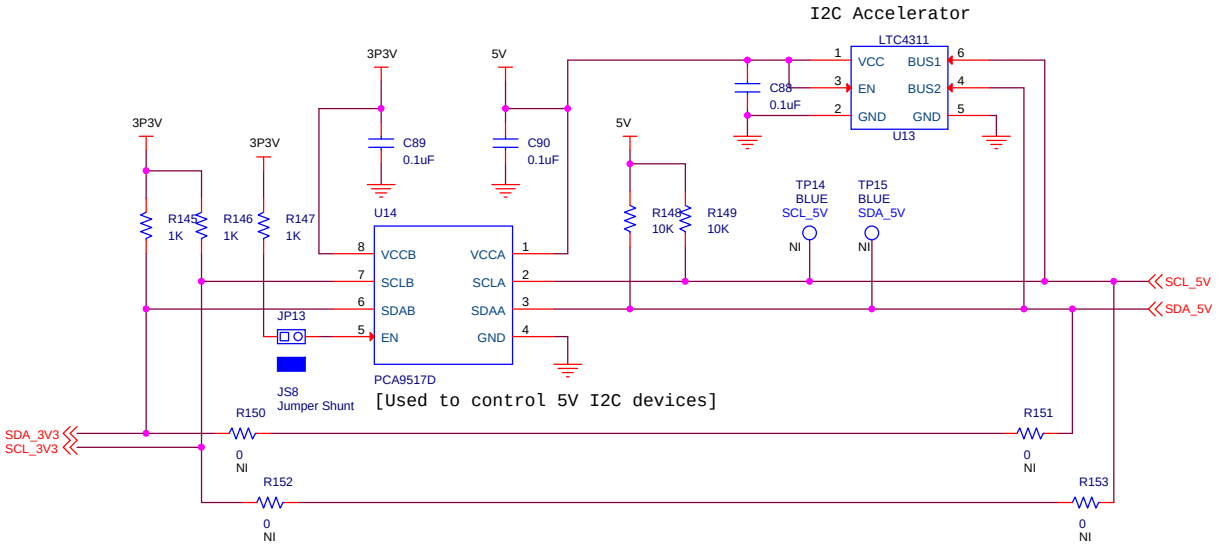
| Title | MCU Connections | |
| Size B | Document Number<br>SI5332-48-PIN-QFN-DUT-CUST-EVB-REV1 . | Rev 1.0 |
| Date: Wednesday, April 12, 2017 | Sheet 9 of 13 | |

# I2C LEVEL TRANSLATOR




| | | |
|---|---|---|
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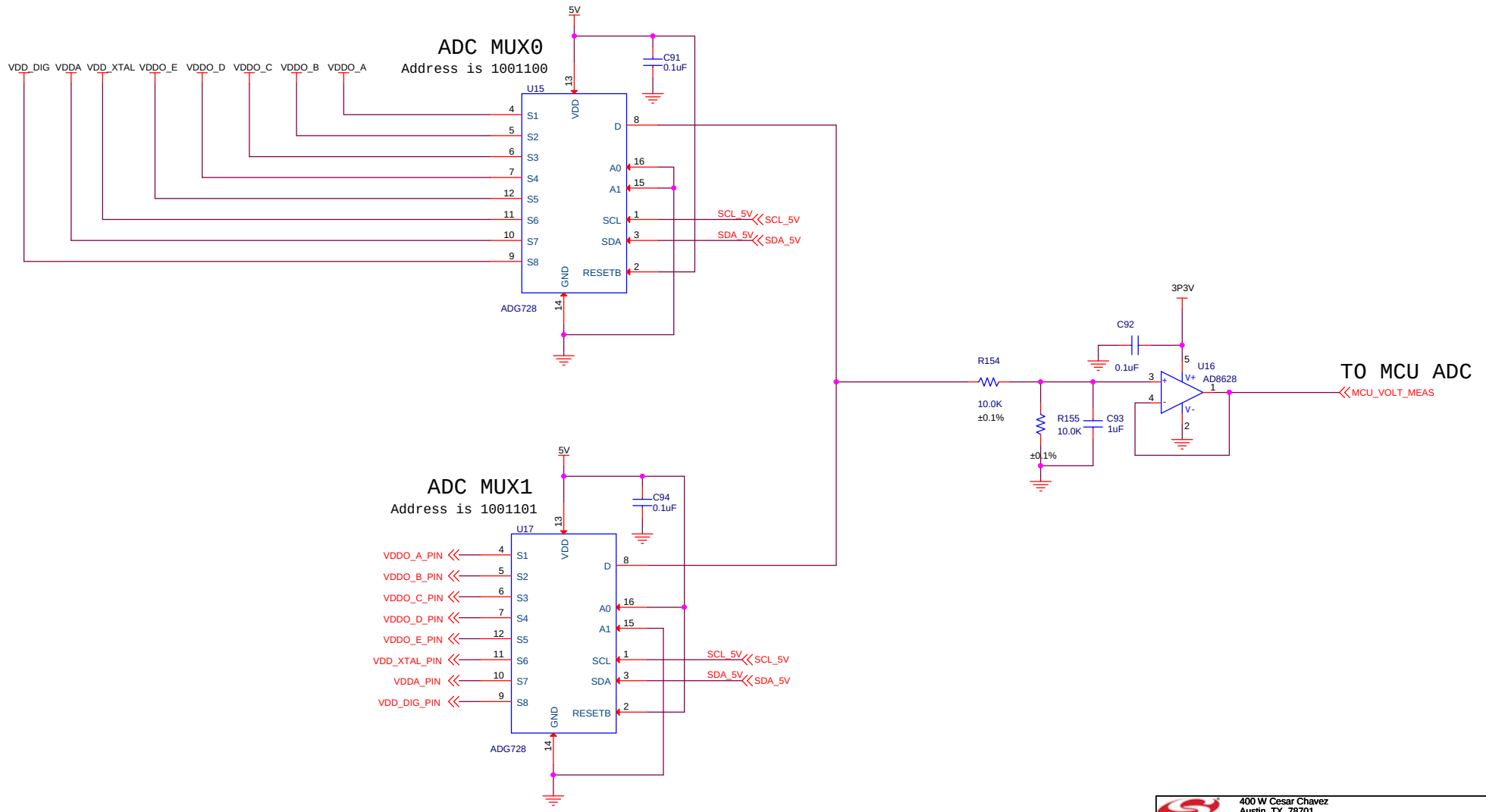
| Title | I2C Level Shifter | |
| Size B | Document Number<br>SI5332-40-PIN-QFN-DUT-CUST-EVB-REV1 . | Rev 1.0 |
| Date: Wednesday, April 12, 2017 | Sheet 10 of 13 | |

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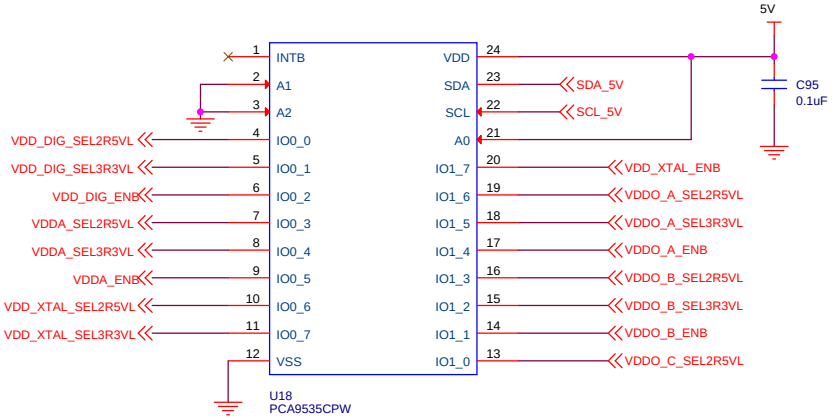
Title
Voltage Measurement Mux

| Size | Document Number | Rev |
|---|---|---|
| B | SI5332-40-PIN-QFN-DUT-CUST-EVB-REV1 . | 1.0 |

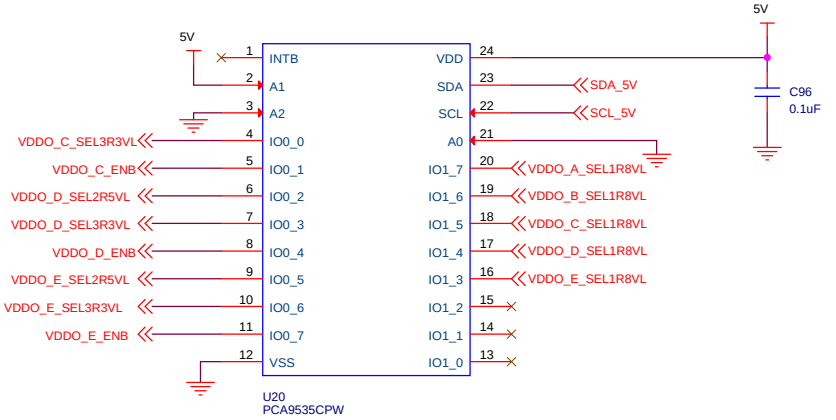
Date: Wednesday, April 12, 2017 Sheet 11 of 13

# VDD Enables and SN



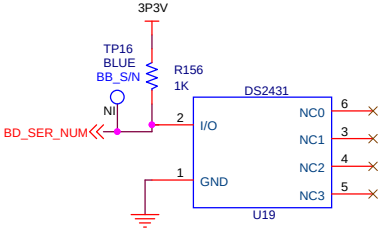

## I2C VDD ENABLES/SELECTS FOR REGULATORS

I2C address: 0100001




## I2C VDD ENABLES/SELECTS FOR REGULATORS

I2C address: 0100010




## Board Serial Number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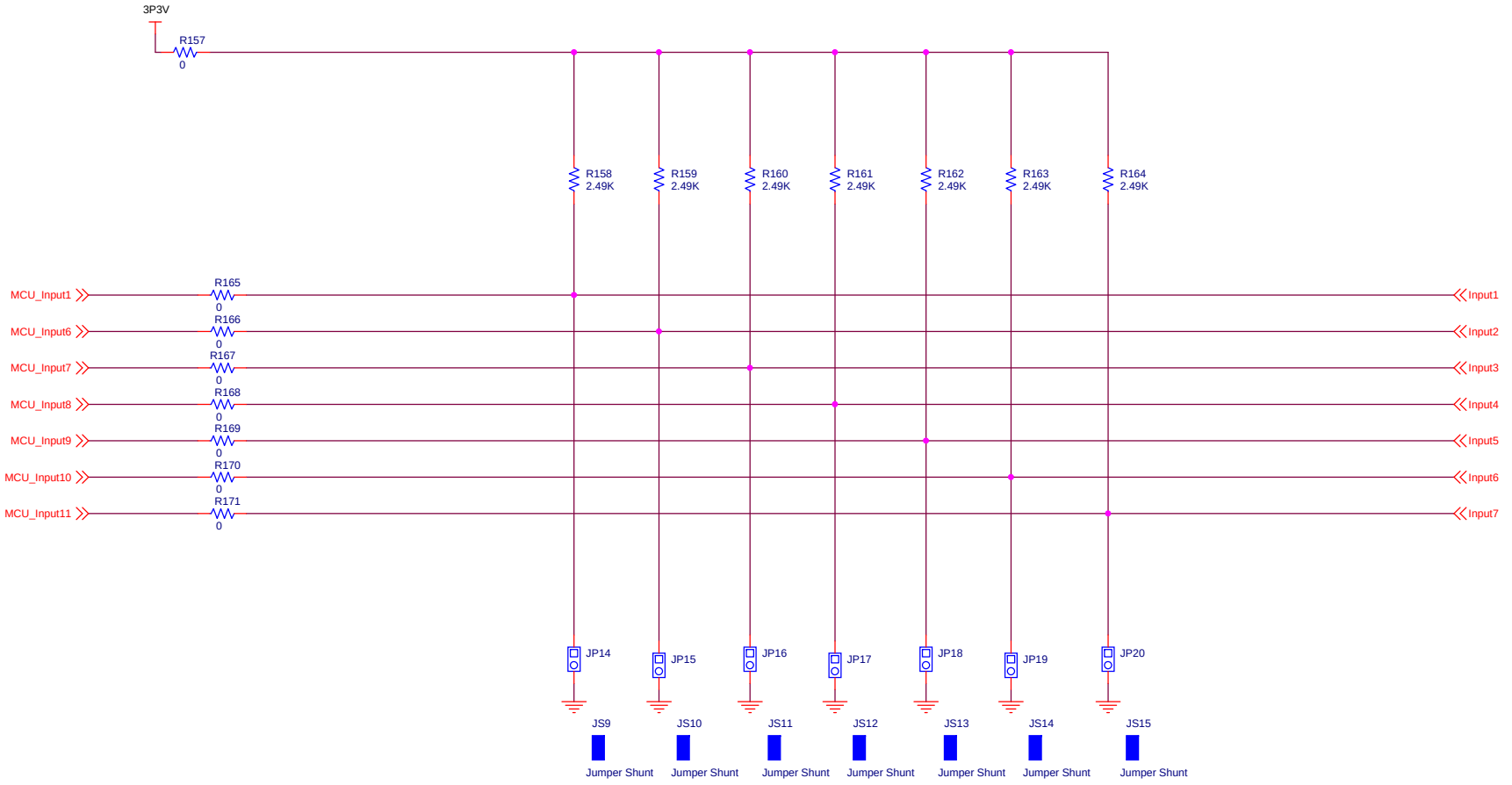
| Title | | |
|---|---|---|
| VDD Enables and SN | | |
| Size B | Document Number SI5332-40-PIN-QFN-DUT-CUST-EVB-REV1 . | Rev 1.0 |
| Date: Wednesday, April 12, 2017 | Sheet 12 of 13 | |

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Title
DC inputs

| Size | Document Number | Rev |
|---|---|---|
| B | SI5332-40-PIN-QFN-DUT-CUST-EVB-REV1 . | 1.0 |

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