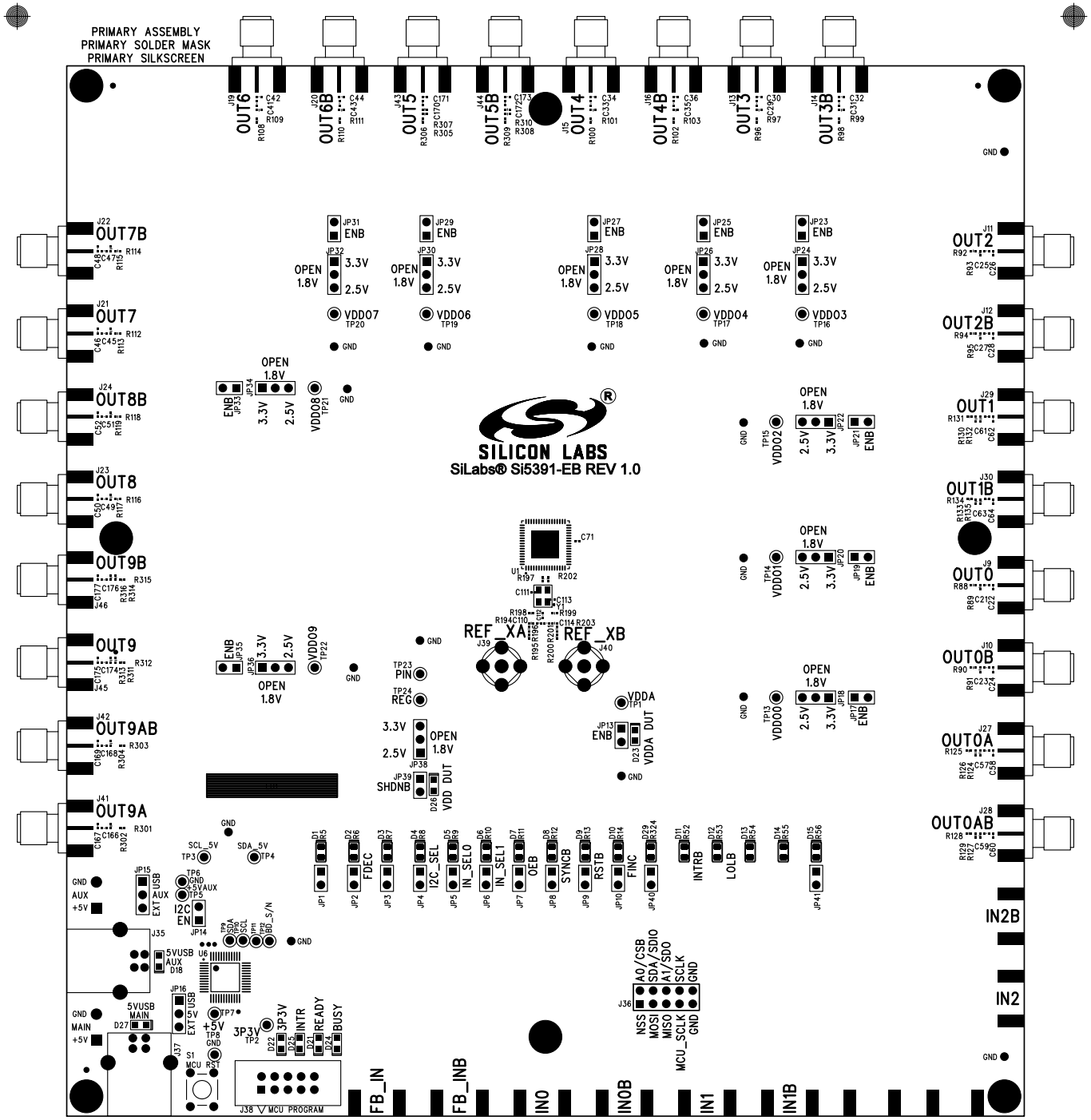
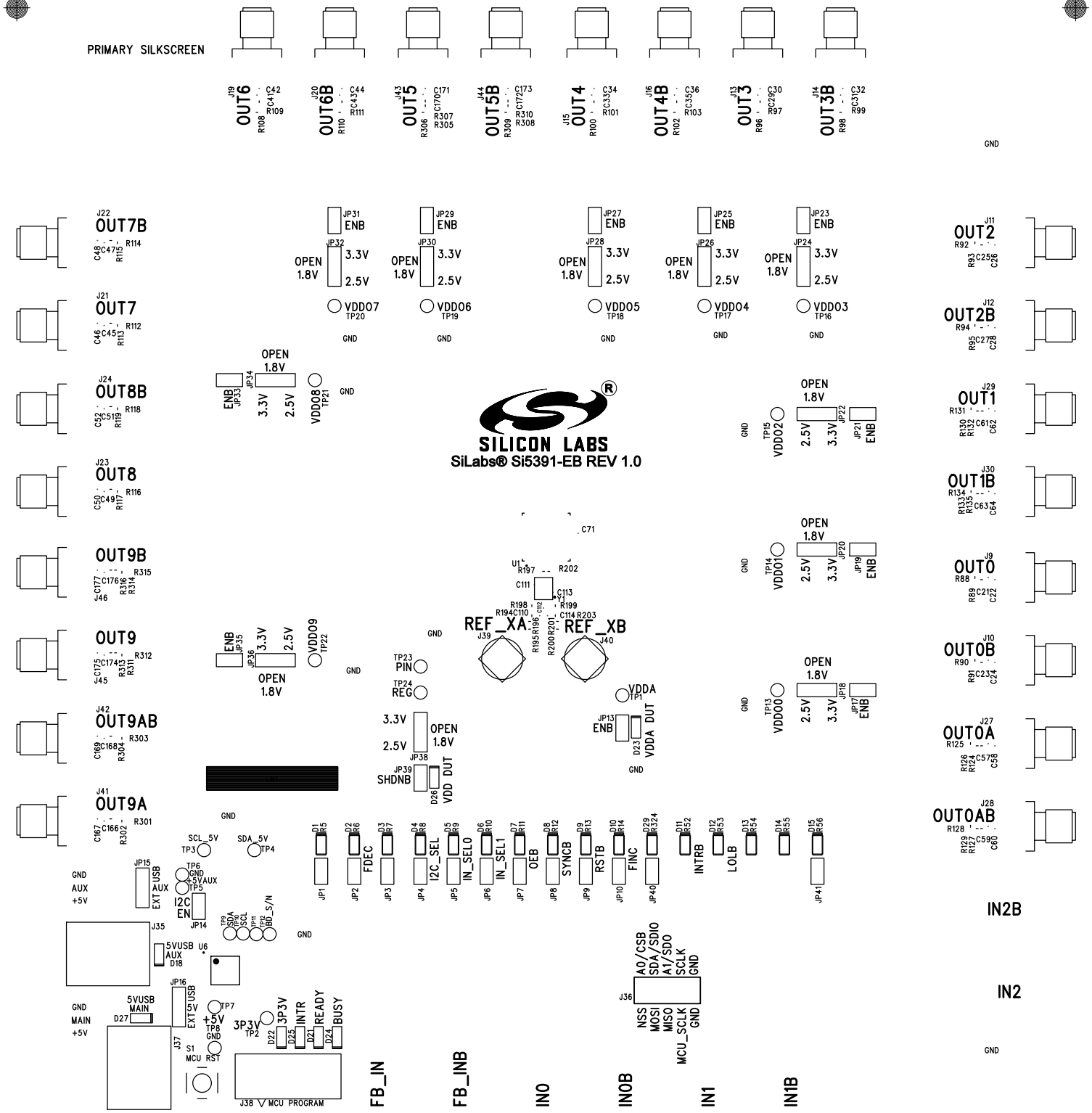
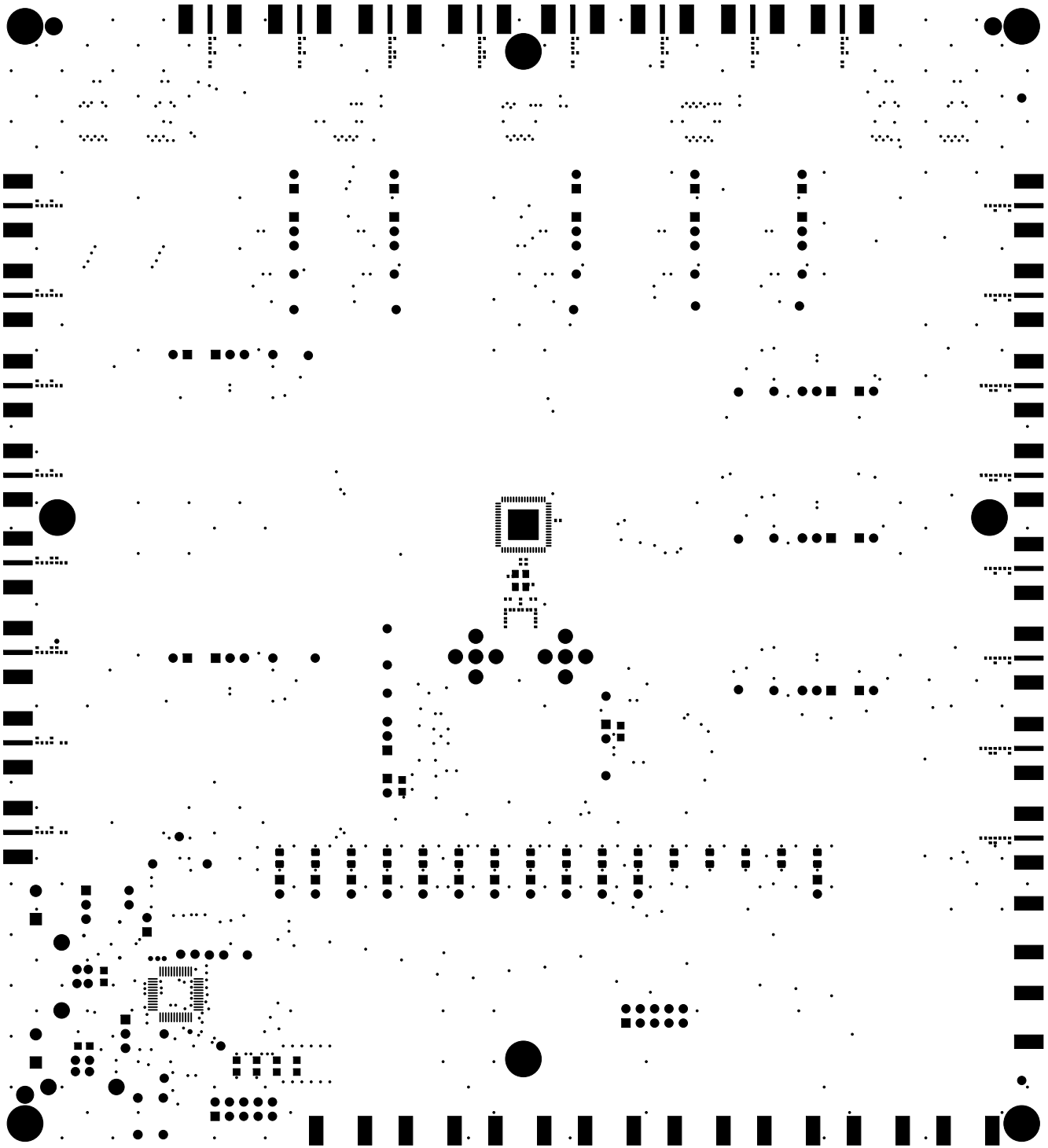

PRIMARY ASSEMBLY
PRIMARY SOLDER MASK
PRIMARY SILKSCREEN
SILICON LABS
SiLabs® Si5391-EB REV 1.0
OUT6
OUT6B
OUT5
OUT5B
OUT4
OUT4B
OUT3
OUT3B
OUT7B
OUT7
OUT8B
OUT8
OUT9B
OUT9
OUT9AB
OUT9A
OUT2
OUT2B
OUT1
OUT1B
OUT0
OUT0B
OUT0A
OUT0AB
IN2B
IN2
FB_IN
FB_INB
IN0
IN0B
IN1
IN1B
REF_XA
REF_XB
VDDO7
VDDO6
VDDO5
VDDO4
VDDO3
VDDO8
VDDO9
VDDO2
VDDO1
VDDO0
VDDA
VDD_DUT
VDDA_DUT
PIN
REG
SHDNB
ENB
OPEN
1.8V
2.5V
3.3V
SCL_5V
SDA_5V
FDEC
I2C_SEL
IN_SEL0
IN_SEL1
OEB
SYNCB
RSTB
FINC
INTRB
LOLB
A0/CSB
SDA/SDIO
A1/SDO
SCLK
GND
NSS
MOSI
MISO
MCU_SCLK
AUX
+5V
EXT USB
5VUSB
MAIN
I2C EN
3P3V
INTR
READY
BUSY
MCU RST
J38 MCU PROGRAM

SECONDARY ASSEMBLY

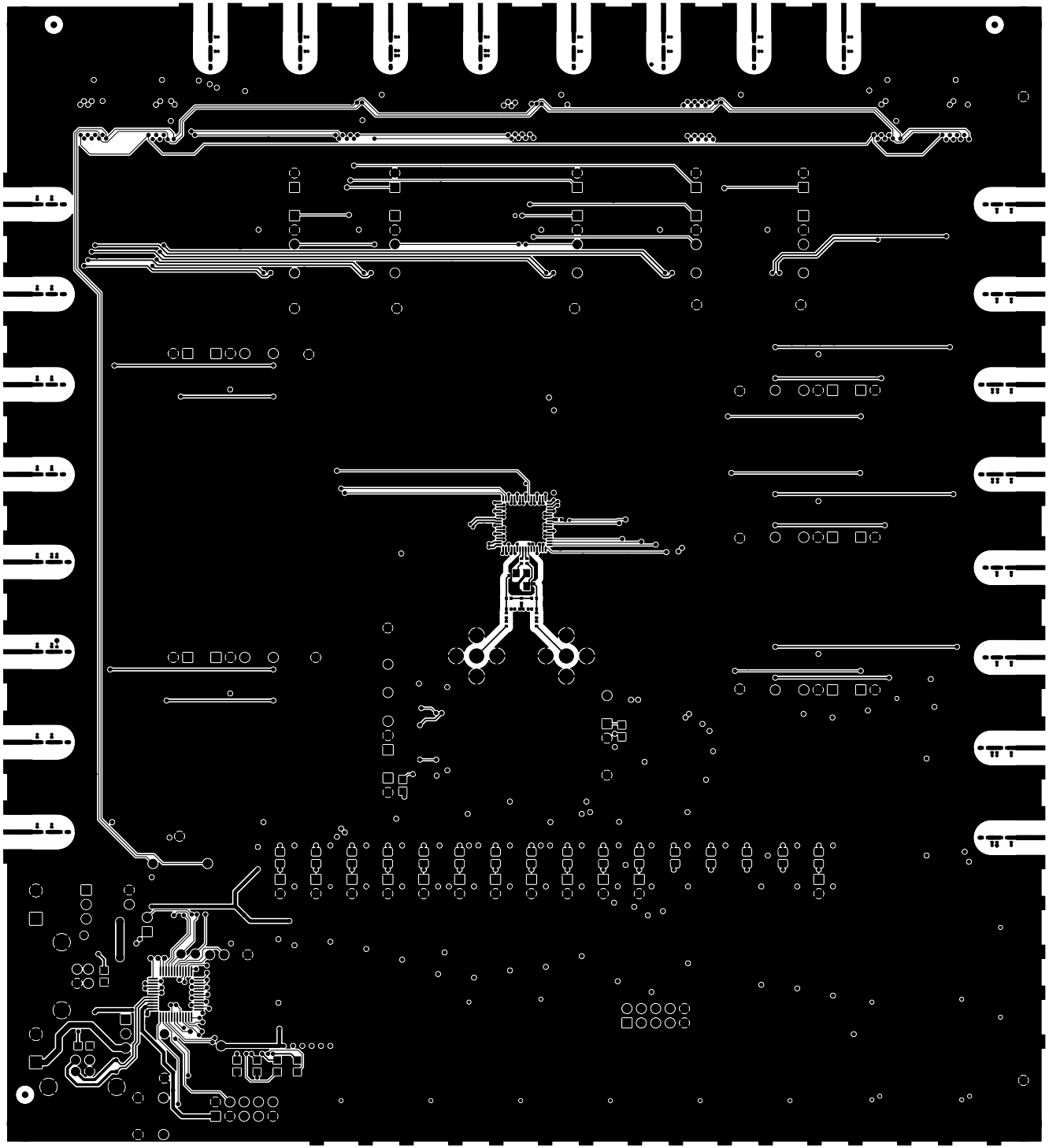
SECONDARY SILKSCREEN


PRIMARY SILKSCREEN
OUT6
OUT6B
OUT5
OUT5B
OUT4
OUT4B
OUT3
OUT3B
OUT7B
OUT7
OUT8B
OUT8
OUT9B
OUT9
OUT9AB
OUT9A
OUT2
OUT2B
OUT1
OUT1B
OUT0
OUT0B
OUT0A
OUT0AB
SILICON LABS
SiLabs® Si5391-EB REV 1.0
REF_XA
REF_XB
VDDO7
VDDO6
VDDO5
VDDO4
VDDO3
VDDO8
VDDO9
VDDO2
VDDO1
VDDO0
VDDA
VDD_DUT
PIN
REG
SHDNB
FDEC
I2C_SEL
IN_SEL0
IN_SEL1
OEB
SYNCB
RSTB
FINC
INTRB
LOLB
IN2B
IN2
FB_IN
FB_INB
IN0
IN0B
IN1
IN1B
A0/CSB
SDA/SDIO
A1/SDO
SCLK
GND
NSS
MOSI
MISO
MCU_SCLK
GND
GND
AUX
+5V
GND
MAIN
+5V
5VUSB
MAIN
5VUSB
AUX
I2C
EN
EXT USB
SCL_5V
SDA_5V
3P3V
INTR
READY
BUSY
MCU RST
J38 MCU PROGRAM

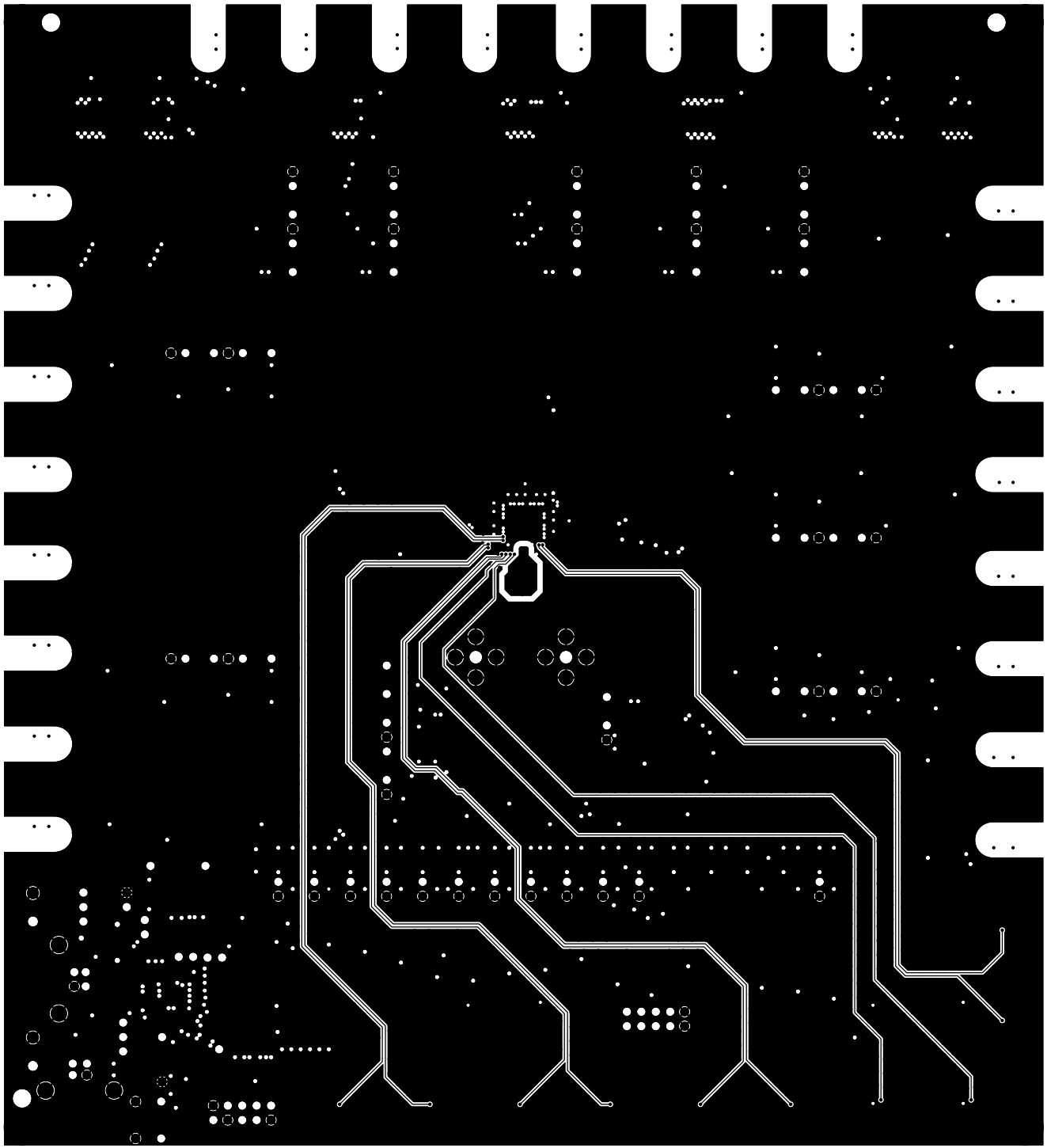
PRIMARY SOLDER MASK



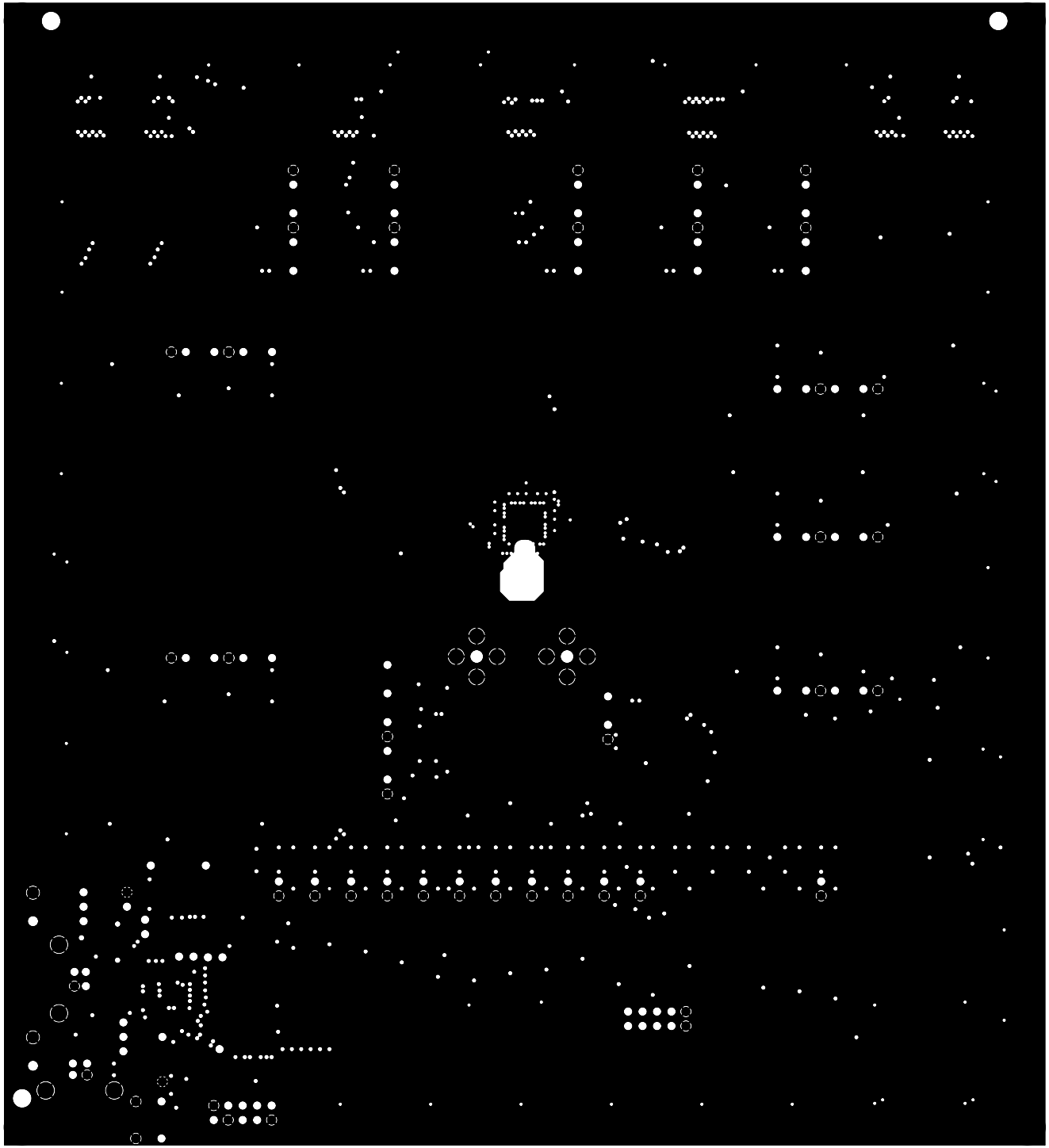
PRIMARY SIDE



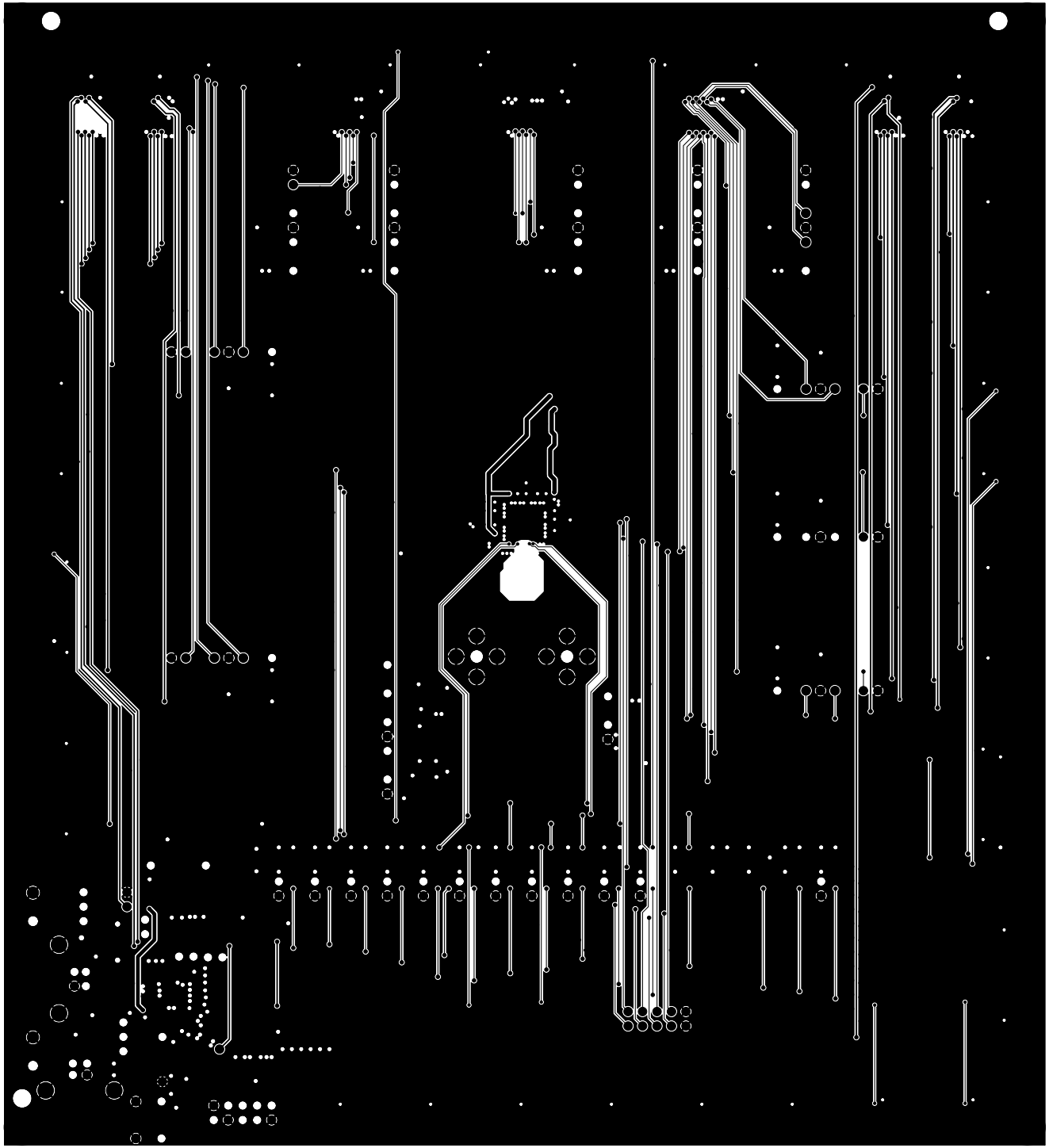
LAYER 02



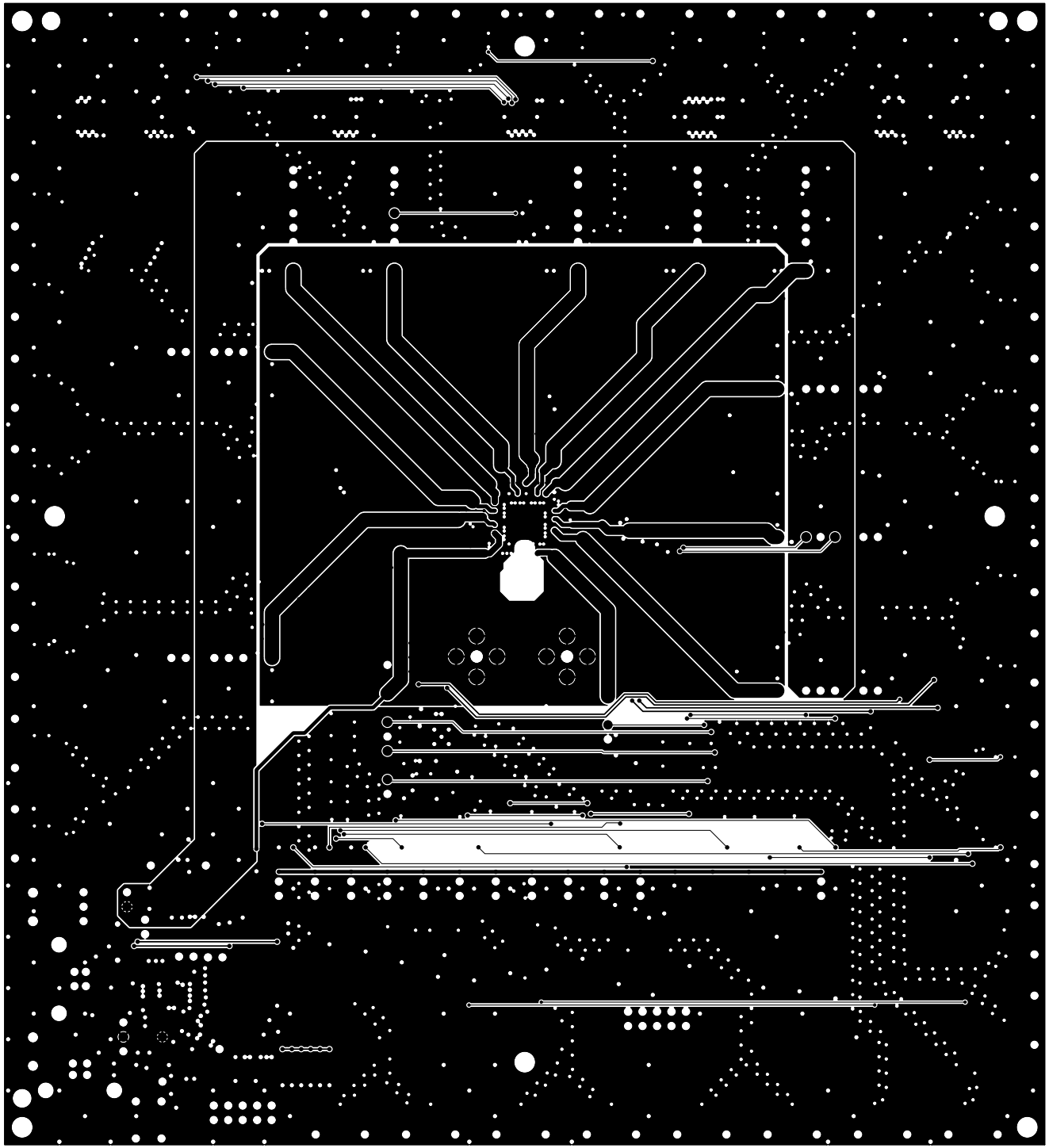
LAYER 03



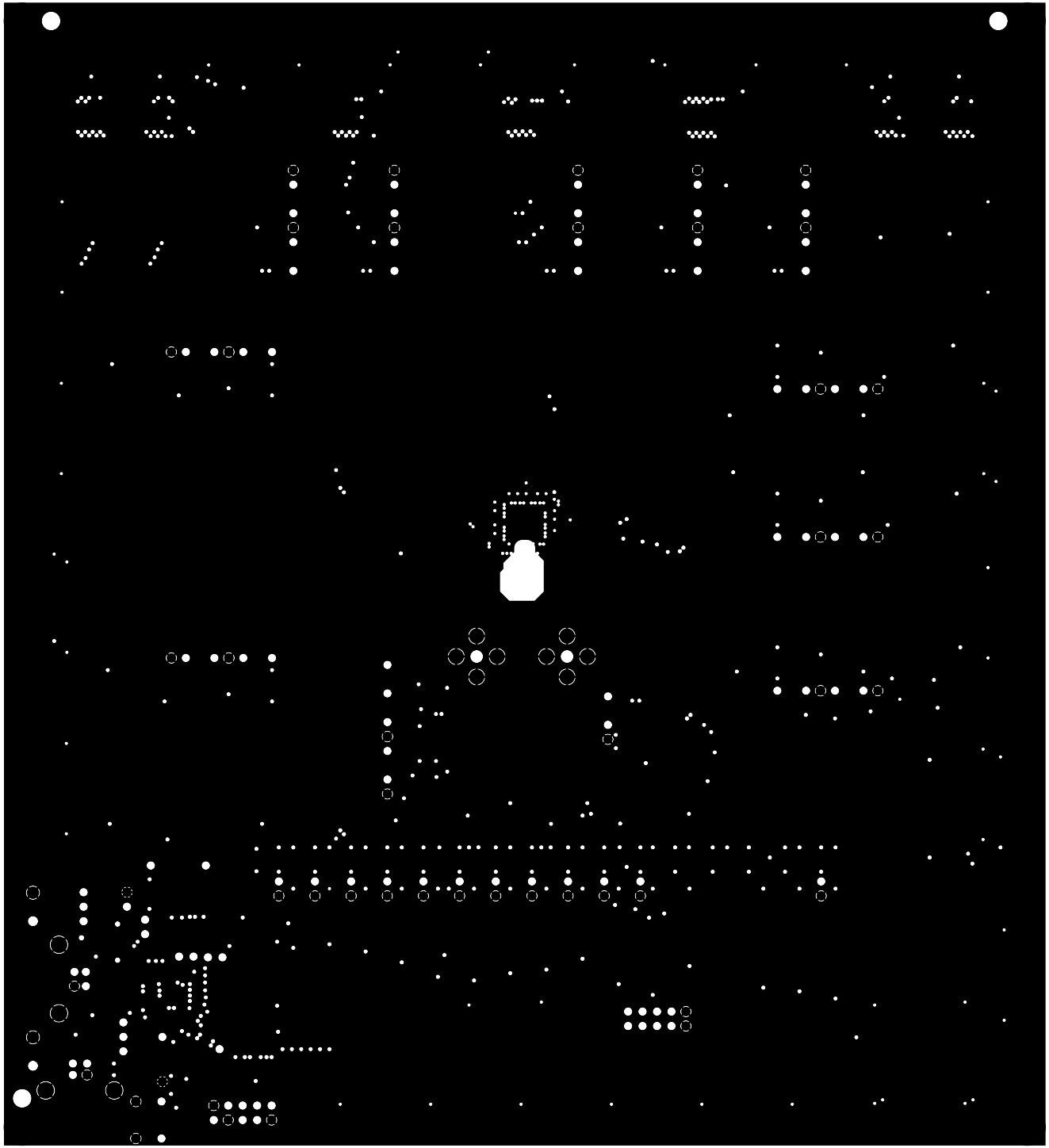
LAYER 04



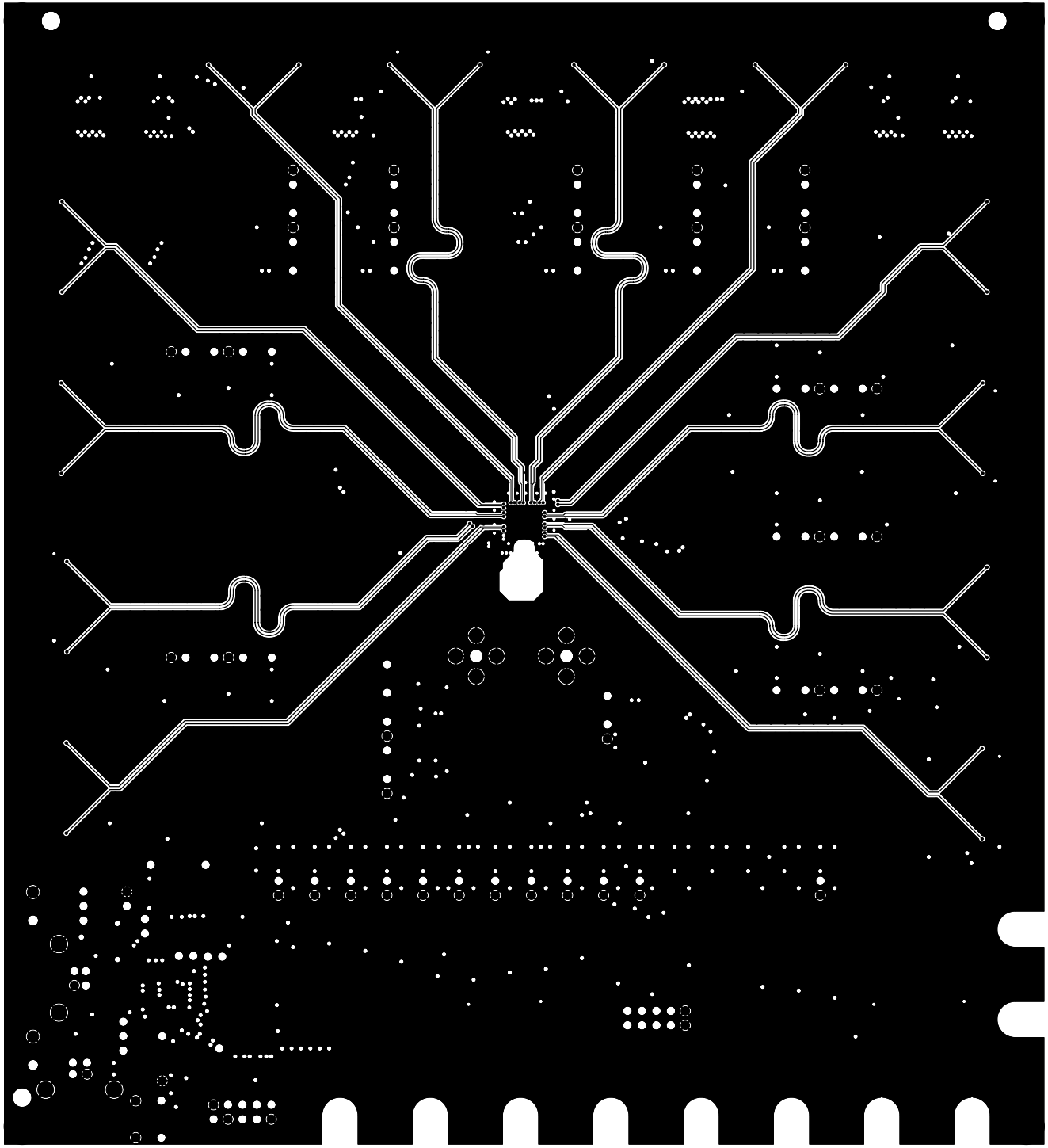
LAYER 05



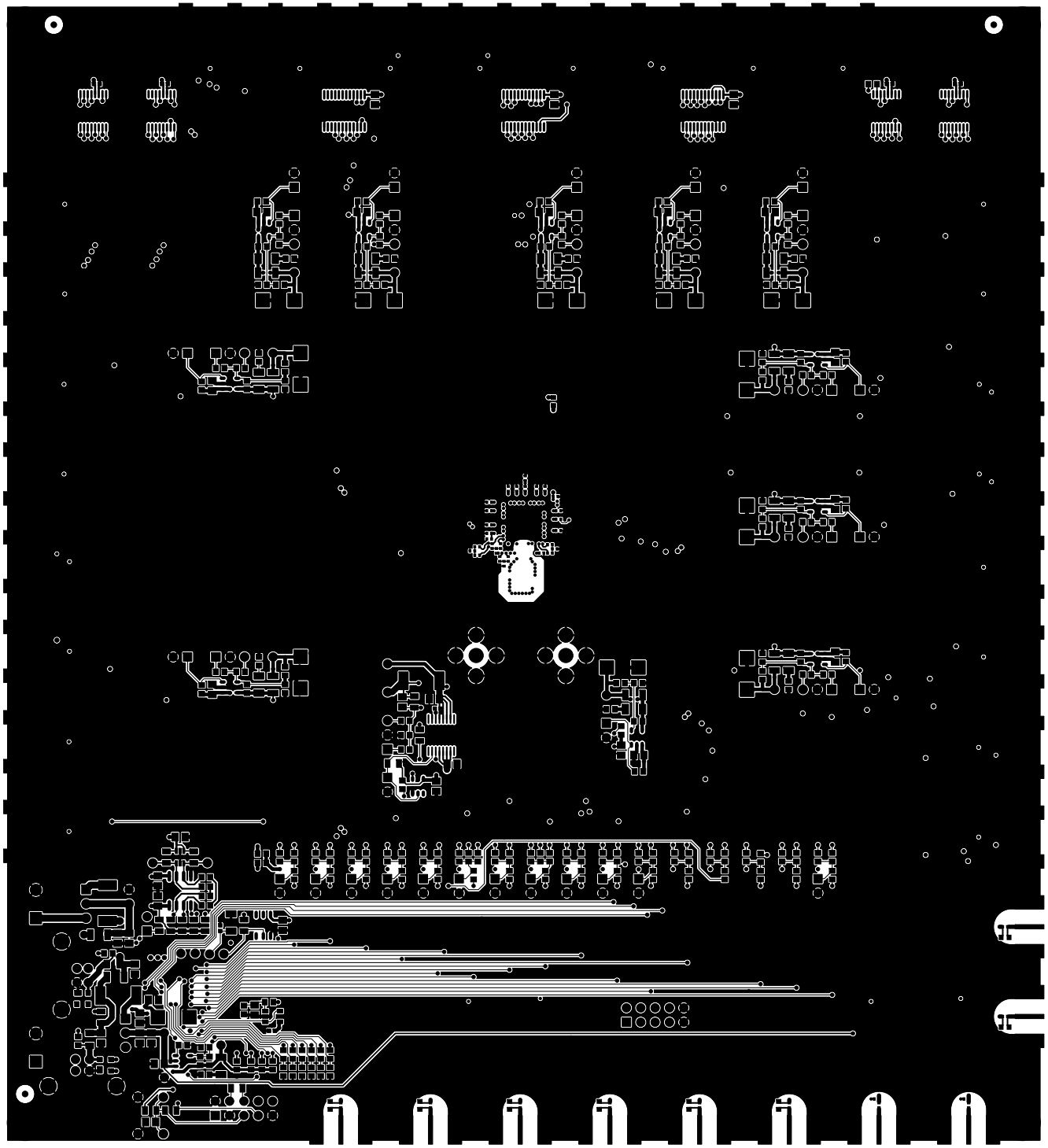
LAYER 06



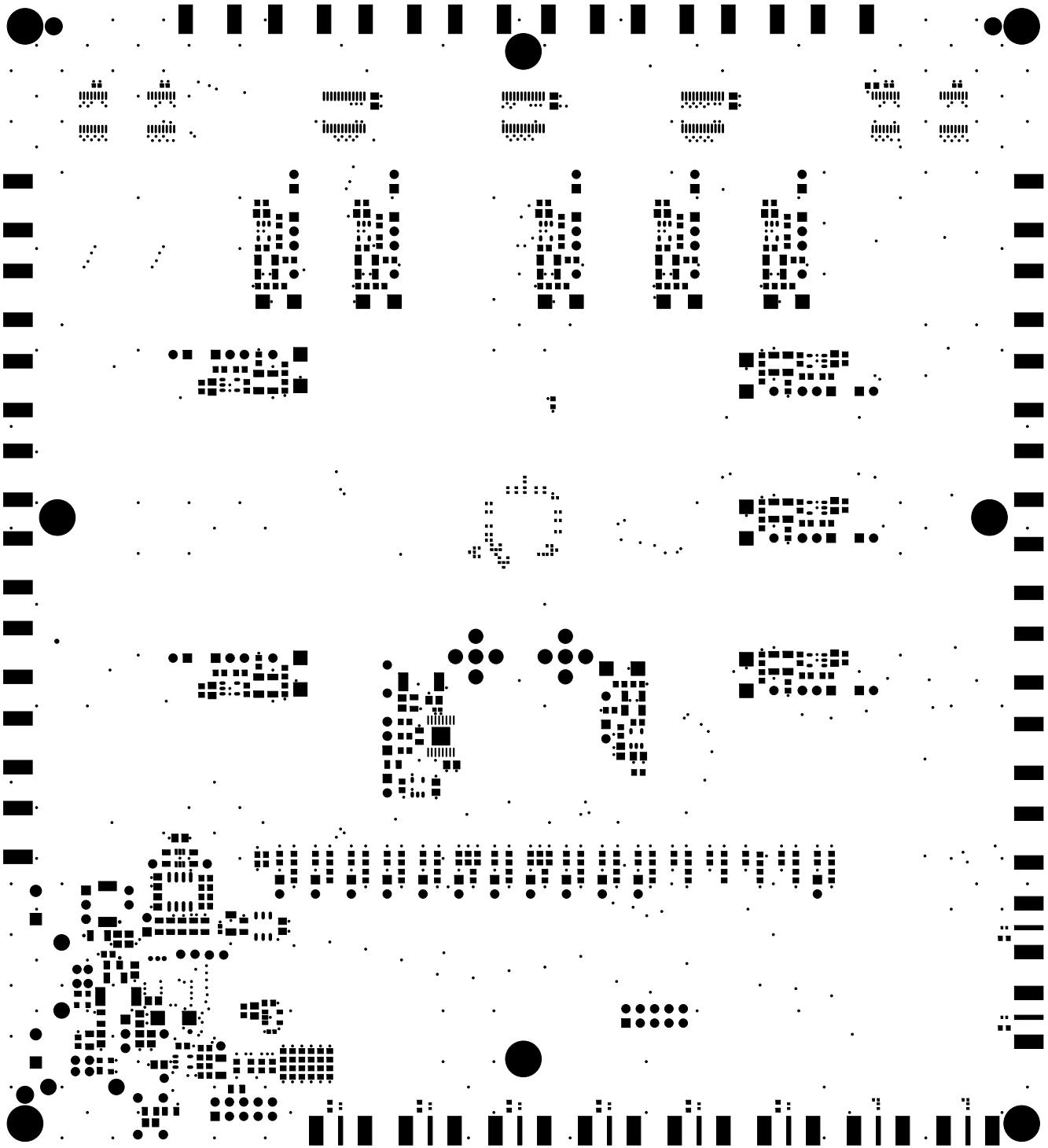
LAYER 07



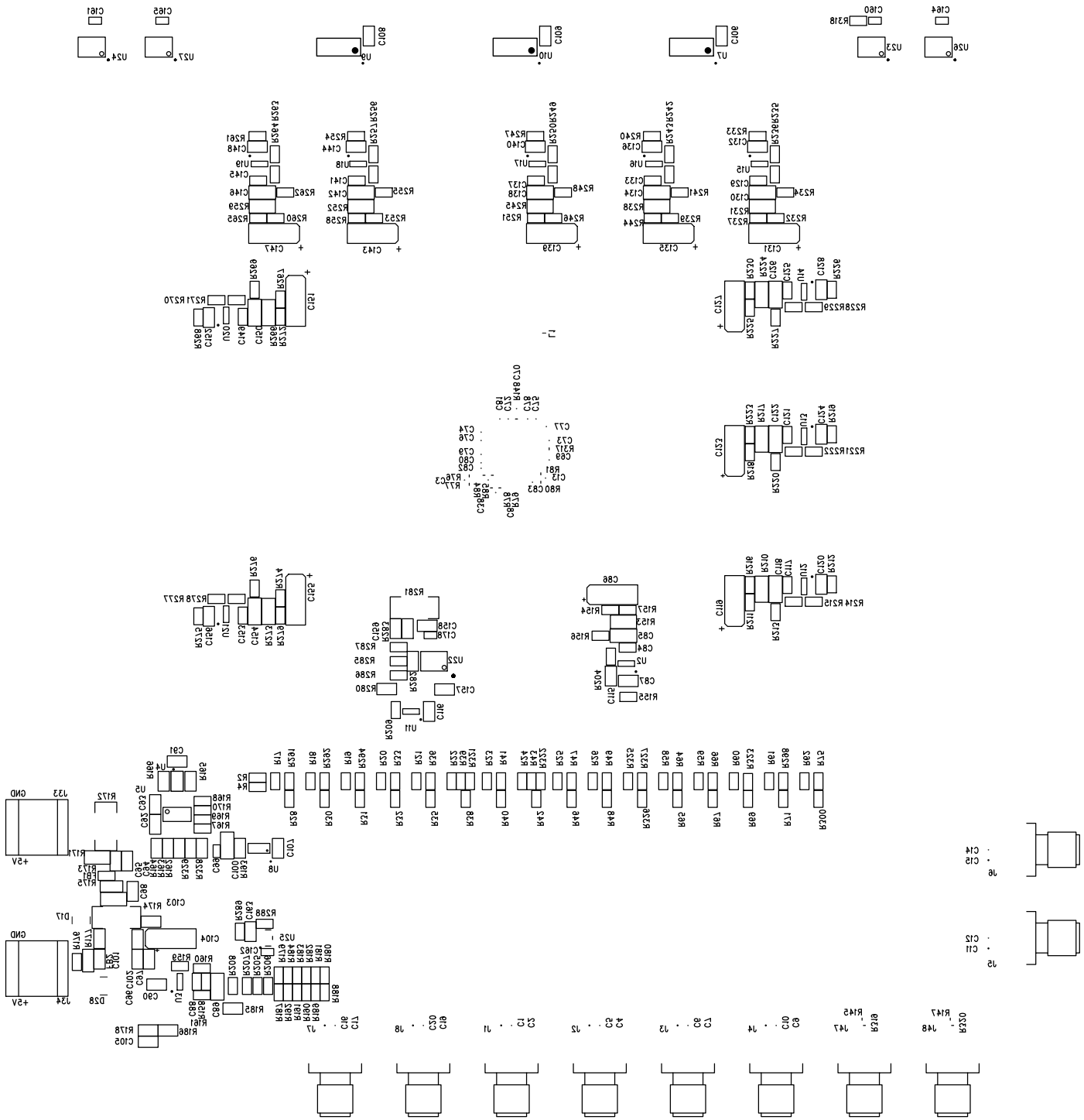
SECONDARY SIDE



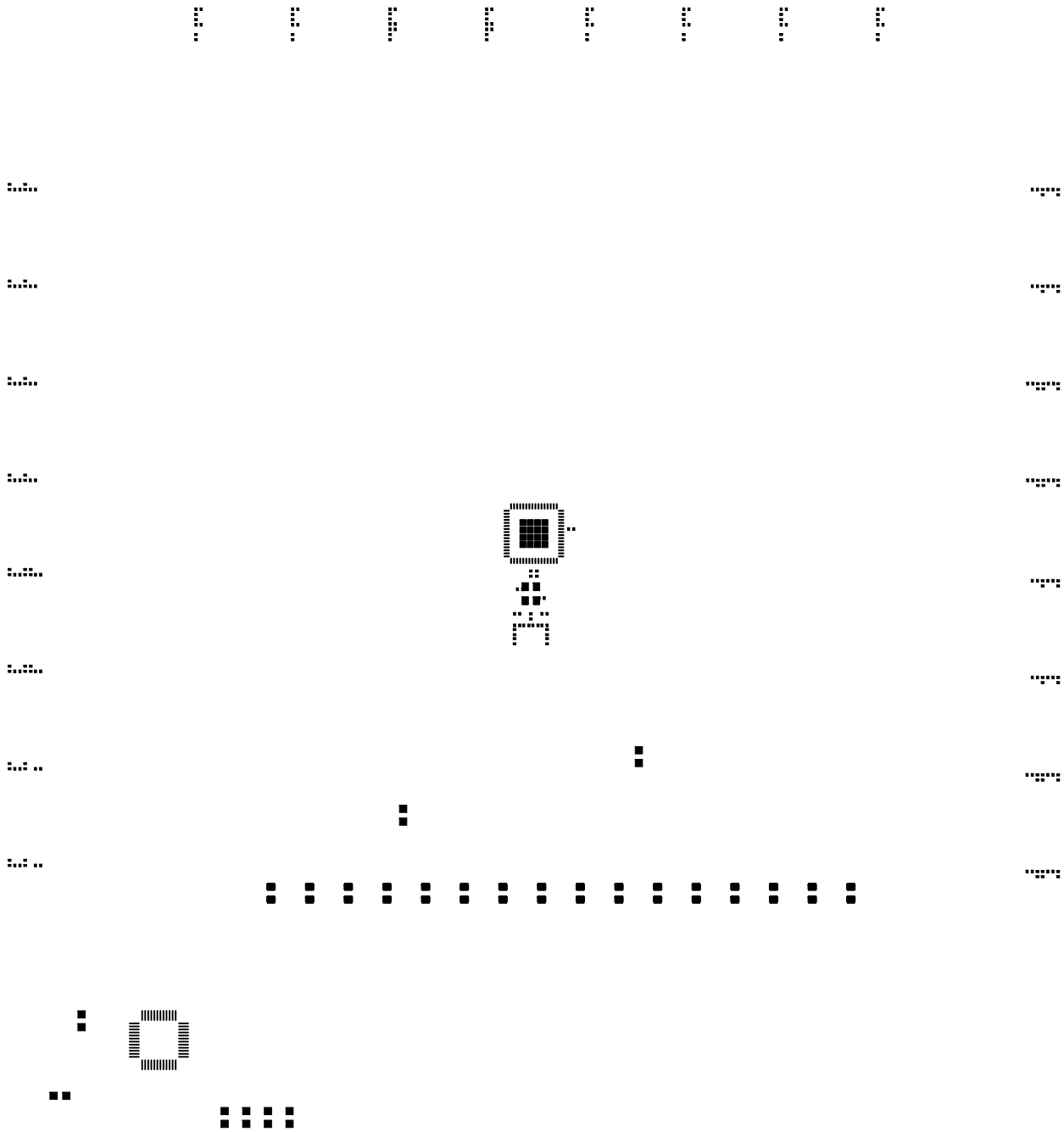
SECONDARY SOLDER MASK



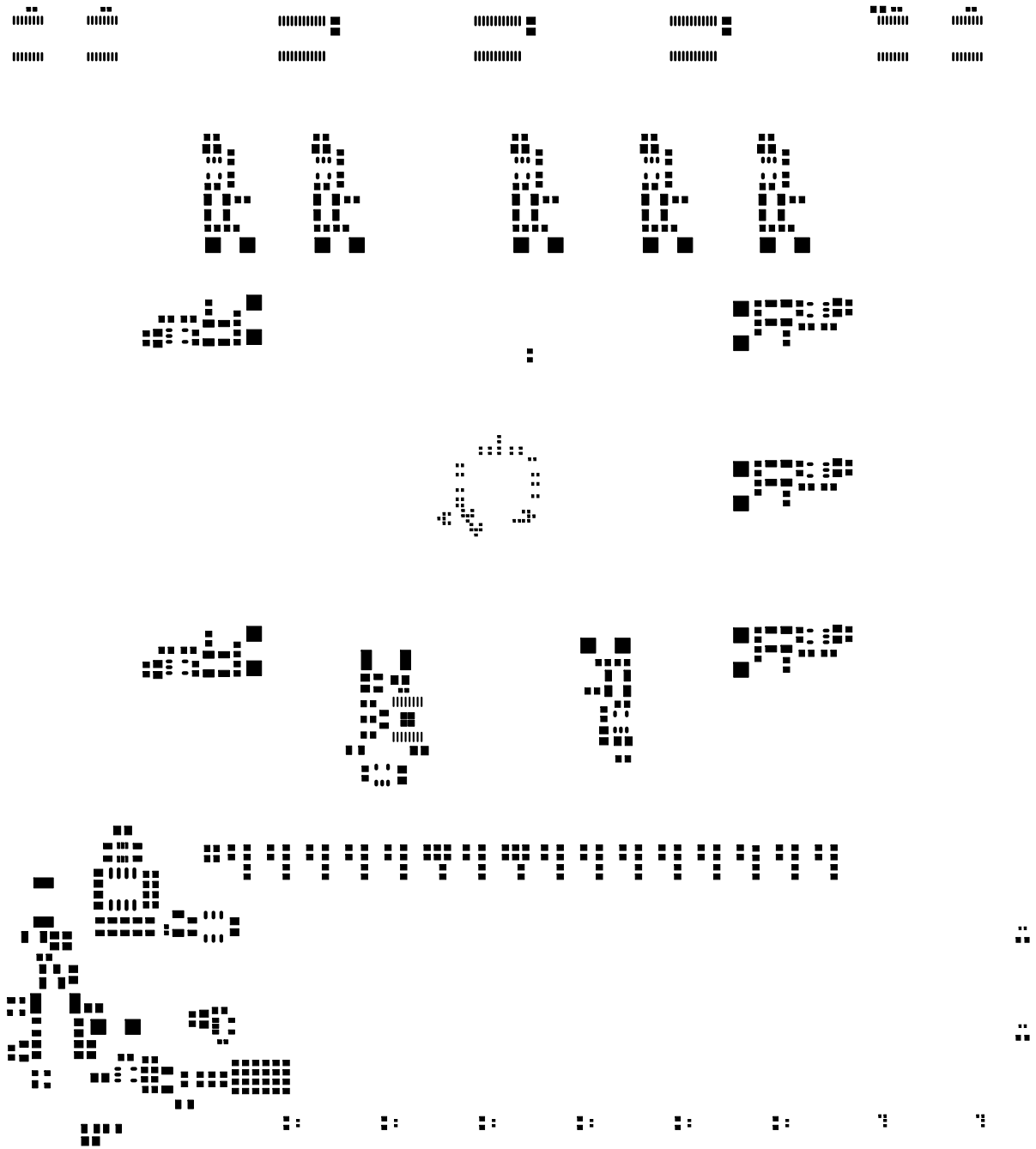
SECONDARY SILKSCREEN

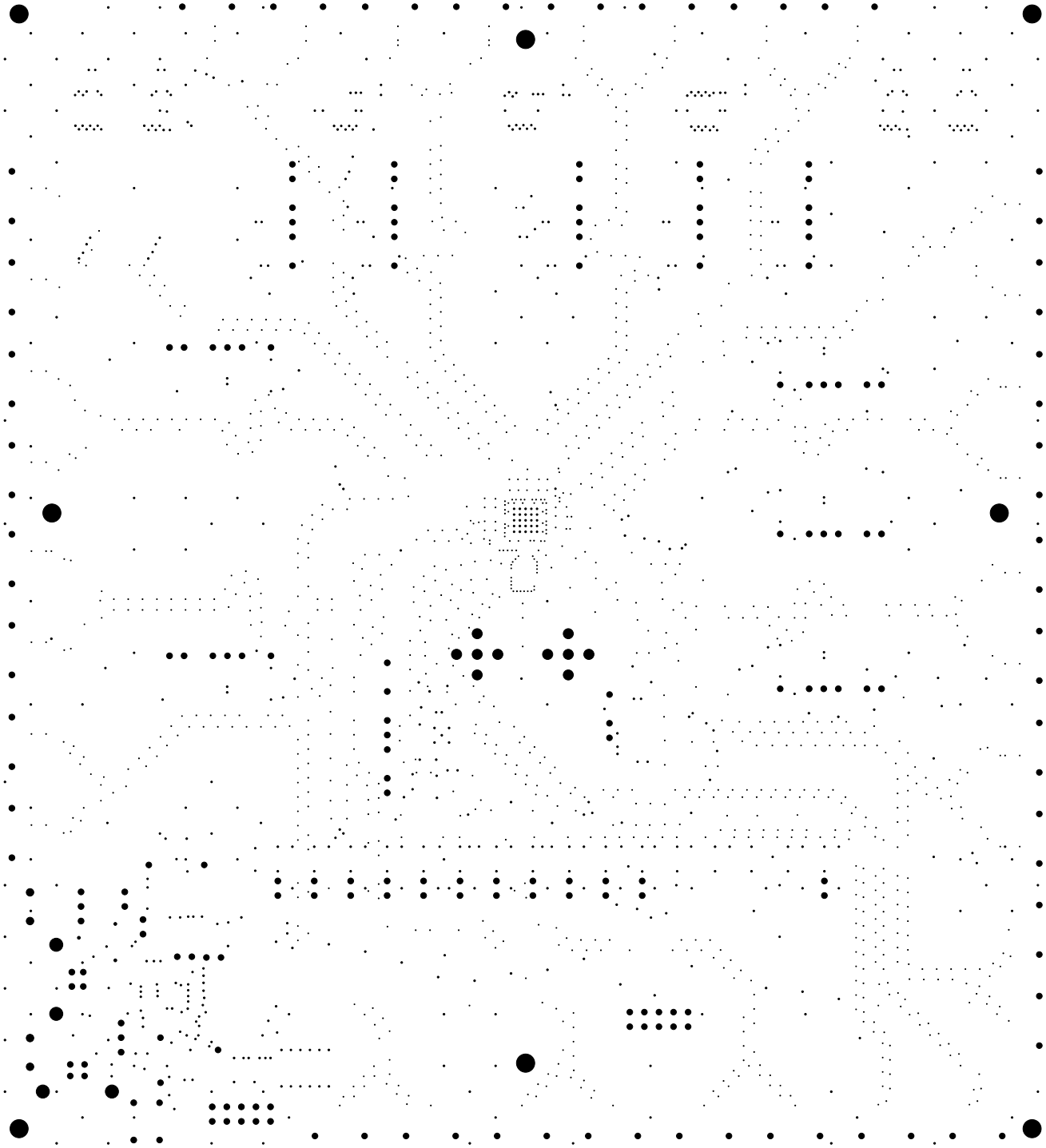


PRIMARY SOLDER PASTE

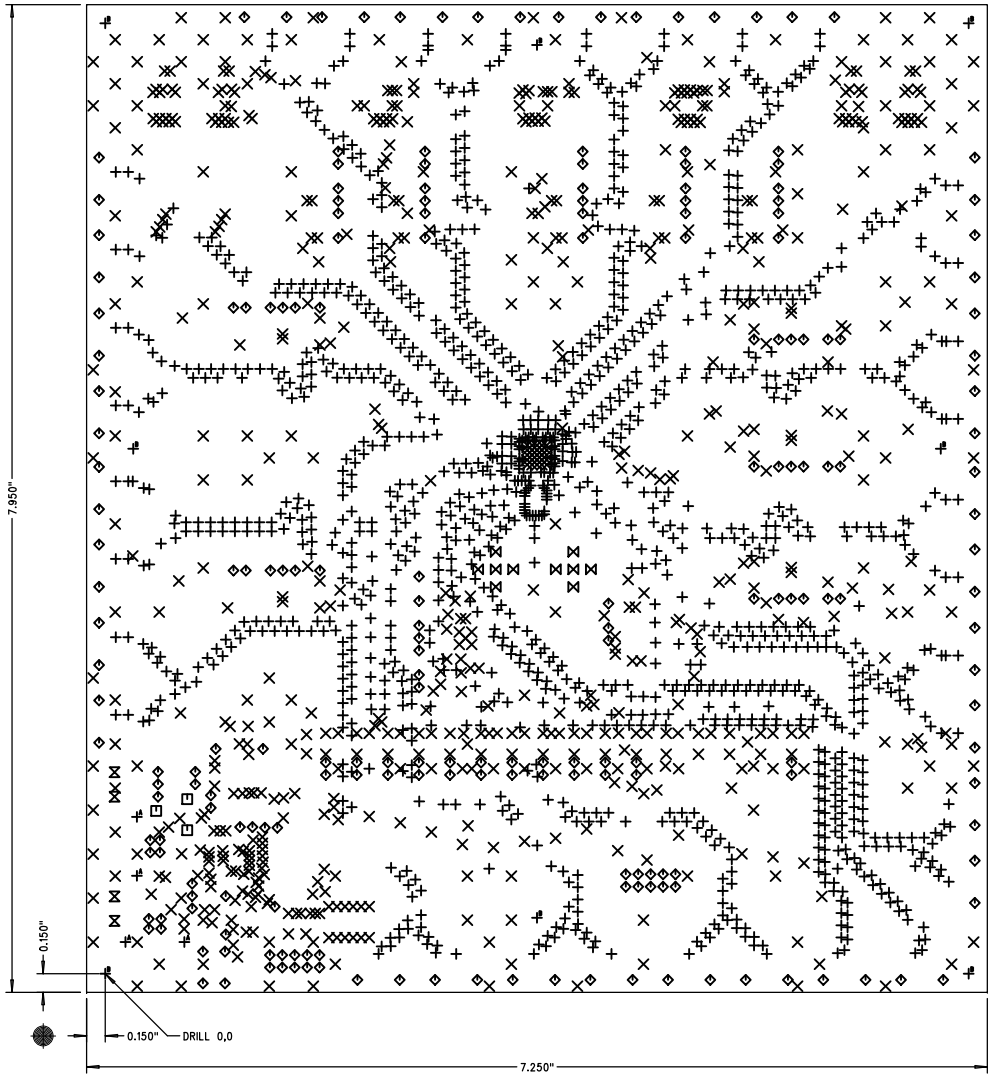


SECONDARY SOLDER PASTE



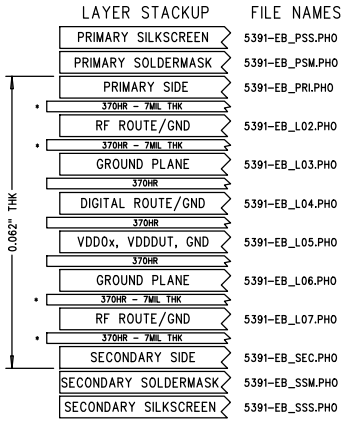


PRIMARY DRILL



NOTES : UNLESS OTHERWISE SPECIFIED

1. MANUFACTURE IN ACCORDANCE WITH IPC-6012, TYPE 3, CLASS 2.
2. END PRODUCT FEATURES SHALL NOT VARY MORE THAN 20% FROM ARTWORK ORIGINALS.
3. LAMINATE AND PREPREG SHALL BE AS PER IPC-4101/26,83,98 WITH A DECOMPOSITION TEMPERATURE >= 345°C, COLOR, NATURAL.
4. COPPER WEIGHT SHALL BE 0.5 OZ./SQ. FT. BEFORE PLATING.
5. ALL PLATED THROUGH HOLES SHALL HAVE A MINIMUM OF 0.001" COPPER.
6. DRILL HOLE TOLERANCE AFTER PLATING SHALL BE ±0.003".
7. MINIMUM ANNULAR RING SHALL BE 0.001".
8. MINIMUM ANNULAR RING AT EMERGENT CONDUCTORS SHALL BE 0.003".
9. FINAL PCB THICKNESS SHALL BE 0.062" ±10%.
10. WARP/TWIST SHALL NOT EXCEED 1.0%
11. FINISH SHALL BE LPI, BLUE SMOBC, ENIG BOTH SIDES.
12. SILKSCREEN WITH NONCONDUCTIVE WHITE EPOXY INK.
13. INTERNAL 0.175MM TRACES TO BE 50 OHM Zo ±5%.
    EXTERNAL 0.275MM TRACES TO BE 50 OHM Zo. ±5%.
    TOP 0.762MM TRACES TO BE 50 OHM Zo ±5% REF TO L03.
    BOTTOM 0.762MM TRACES TO BE 50 OHM Zo ±5% REF TO L06.
14. VENDOR TO PROVIDE PCB MICRO-SECTION OF COUPON AREA & TDR TEST REPORT.
15. REFERENCE ADDITIONAL FAB NOTES IN FILE README.TXT



SCALE: NONE

SIZE	QTY	SYM	PLT	TOOL	TOL
0.006	1379	+	P	1	+0/-0.006
0.012	699	×	P	2	+0/-0.012
0.020	3	□	P	3	+/-0.003
0.040	213	◇	P	4	+/-0.003
0.052	4	⧖	P	5	+/-0.003
0.070	10	⋈	P	6	+/-0.003
0.091	4	A	P	7	+/-0.003
0.125	8	B	P	8	+/-0.003

UNLESS OTHERWISE SPECIFIED

DIMENSIONS ARE IN INCHES AND APPLY AFTER FINISH
DIMENSIONS IN BRACKETS [ ] ARE IN MILLIMETERS
INTERPRET DRAWING PER MIL-D-1000

TOLERANCES
HOLE TOLERANCES PER 78027

DECIMALS	ANGLES	SURFACES
.XX +/- .XXX +/-	+/-	MICRONCHES

PART TO BE FREE OF BURRS

BREAK EDGES	BEND RADIUS	BEND RELIEF
MAX	MAX	MAX

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DESIGN	TT	21APR2017
LAYOUT	CT	06DEC2017

DO NOT SCALE DRAWING

COMPANY: SILICON LABS
400 W CESAR CHAVEZ ST.
AUSTIN, TX 78701
(512)416-8500
www.silabs.com

NAME: Si5391-EB

REV : 1.0

SIZE B

PART NUMBER:

SCALE 1:1

FABRICATION DRAWING

SHEET 1 OF 1