

*** PCB SPECIFICATION FOR BARE BOARD MANUFACTURING ***

PRODUCT OWNER : Silicon Labs Norway
DOCUMENT/BOARD : PCB5204 Rev A03
DATE : 2017-11-07 (Updated 2017-11-08)
REVISION : A03

PREPARED BY : Ole Jacob Bryhni Frostad
BOARDS pr PANEL: 12 (4 X 3)
PANEL SIZE : 210.2 x 205.4 mm
BOARD SIZE : 34.0 x 50.5 mm
BOARD THICKNESS: 1.6 mm +/- 10 %
NO OF LAYERS : 4
MATERIAL(S) : Glass Epoxy FR-4, NEMA Class 2, UL 94V-0, Tg min 150 C
Materials in compliance with the RoHS and WEEE directives
MARKINGS: Logo, Week/Year, UL (ON SECONDARY SIDE (BOT))
Avoid areas reserved for DataMatrix, Barcodes or Lables
QUALITY REQ. : IPC-A-600 (current revisions) Class 2, and IPC specifications
referred to by IPC-A-600
GENERAL REQ. : - Copper must not be added or removed from inside the board outline(s),
without written consent/approval.
If applicable, the following requirements are valid:
- If Build-Up (Stack-Up) is specified, follow Build-Up,
otherwise use (board manufacturer) standard Build-Up.
- Break-away areas may be used for patterns, holes etc
by manufacturer for QA purposes.
- If V-CUT, use angle 30 +/- 5 degrees.
V-CUT minimum remaining thickness 0.5 +/- 0.1 mm.
Use of V-CUT test pads is allowed.
- Inner radius (contour/outline) 1.2 mm, unless stated otherwise.
COPPER THK. : SEE BUILD-UP
COPPER PASSIV. : ENIG to meet IPC-4552 Class 2 requirements (current revision)
(Electroless Nickel/Immersion Gold)
RESIST MASK : Solder Mask Color: BLACK (NB! NON-STANDARD)
Photo Polymer Wet film
Thickness minimum 8 um, maximum 20 um
VIA HOLES : PLUGGED/FILLED, IPC-4761 (current revision) Type IV-b
Plugged and Covered Both Sides, Low CTE Plugging Paste
If Type IV-b is not available as a process, then Type IV-a
for the Top Side, and Overprinted (Tented) Bot Side is OK
u-Vias (microvias) must be 100% Copper Filled
LEGEND/SILKSCR.: WHITE, BOTH SIDES (TOP + BOT)
CONTROLLED IMP : Design has Controlled impedances. FOLLOW BUILD-UP STRICTLY!
Unless explicitly stated otherwise, controlled impedance
has been designed into the board. Use of test strip is
hence normally not required.
NOMINAL VALUES for Width, Spacing and VIA Diameter:
Cu TRACK(TRACE): Minimum conductor width : 0.125 mm (4.92 mil)
Cu SPACING : Minimum conductor spacing: 0.125 mm (4.92 mil)
Minimum via pad diameter : 0.5 mm (19.68 mil)

(SPECIFICATION CONTINUED ON NEXT PAGE)

BUILD UP :

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L1 ===== 35 um Cu (1.0 Oz) + Plating
- - - - P R E P R E G - - - - 325 um
L2 ===== 35 um Cu (1.0 Oz)
////////// C O R E ////////// 844 um (ca)
L3 ===== 35 um Cu
- - - - P R E P R E G - - - - 325 um
L4 ===== 35 um Cu (1.0 Oz) + Plating

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NB! Thicker than normal Top and Bottom Layer!

Core may be adjusted in order to reach correct board thickness

TEST

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: 100% Electrical Test
Optical test, AOI (with automatic scanner)
Visual inspection
(Generate netlist from Gerber and Drill files)

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Avoid use of 2125 Prepreg

If NB! is used in this specification, it is latin,
meaning "mark well" or "observe particularly"

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+++ YOUR CIRCUIT BOARD DESIGN PARTNER +++
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