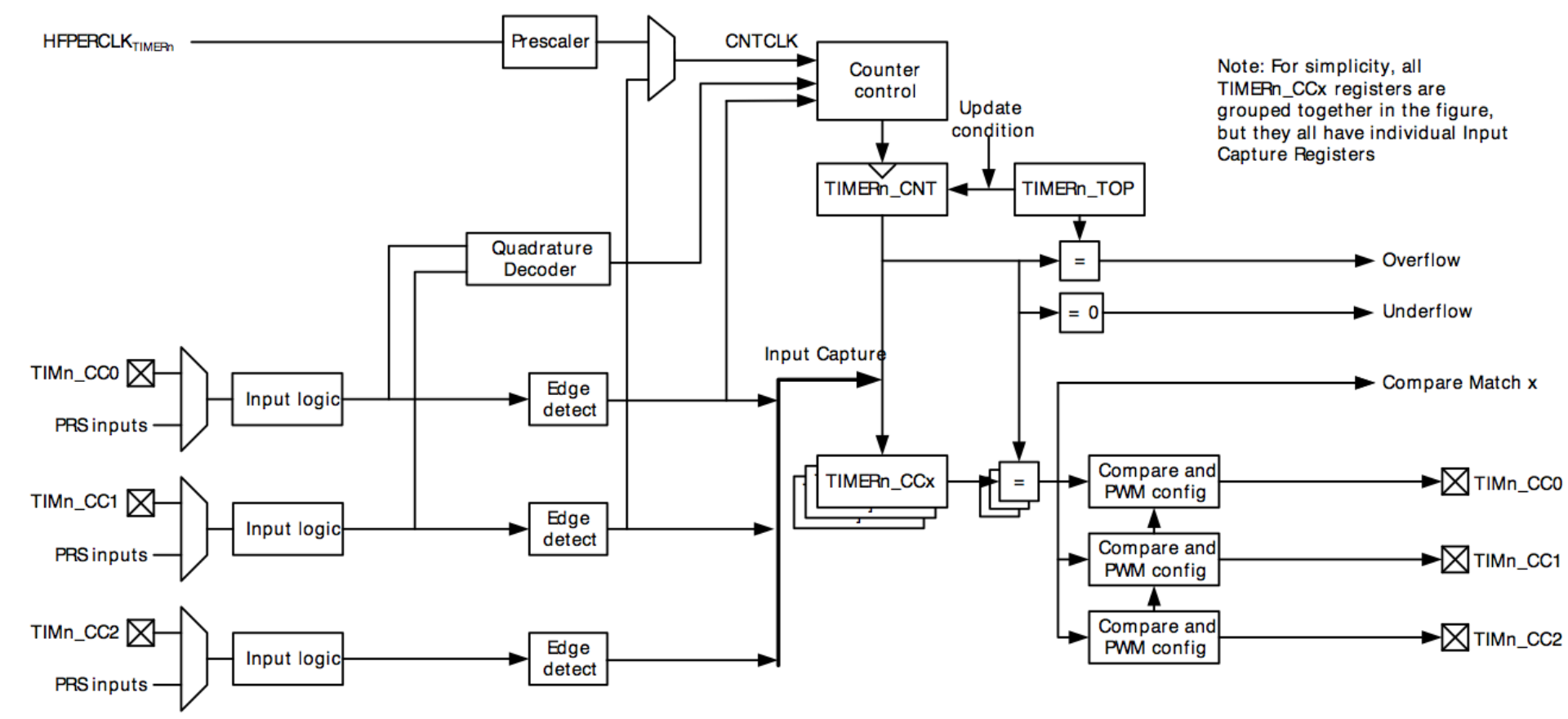
EFM32 Series 0: Timers and Counters

Real Time Counters

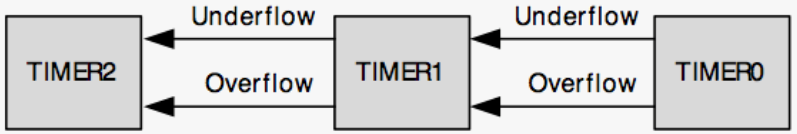
- RTC
  - 24 bit wide
  - Prescaler DIV by 1-32768
  - Two compare channels
  - Interrupts on compare match and overflow
- BURTC
  - 32 bit wide
  - Prescaler DIV by 1-128
  - One compare channel
  - Interrupts on compare match and overflow
  - Can operate in EM4 and backup mode
  - Reset by pin reset
- Slightly lower current consumption than RTC
  - Allows LFA branch to be turned off
- Interrupt timing: Flag set at end of period

TIMER


HFPERCLK$_{TIMERn}$
Prescaler
CNTCLK
Counter control
Update condition
TIMERn_CNT
TIMERn_TOP
Note: For simplicity, all TIMERn_CCx registers are grouped together in the figure, but they all have individual Input Capture Registers
Quadrature Decoder
=
Overflow
= 0
Underflow
Input Capture
Compare Match x
TIMn_CC0
PRS inputs
Input logic
Edge detect
TIMERn_CCx
=
Compare and PWM config
TIMn_CC0
TIMn_CC1
PRS inputs
Input logic
Edge detect
Compare and PWM config
TIMn_CC1
TIMn_CC2
PRS inputs
Input logic
Edge detect
Compare and PWM config
TIMn_CC2

TIMER

- 16 bit wide
  - Up to 3 TIMERs can be daisy-chained to a 48-bit counter



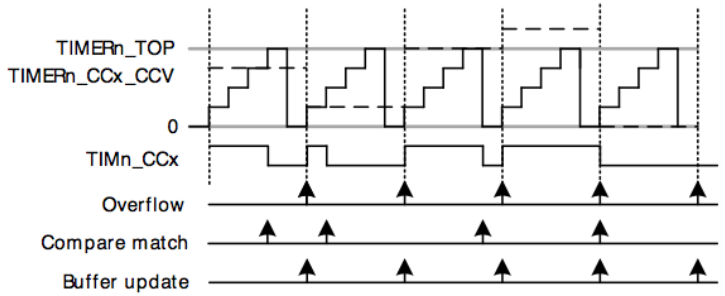
  - 2x mode (counts and compares on rising+falling edge)

- Counter modes:
  - Up-count
  - Down-count
  - Up/down-count
  - Quadrature decoder

TIMER

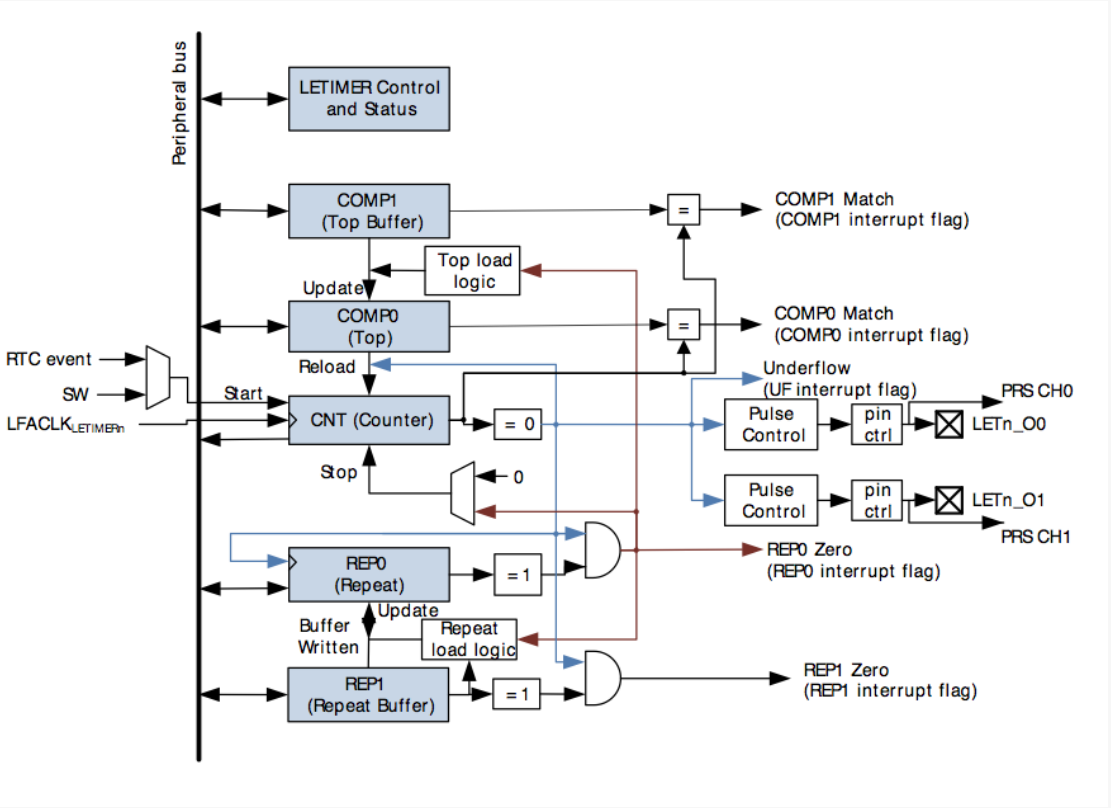
- Capture/Compare
  - Input capture
    - Period/pulse-width measurement
  - Output compare
    - Frequency generation

- PWM generation
  - Dead-Time Insertion for BLDC motors
    - DTI not available on TG
    - Application Note in writing (using SiLabs BLDC demo board)

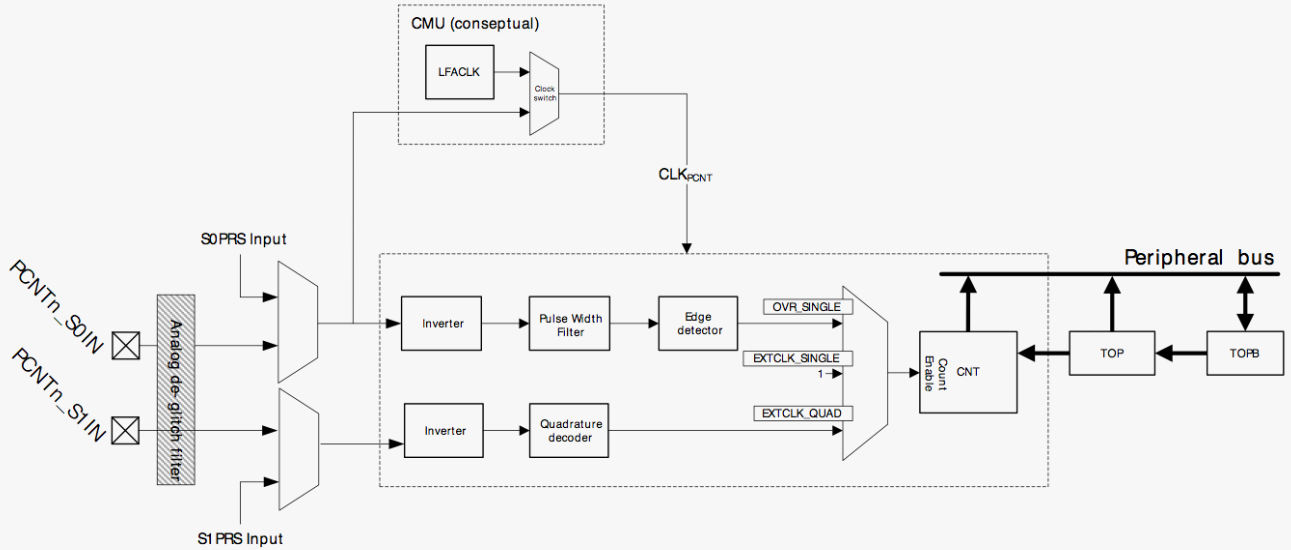


LETIMER

- 16-bit down-counter
- 2 compare channels
- Repeat modes:
  - Free
  - One-shot
  - Buffered
  - Double
- PWM generation
- Interrupt:
  - compare match
  - underflow
  - repeat done
- Duty cycle external components or sensors
  - Example: COM line inversion on memory LCD

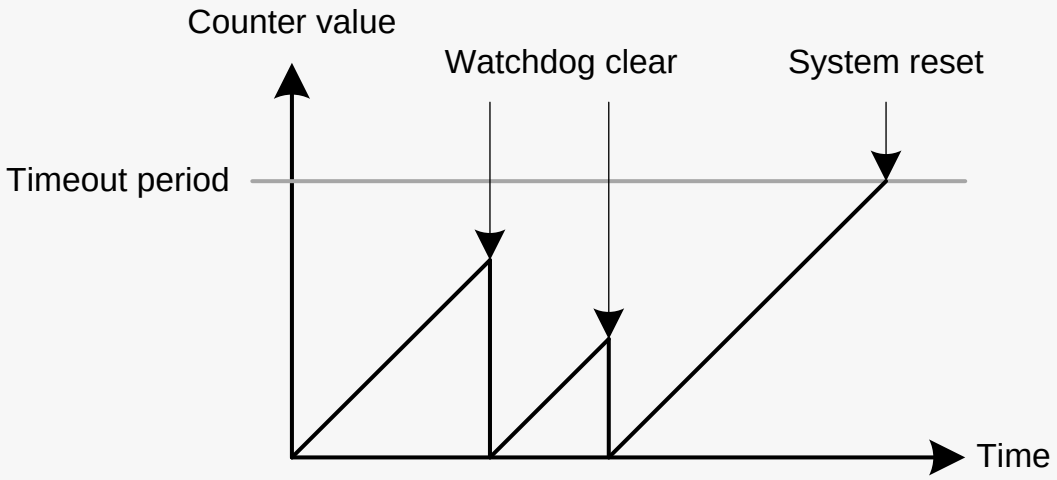


PCNT



- Operating modes:
  - Single input oversampling
    - Count direction can be controlled by external pin
  - Externally clocked single input counter
    - PCNT clocked by input signal
    - Operates without LF clock => EM3
    - Pulse-width filter not available
  - Externally clocked quadrature decoder
- Register update
  - External clock => 2-3 ext. clock synchronization delay

WATCHDOG



- Watchdog Timer Highlights
  - Timeout from 9 to 262145 clock cycles (2^(3+n)+1)
  - Clock source: ULFRCO/LFXO/LFRCO
  - Lock WDOG registers to avoid unintentional changes
  - Available down to EM3 (ULFRCO)

- Errata:
  - G/TG: Set EM3RUN to keep WDOG running in EM2 (LFXO only)
  - Older revisions: WDOG keeps running in EM2/EM3 => RESET

SILICON LABS

www.silabs.com/efm32