



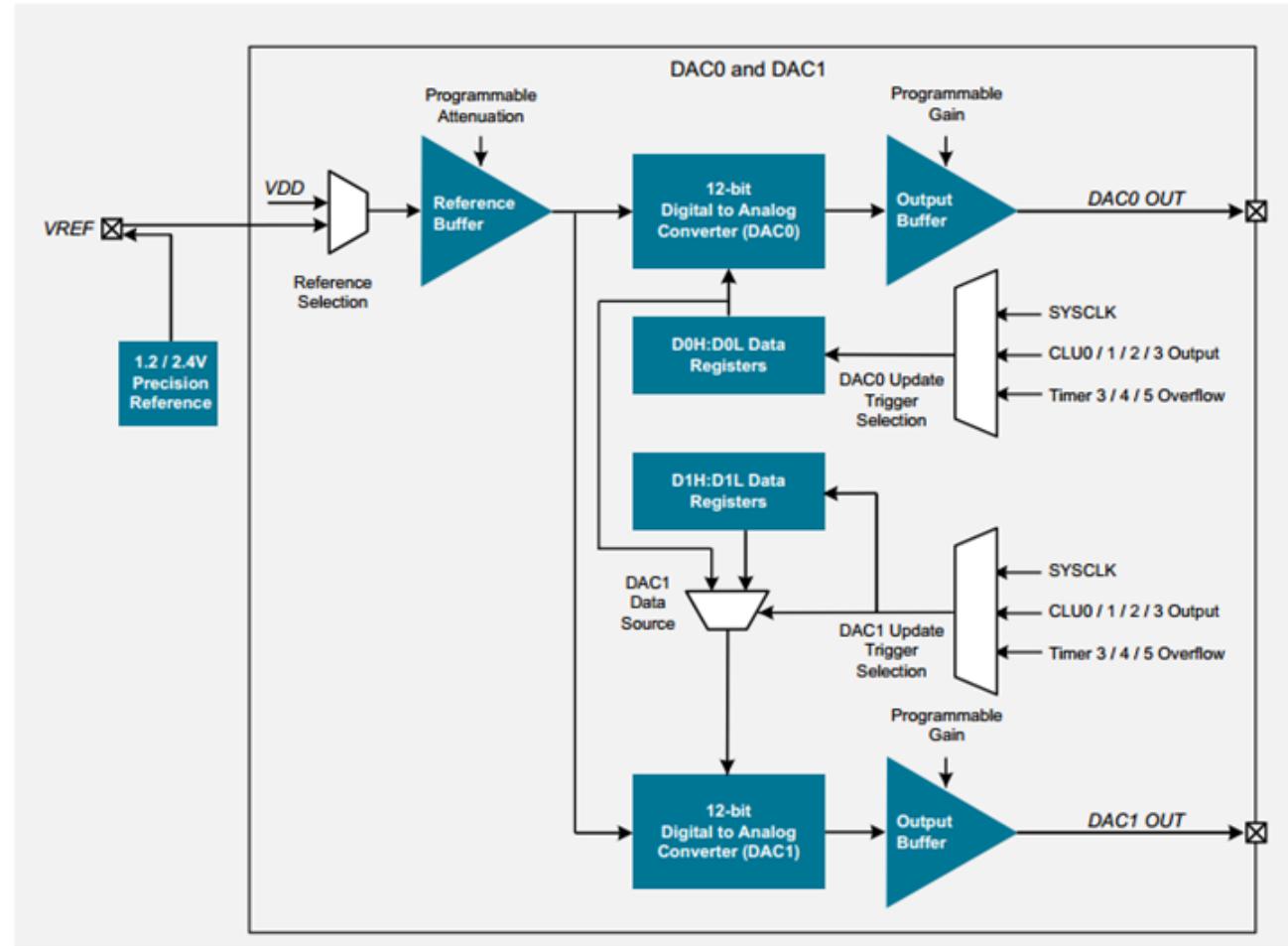
EFM8LB1 – Digital to Analog Converter (DAC)

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Agenda

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DAC Overview



DAC0 and DAC1 Pair Block Diagram

- EFM8LB1 DAC can output constant voltage between 0V – 3.6V.
- The DACs don't require any clocks to maintain the output voltage.
- Four DACs are included, organized in pairs: DAC0/1, DAC2/3.
- Each DAC has 12-bit resolution.

General Operation – Output Voltage

- Output Voltage
 - The output voltage is decided by DAC data input, the reference voltage, the reference buffer attenuation setting and the output buffer gain. The formula as follows.

$$\text{DAC Output(V)} = (\text{DAC Data} / 4096) \times \text{VREF} \times \text{Attenuation} \times \text{Gain}$$

- Each factor in formula is discussed in further detail in the following section.

General Operation - Data Word

- Data Word
 - The 12-bit data input to the DAC contains two registers DACnH and DACnL.
 - Always write to the DACnL register first, then write to the DACnH register.
 - The data is right justified by default.
 - DAC1 and DAC3 Features, Using DAC1 as an example.
 - The DAC1 D1SRC field allows four data sources,
 - DAC1 and DAC0 data register, and inverse value of them.
 - The DAC1 D1AMEN bit provides additional options for generating DAC1 input data.
 - Alternate mode, DAC1 updates are based on the logical level of the trigger source.
 - When DAC1 trigger is low, DAC1 receives the DAC1 data register.
 - When DAC1 trigger is high, DAC1 receives the data source selected in D1SRC.
 - The trigger source must be one of the Configurable Logic Units.

General Operation – Reference Voltage, Attenuation, Gain

- Reference Voltage
 - The reference voltage range is 1.15v – 3.6v.
 - The reference for each DAC pair can be independently selected.
 - The reference voltage options are VDD pin (default setting) and VREF pin.
 - It is recommended to use VREF pin as reference voltage.
 - Route internal precision 1.2/2.4v voltage reference to VREF pin.
 - Configure VREF pin as analog mode using the PnMDIN register.
- Reference Buffer Attenuation and Output Buffer Gain
 - The reference voltage can be scaled by 1/2 , 1/2.4, or 1/3.
 - The DAC output can be scaled by 2, 2.4 or 3.

General Operation – Turning the DAC On/Off, Output Pin

- Turning the DAC On/Off
 - EN bit in the DACnCF0 register turns on the DAC and drive its respective pin.
 - The EN bit only affects the analog circuitry and its respective pin. That means you can access the its registers even if the associated DAC is disabled.
- Output Pin
 - Each DAC has a single output pin at a fixed location in the table below.
 - When using the DAC output, the pin should be configured to analog mode using the PnMDIN register.

DAC Output	32-Pin Packages	24-Pin Packages
DAC0 Output	P3.0	P2.0
DAC1 Output	P3.1	P2.1
DAC2 Output	P3.2	P2.2
DAC3 Output	P3.3	P2.3

General Operation – Update Trigger

- Update Trigger
 - The DAC output is updated by hardware by a trigger, and options as follows,
 - SYSCLK(default setting)
 - Timer 3/4/5 high byte overflow
 - Configurable Logic output 0/1/2/3 rising edge
 - SYSCLK as update trigger, the DAC output is updated one system clock after writing to DACnH.
 - Firmware can set DnUDIS bits to disable DAC updates. Write values to multiple DAC input data registers, and then update all of the DAC outputs on the same clock edge by clearing the appropriate DnUDIS bits.

Firmware Example

- Sine wave software example
 - The example uses VREF 2.4V and output 1 kHz sine wave on all four DACs.
 - The Timer 3 200 kHz overflow as the update trigger.
- Function Generator demo
 - The example uses Timer 4 as the update trigger.
 - The available functions are sine, square, triangle, saw tooth, and windowed sine.
 - The frequency options are 10 Hz, 20 Hz, 50 Hz, 100 Hz, 200 Hz, 500 Hz, 1 kHz, 2 kHz, 5 kHz.
 - The function and frequency are displayed on the screen.

Thank you!