UG382: WF200 Hardware Design User's Guide

The purpose of this guide is to help users design WiFi applications using the WF200.

KEY FEATURES

- Schematics guidelines
- BOM selection guideline
- RF matching guideline
- Layout guideline
- Package information

Table of Contents

1. WF200 Pinout

WF200 is a 4 x 4 mm 32-pin QFP package. The diagram below describes the pinout (top view) .

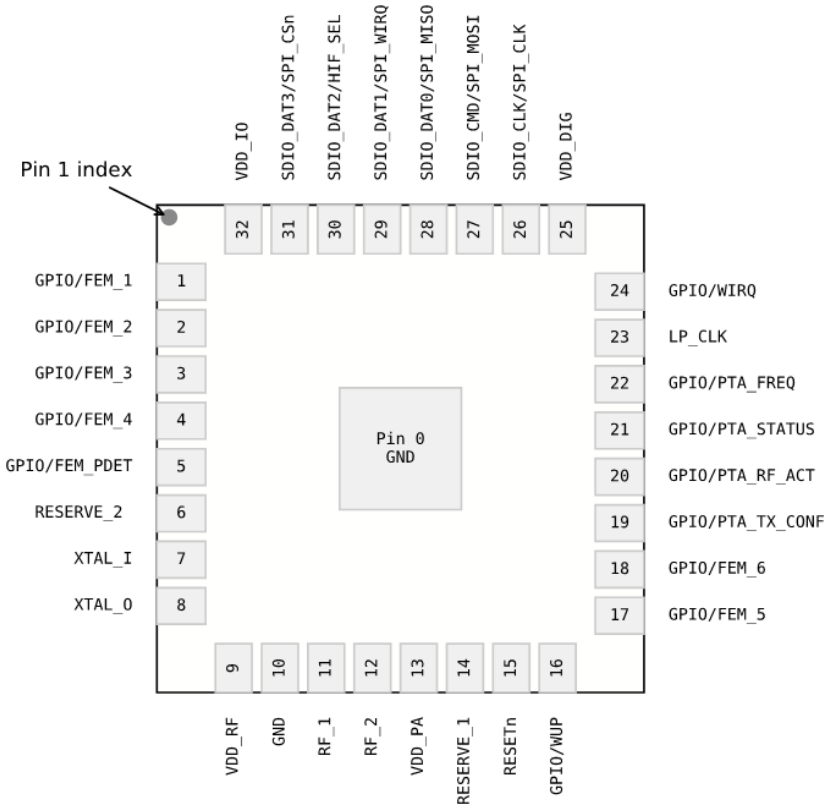


Figure 1.1. WF200 Pinout

Table 1.1. WF200 Pin Descriptions

Pin #	WF200 Pin Name	Description
1	GPIO/FEM_1	These pins can be used for dynamic control of an external front-end module (FEM), otherwise this can be used as GPIO.
2	GPIO/FEM_2	
3	GPIO/FEM_3	
4	GPIO/FEM_4	This pin can be used for dynamic control of an external Power Amplifier, otherwise this can be used as GPIO.
5	GPIO/FEM_PDET	This pin can be used as an analog input to be connected to a Power Amplifier detector output (Vdet) in case an external Power amplifier or a FEM is used. Otherwise, it can be used as a GPIO.
6	RESERVE_2	Reserved. This pin should be left unconnected.
7	XTAL_I	Crystal Oscillator input port, or external clock input.
8	XTAL_O	Crystal Oscillator output port.
9	VDD_RF	Power supply for the RF part.
10	GND	Ground pin.
11	RF_1	RF_1 input / output port. If not used, this pin should be connected to GND through a 50 Ω resistor.
12	RF_2	RF_2 input / output port. If not used, this pin should be connected to GND through a 50 Ω resistor.

Pin #	WF200 Pin Name	Description
13	VDD_PA	Power supply for the Power Amplifier.
14	RESERVE_1	Reserved. For normal operation, this pin must be grounded.
15	RESETn	RESET pin, active Low.
16	GPIO/WUP	This pin should be used to wake-up the chip while in sleep mode, or can be used as a GPIO.
17	GPIO/FEM_5	These pins can be used for dynamic control of an external front-end module (FEM), otherwise this can be used as GPIO.
18	GPIO/FEM_6	
19	GPIO/PTA_TX_CONF	As part of PTA interface, these pins can be used to manage coexistence with another 2.4 GHz radio or can be used as a GPIO.
20	GPIO/PTA_RF_ACT	
21	GPIO/PTA_STATUS	
22	GPIO/PTA_FREQ	
23	LP_CLK	Low Power clock input. This pin is typically connected to a 32 kHz reference clock. If not used, this pin should be connected to GND.
24	GPIO/WIRQ	This pin can be used as an IRQ to host for SDIO or can be used as a GPIO.
25	VDD_DIG	Power supply for the digital part.
26	SDIO_CLK/SPI_CLK	Host interface: SDIO_CLK or SPI_CLK.
27	SDIO_CMD/SPI_MOSI	Host interface: SDIO_CMD or SPI_MOSI.
28	SDIO_DAT0/SPI_MISO	Host interface: SDIO_DAT0 or SPI_MISO.
29	SDIO_DAT1/SPI_WIRQ	Host interface: SDIO_DAT1 or WIRQ.
30	SDIO_DAT2/HIF_SEL	Host interface selection: Used to select the host interface during reset rising edge. If Low, selects SPI interface. When High, selects SDIO interface and this pin becomes SDIO_DAT2.
31	SDIO_DAT3/SPI_CSn	Host interface: SDIO_DAT3 or SPI_CSn.
32	VDD_IO	Power supply for I/Os.
0	EDP	Exposed die pad to connect to GND.

2. Device Configuration

The configuration linked to the hardware platform (RF pins, configurable pins, etc.) is achieved through firmware by downloading a dedicated binary file (a so-called PDS file, which stands for "Platform Data Set") just after firmware download and before operation. More details on device configuration will be provided in an upcoming application note.

Table 2.1. WF200 Pin Status and Impedance

Pin #	Pin Name	I/O	Configuration	
			Reset[1]	After Boot
1	GPIO/FEM_1	I/O	Tristate	According to PDS
2	GPIO/FEM_2	I/O	Tristate	According to PDS
3	GPIO/FEM_3	I/O	Tristate	According to PDS
4	GPIO/FEM_4	I/O	Tristate	According to PDS
5	GPIO/FEM_DET	I/O	Tristate	According to PDS
7	XTAL_I	I	20.2 pF	According to PDS
8	XTAL_O	O	20.2 pF	According to PDS
11	RF_1	I/O	18.6+j9.6 Ω at 2442 MHz	
12	RF_2	I/O	18.6+j9.6 Ω at 2442 MHz	
15	RESETn	I	43 kΩ pull-up resistor	
16	GPIO/WUP	I/O	Tristate	According to PDS
17	GPIO/FEM_5	I/O	Tristate	According to PDS
18	GPIO/FEM_6	I/O	Tristate	According to PDS
19	PTA_TX_CONF	I/O	Tristate	According to PDS
20	PTA_RF_ACT	I/O	Tristate	According to PDS
21	PTA_STATUS	I/O	Tristate	According to PDS
22	PTA_FREQ	I/O	Tristate	According to PDS
23	LP_CLK	I	No-pull resistor	
24	GPIO_WIRQ	I/O	Tristate	According to PDS

Note:
1. All digital I/Os are in tristate except pin LP_CLK, which is configured as input.

3. Features Description

3.1 RF Ports

The WF200 has two RF ports: RF_1 and RF_2. Any of the RF ports can be used in a similar way. However, note that RF_2 output power is around 1 dB lower than that of RF_1. There can be several configurations for the RF part, as described below:

- Single antenna: for this case, any RF pin can be used.
- Antenna diversity without external FEM: in this case, both RF_1 and RF_2 ports are connected to their respective antennas, and, over time, the WF200 selects the antenna that provides the best budget link to optimize performance, range, and throughput.
- Use of an external Front-End Module (FEM): In this case, one port is used for Tx and the other for Rx.

This RF configuration is set with the PDS file.

3.2 Host Interface

The host interface allows control of the WF200 by an MCU or SoC using either SPI or SDIO. Selection between SPI and SDIO is done upon the logic state on the SDIO_DAT2/HIF_SEL pin during the rising edge of the RESETn signal. If this signal is HIGH, the host interface is configured as SDIO; otherwise, it is configured as SPI.

This is summarized in the table below:

Table 3.1. WF200 Host Interface Configuration

WF200 Pin name	SPI Mode		SDIO Mode	
RESETn	0 → 1	1	0 → 1	1
SDIO_DAT2/HIF_SEL	0	x	1	SDIO_DAT2
SDIO_CLK/SPI_CLK	x	SPI_CLK	x	SDIO_CLK
SDIO_CMD/SPI_MOSI	x	SPI_MOSI	x	SDIO_CMD
SDIO_DAT0/SPI_MISO	x	SPI_MISO	x	SDIO_DAT0
SDIO_DAT1/SPI_WIRQ	x	WIRQ	x	SDIO_DAT1
SDIO_DAT3/SPI_CSn	x	SPI_CSn	x	SDIO_DAT3

Besides the host interface main signals, a couple of pins also complement the host interface.

- The GPIO/WIRQ pin can optionally be used in SDIO mode to provide the Interrupt request to the host in case a given host does not support in-band IRQ. It is also used to wake up the host in case it is in a power saving mode with the host interface inactive. If this is not required, the pin can be configured as GPIO.
- The GPIO/WUP pin should be used by the host to wake up the WF200 when in power-save mode. If power save mode is not enabled on the WF200, this pin can be used as a GPIO. Note that this pin should be LOW to enable the WF200 to reach sleep or standby modes.

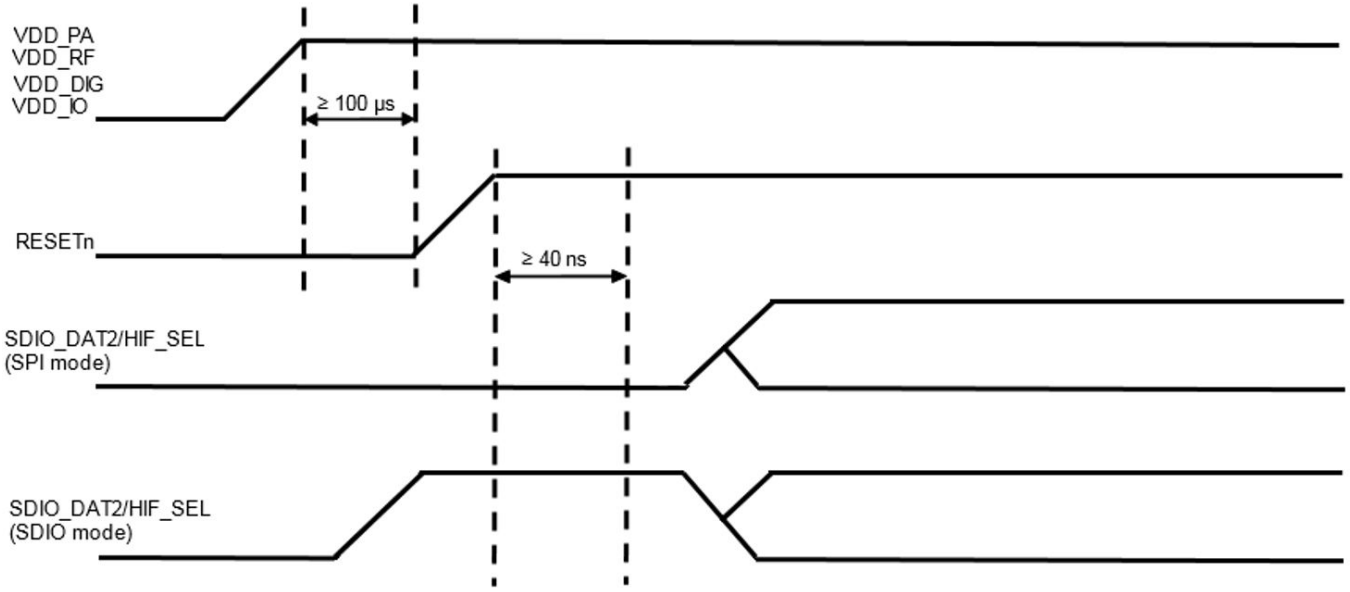


Figure 3.1. WF200 Power Up and Host Interface Timing Parameters

3.3 Programmable Pins

3.3.1 Multi-Protocol Coexistence

Refer to the WF200 Data Sheet for more details.

3.3.2 FEM

FEM pins can be used to control a potential Front-End Module (FEM). The FEM interface is composed of seven pins as described below:

- FEM_PDET is an analog input that is connected to the Tx Power Amplifier detector output for Tx power control. The voltage range on this input is 0 to 1.2 V, which matches most of Power Amplifiers' detector output.
- FEM_4 is the signal to be used as Power Amplifier enable.
- FEM_1 to FEM_3, FEM_5 and FEM_6 are used to dynamically control the FEM during Tx and Rx. All other FEM_x signals are configurable thanks to an embedded LookUp Table. This facilitates PCB layout as a given FEM control signal can be generated by any of these pins. The LUT also enables to adapt to any FEM control logic. Configuration of FEM signals is achieved thanks to the downloaded PDS file.

Available pins can also be configured to monitor the WLAN activity, that is, to drive an LED during Tx and another one during Rx, or a single one during Tx/Rx.

Details regarding FEM control and signals configurations will be provided in an upcoming application note.

3.3.3 Common Features for Programmable Pins

In this section, programmable pins refer to GPIO/FEM_xx pins (7 pins), GPIO/PTA_xx pins (4 pins), GPIO/WUP and GPIO/WIRQ.

Each of these pins has the following features:

- Configurable slew rate, to optimize power consumption.
- Programmable pull-up or pull-down. Resistance value for such pull-up or pull-down is 43 kΩ typical.

These features are available whether the pin is used as a GPIO or in “functional” mode and are configured through the PDS file.

3.4 Clocks

WF200 requires a reference clock that has to be at 38.4 MHz. This reference clock is either generated with its crystal oscillator or provided by an external device.

3.4.1 Crystal Use Case

When using the crystal oscillator, the external Xtal should be connected between the XTAL_I and XTAL_O pins, and external load capacitors are not required. The WF200 embeds adjustable load capacitors on both the XTAL_I and XTAL_O pins, and these capacitors can be trimmed independently to adapt to the application and adjust the oscillator frequency. The load capacitance settings are configured within the PDS file.

Xtal requirements are detailed in the data sheet.

3.4.2 External Clock Case

If an external clock is used, the clock should be provided to XTAL_I pin, and XTAL_O pin can be either left unconnected or grounded.

Electrical requirements for external reference clock are detailed in the data sheet.

3.4.3 Low-Power Clock

Additionally, WF200 has a provision for a 32 kHz clock input (LP_CLK pin) that allows the lowest power consumption (sleep state) while in power save mode. This clock can be used during sleep mode and should be a square wave with I/O levels complying with IO pin requirements.

Minimizing battery current between Rx beacons requires ±1000 ppm frequency tolerance. Most hosts have 32 kHz that can be shared to WF200. Refer to the WF200 Data Sheet for more details regarding low-power clock requirements.

4. Power Supplies

WF200 has four power supplies pins respectively dedicated to the Power Amplifier (VDD_PA), the RF part (VDD_RF), the digital core (VDD_DIG) and the digital pins (VDD_IO).

The requirements for these supplies are summarized in the table below.

Table 4.1. Power Supply Requirements

WF200 Pin Name	Min Voltage	Max Voltage	Typical Supply Current
VDD_PA	VDD_RF	3.6 V	~100 mA
VDD_RF	1.62 V	VDD_PA	~25 mA
VDD_DIG	1.62 V	3.6 V	~15 mA
VDD_IO	1.62 V	3.6 V	Upon SPI/SDIO frequency and load

Note: Although VDD_PA is variable, the maximum Tx power can be achieved only when VDD_PA is set to 3.0 V minimum.

There are no specific pin requirements on supplies sequencing except that all supply voltages should be settled at the rising edge of the RESETn pin, as shown in Figure 3.1 WF200 Power Up and Host Interface Timing Parameters on page 7.

5. Application Schematics Recommendations

5.1 Power Supplies

The WF200 has four supply pins, each one dedicated to a specific part: VDD_PA, VDD_RF, VDD_DIG, and VDD_IO. Each supply voltage can be set according to recommended operating conditions specified in datasheet. Depending on the design constraints and application targets (e.g., reduced BOM, maximum Tx power, host I/O voltage, power consumption), the application can use one to four supply sources.

The VDD_IO pin supplies the digital I/Os. This voltage has to be set to be compliant with the IC's WF200 interfaces, that is, with the host, a potential 2.4 GHz RF transceiver (PTA interface), and a potential Front-End Module (FEM). There are cases in which voltages must be different, and, in such cases, level shifters might be required. Considering the higher timing constraints on the host interface signals, it is preferred to set the VDD_IO voltage to be directly compliant with the host device and to use potential level shifters for FEM and PTA parts.

The VDD_DIG pin supplies the digital core through dedicated regulators. No impact from the voltage is expected on the device behavior, but a higher current consumption is expected when the voltage is 3.3 V. The current increase is minor in active mode, but it can be more significant when in sleep mode. Therefore, low-power applications would rather have a lower voltage on the VDD_DIG supply.

VDD_RF supplies the RF transceiver part. WF200 performance requires that the voltage be properly filtered.

VDD_PA supplies the Power Amplifier while in Tx mode. WF200 performance requires that the voltage be properly filtered.

Note:

- VDD_PA voltage should not be lower than VDD_RF.
- To minimize sleep mode current consumption, the number of pull-up resistors should be reduced as much as possible.

Each supply pin should have dedicated bypass capacitors for supply decoupling. To ensure optimal performance, VDD_RF and VDD_PA should also be correctly filtered, which may require using a series of ferrite beads or inductors for these supplies, if they are shared with other parts or supply pins. The “typical application schematics” section provides an example of supply schematics.

The recommended bypass filtering capacitors on the supply lines are as follows:

- VDD_PA: 12 pF; 47 nF; 10 µF X5R
- VDD_RF: 12 pF; 47 nF; 10 µF X5R
- VDD_DIG: 10 nF; 10 µF X5R
- VDD_IO: 100 nF; 10 µF X5R

It is recommended to select regulators that are:

- Stable with recommended ceramic capacitor values.
- Able to deliver 300 mA to supply enough current for the load peaks of the power amplifier.
- Able to react to load changes within 5 µs.

5.2 RF Part

This section provides details on the RF matching implementation utilized with the WF200 parts.

The 2.4 GHz RF front end has two unified, single-ended TX and RX pins (RF_1 and RF_2), so the TX and RX paths are tied together internally.

The on-chip part of the front end comprises a differential PA, a differential LNA, an integrated balun, and an RF T/R switch. The PA is biased through the VDD_PA pin. Externally, a single-ended matching network and harmonic filtering are required.

The first step of the matching design procedure is to determine the optimum termination impedance at the PA. The realized matching network should present this impedance for the PA at the RF pin if 50 Ω termination is applied at the antenna port. The optimum impedances are determined empirically by load pull methods. The RF_1 and RF_2 ports are similar, so the same optimum load impedance and, thus, the same matching network are applied at both RF ports.

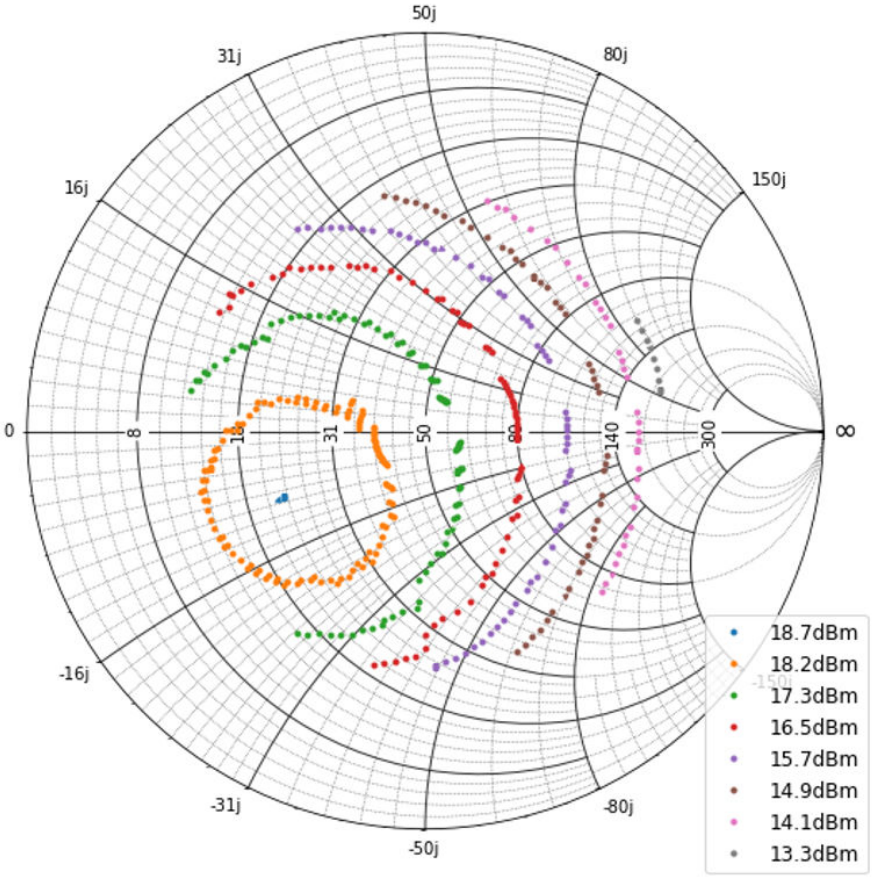


Figure 5.1. Load-Pull Curves and Optimum Termination Impedance at the RF Pin of WF200 (CW Peak Power Shown)

In real radio links, the TX power and the receiver sensitivity together (i.e., the link budget) determine the range. So, with the applied TX termination impedance, the impedance match in RX mode should be acceptable as well. In RX mode, the optimum termination impedance would be 50 Ω. Using the optimum load impedance instead, from the reflection coefficient and corresponding S11 calculations, the extra insertion loss is around 1 dB.

Silicon Labs reference designs utilize lumped elements in the RF matching network. At the operating frequency band of 2.4 GHz, the SMD components used and the PCB parasitic effects need to be taken into account during the matching network design. The SMD components at these high-frequency ranges rather behave as a resonator. A capacitor can be realized by a series RLC resonant circuit; meanwhile, an inductor's equivalent circuit represents a parallel RLC resonant circuit. Regarding the PCB parasitic effects, the series traces can be modeled as transmission lines with distributed L – C components and can have considerable parasitic inductance, while an SMD pad can behave as a parallel parasitic capacitance. The SMD components with different sizes have different parasitics, so it is also important to calculate with the appropriate values. Silicon Labs reference designs currently use SMD 0402 components. To reduce parasitic effects, it is recommended that the matching network be as close as possible to the RF_1 and RF_2 pins.

The recommended matching network for both RF ports is shown in the figure below. As can be observed, a three-element PI network is suggested considering 50 Ω antenna impedance within the Wi-Fi frequency band. The circuit provides the optimum impedance load for the WF200 part while ensuring sufficient harmonic suppression. The first shunt capacitor, C1, is tuned to self-resonance at the 4.8 GHz frequency band and thus provides enhanced attenuation at the second harmonic.

The matching circuit should show the `Zload_opt` impedance at the RF port of WF200 (RF port) while it is terminated by 50 Ω at its output (50 Ω ANT port). The impedance procedure is shown in Figure 5.5 3-Element PI Match for WF200 with SMD and Estimated PCB Parasitics on page 13, where the matching design is started from a termination impedance (ZL) which is the complex conjugate of the `Zload_opt` impedance. The reason is that the matching network will show the required `Zload_opt` impedance at its RF port, only if it is perfectly matched there to a termination which is the complex conjugate of the `Zload_opt` impedance.

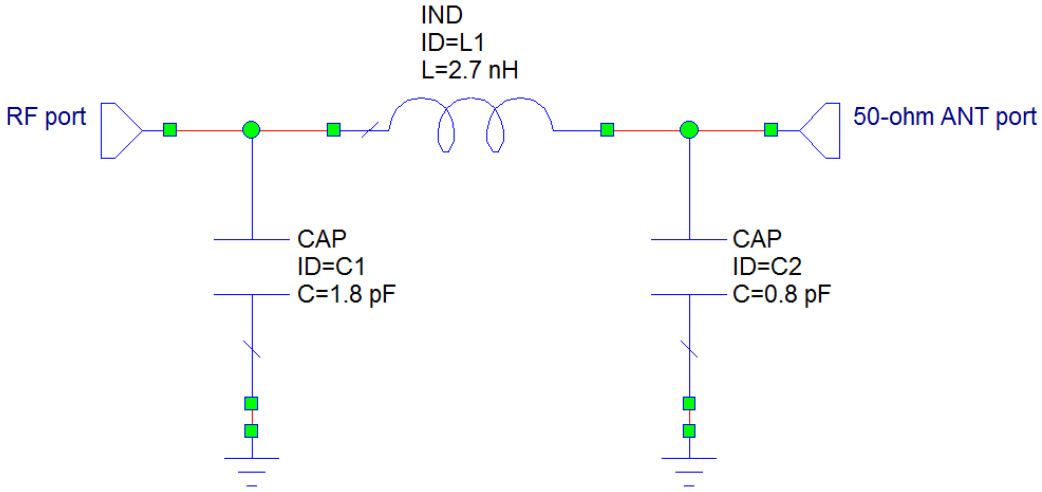


Figure 5.2. Recommended 0402 RF Match for WF200 Expansion Kit PCB

Matching circuit simulation example using discrete modelling from SMD manufacturers and PCB parasitics of WF200 Expansion Kit BRD8022A-A06 is detailed in the figures below.

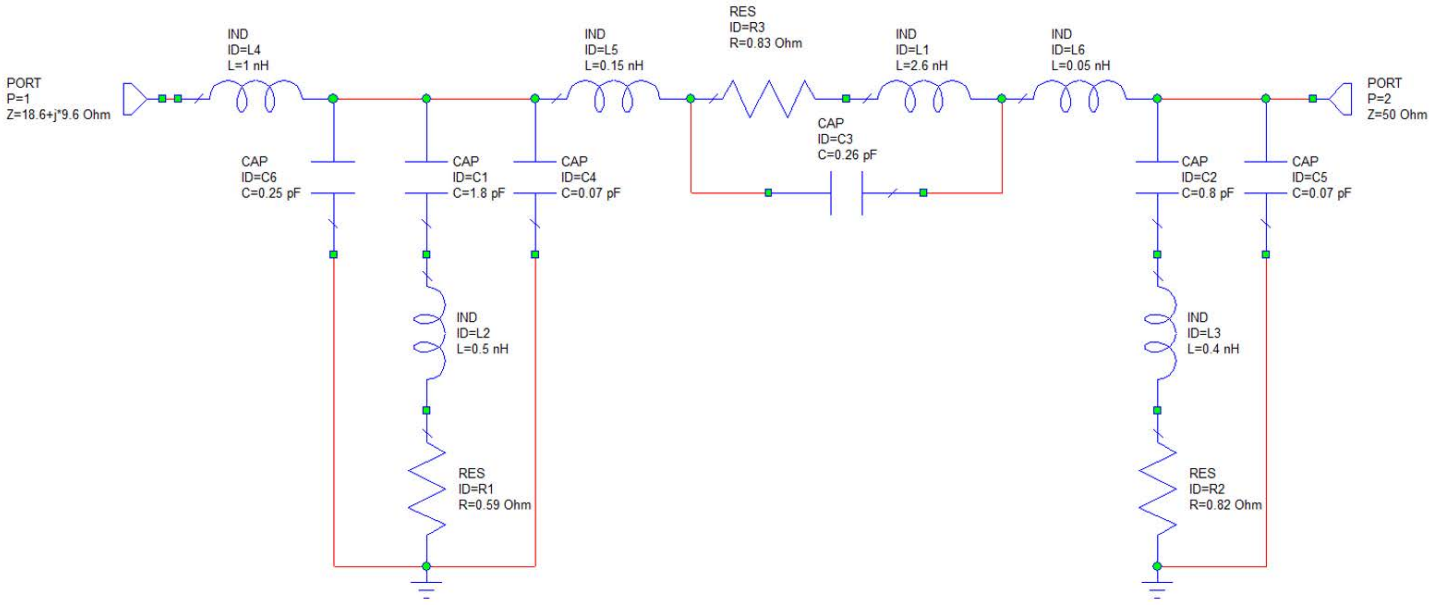


Figure 5.3. Discrete Schematic with 0402 SMD Models and Estimated PCB Parasitics

Port 1 (left-hand side-end) is the RF port/pin of the chip where the port impedance (*ZL*) should be set for the complex conjugate of optimum load impedance (*ZL=Zload_opt**), while the Port 2 (right end) is the 50 Ω antenna port.

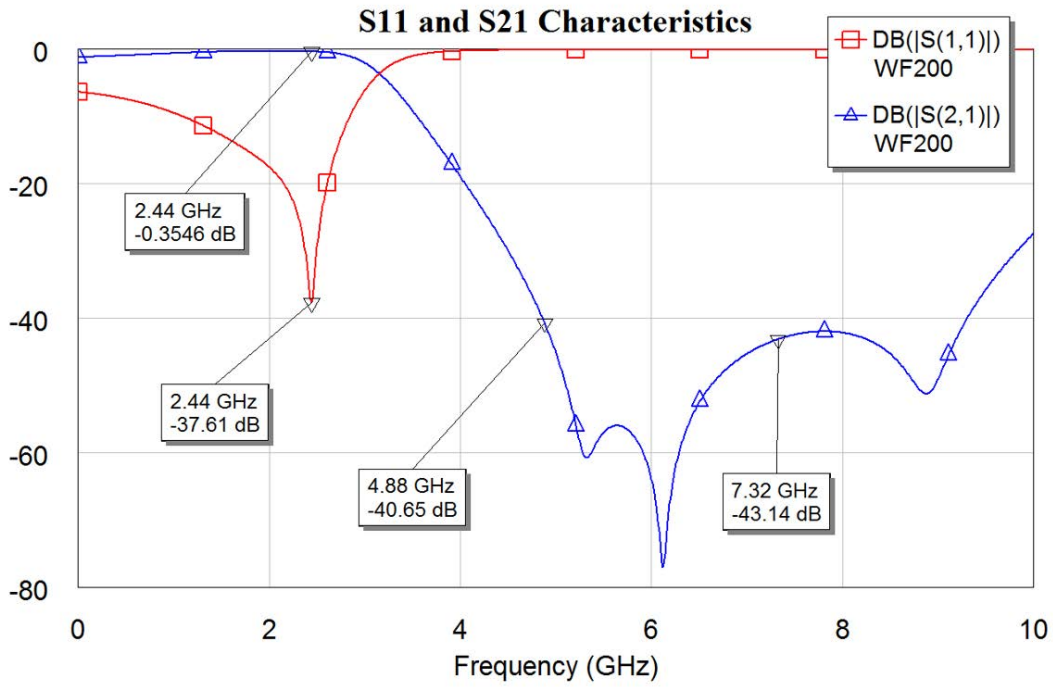


Figure 5.4. S11 and S21 Simulation Results

At 2.4 GHz, the parasitics of the SMD elements and the PCB layout have a major effect, so tuning of matching network values is required for any change compared to WF200 PCB layout and BOM.

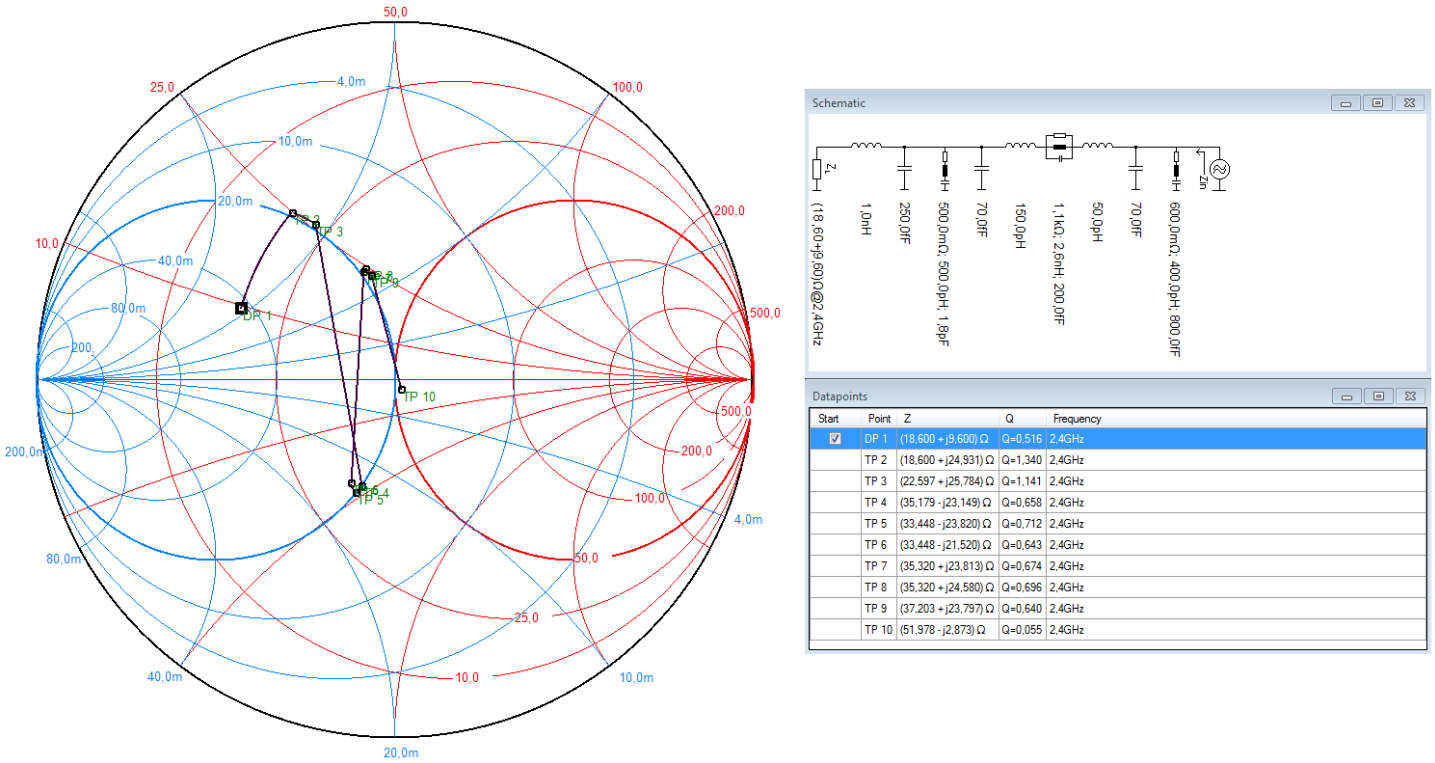


Figure 5.5. 3-Element PI Match for WF200 with SMD and Estimated PCB Parasitics

Table 5.1. SMD Details of the 0402 PI Match for WF200 Expansion Kit PCB

Schematic Reference Designator	Component Value	Tolerance	Part Number	Manufacturer
C1	1.8 pF	± 0.05 pF	GRM1555C1H1R8WA01	Murata
L1	2.7 nH	± 0.2 nH	LQW15AN2N7C00	Murata
C2	0.8 pF	± 0.1 pF	GJM1555C1HR80BB01	Murata

In order to keep the EVM performance, the return loss requirement at the ANT port is recommended to be: RL > 10 dB in the frequency range of 2.412 – 2.472 GHz under any conditions, e.g., with taking into account the technical spreading as well. With VSWR 2:1, 3:1, or even higher, it is recommended to apply TX gain backoff in order to maintain passing modulation parameters as detailed in Tables 5.2 and 5.3. Note, however, that the higher the VSWR, the higher the mismatch between antenna and RF port and the higher the sensitivity loss due to mismatch (typ. 0.5 dB loss for VSWR 2:1, 1.3 dB loss for VSWR 3:1).

Table 5.2. WF200 Recommended TX Backoff for 2:1 VSWR at RF Port

Recommended TX Backoff for 2:1 VSWR (Value in dB)						
Group of Modulations and Code Rates	FCC					ETSI/ Japan
	Channel Center Frequency (MHz)					
	2412	2417	2422 to 2452	2457	2462	2412 to 2472
MOD_GROUP_0 : B_1Mbps, B_2Mbps, B_5.5Mbps, B_11Mbps	2	2	2	2	2	2
MOD_GROUP_1 : G_6Mbps, G_9Mbps, G_12Mbps, N_MCS0, N_MCS1	6.75	2.5	2.5	3	7	2.5
MOD_GROUP_2 : G_18Mbps, G_24Mbps, N_MCS2, N_MCS3	5.75	2	2	2	6	2
MOD_GROUP_3 : G_36Mbps, G_48Mbps, N_MCS4, N_MCS5	4	2	2	2	4	2
MOD_GROUP_4 : G_54Mbps, N_MCS6	2.5	2.5	2.5	2.5	2.75	2.5
MOD_GROUP_5 : N_MCS7	3	3	3	3	3	3

Table 5.3. WF200 Recommended TX Backoff for 3:1 VSWR at RF Port

Recommended TX Backoff for 3:1 VSWR (Value in dB)						
Group of Modulations and Code Rates	FCC					ETSI/ Japan
	Channel Center Frequency (MHz)					
	2412	2417	2422 to 2452	2457	2462	2412 to 2472
MOD_GROUP_0 : B_1Mbps, B_2Mbps, B_5.5Mbps, B_11Mbps	3	3	3	3	3	3
MOD_GROUP_1 : G_6Mbps, G_9Mbps, G_12Mbps, N_MCS0, N_MCS1	7	3	2.5	3	7.5	2.5
MOD_GROUP_2 : G_18Mbps, G_24Mbps, N_MCS2, N_MCS3	6	2.5	2.5	2.5	6	2.5
MOD_GROUP_3 : G_36Mbps, G_48Mbps, N_MCS4, N_MCS5	4	3	3	3	4.5	3
MOD_GROUP_4 : G_54Mbps, N_MCS6	4	4	4	4	4	4
MOD_GROUP_5 : N_MCS7	5	5	5	5	5	5

The default recommended RF port for use is RF_1. If antenna diversity is not applied and only one RF port is being used, then the recommended termination of the unused RF port is 50 Ω.

Silicon Labs development kit utilizes a printed inverted-F antenna to provide a 50 Ω in/output. An inverted-F antenna can inherently be matched to 50 Ω without using any external tuning component. However, board size, plastic enclosures, metal shielding, and components in close proximity to the antenna can affect antenna performance. For best performance, the antenna might require tuning that can be realized in two ways:

- Dimensional changes in the antenna layout structure, or
- Application of external tuning components

The latter is typically the preferred solution when layout modification is not required on a custom design. To accomplish this, Silicon Labs generally recommends reserving SMD placeholders for external antenna tuning components, where the suggested external antenna matching structure is a three-element PI network. You can achieve a good match using a maximum of two elements (with one series and one shunt component) of the PI network. Any unknown passive impedance can get matched to 50 Ω on this PI network, since all L, C, L-C, C-L combinations can be realized on it, and, therefore, any detuning effect can be compensated for.

The figure below shows the recommended RF matching structure that contains of the 50 Ω matching of the WF200 device together with the separate antenna matching components. When both matching networks are located next to each other, the capacitors, C2 and C3, can be combined into one, and, thus, the network can be simplified down to five elements. C1, L1, and C2 should be located close to the WF200 RF output port. C3, L2, and C4 should be located close to the antenna input port.

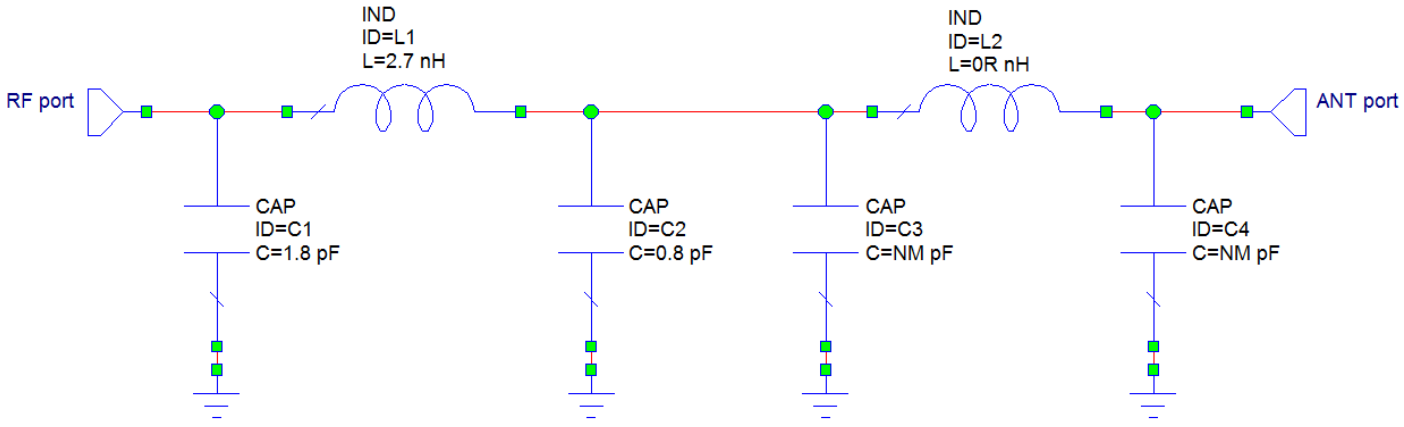


Figure 5.6. Recommended WF200 RF Match + Separate Antenna Match

For 0201 matching networks, refer to the table below. Note that it is recommended to add placeholders for the C-L H2 notch filter (located between the RF and antenna matching network). The purpose of this is to have flexibility to increase rejection at 4.8 GHz or 7.2 GHz if needed.

Table 5.4. SMD Details of the 0201 PI Match for WF200 Expansion Kit PCB

Schematic Reference Designator	Component Value	Tolerance	Part Number	Manufacturer
C1	2.3 pF	± 0.05 pF	GRM0335C1H2R3WA01	Murata
L1	2.9 nH	± 0.1 nH	LQP03HQ2N9B02	Murata
C2	1.5 pF	± 0.05 pF	GRM0335C1H1R5WA01	Murata

6. Typical Application Schematics

The following diagrams show simple applications using SDIO and SPI interfaces.

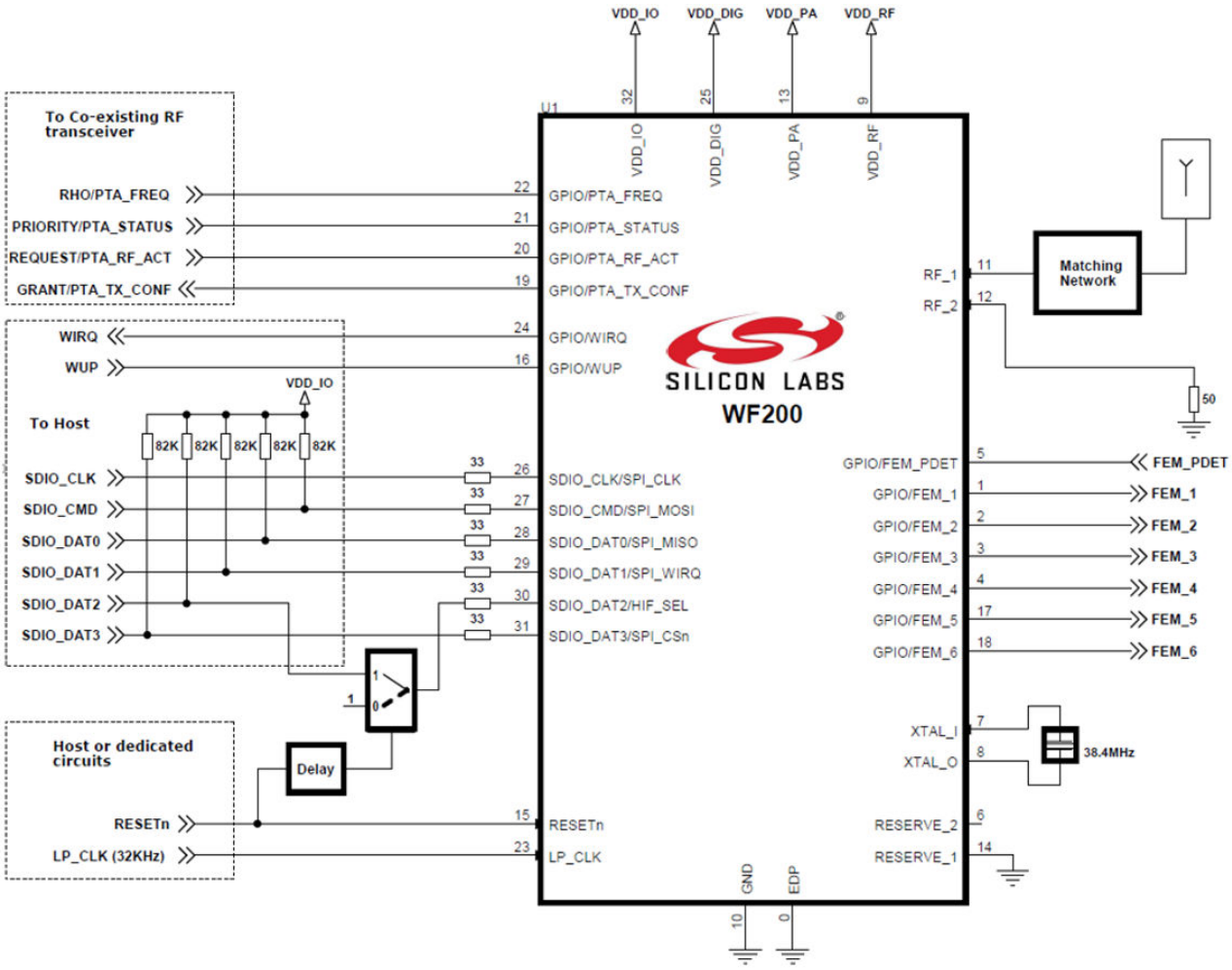


Figure 6.1. Application Using SDIO Interface

Note: Delay and switch can be removed when the host directly manages SDIO interface selection as detailed in Figure 3.1 WF200 Power Up and Host Interface Timing Parameters on page 7.

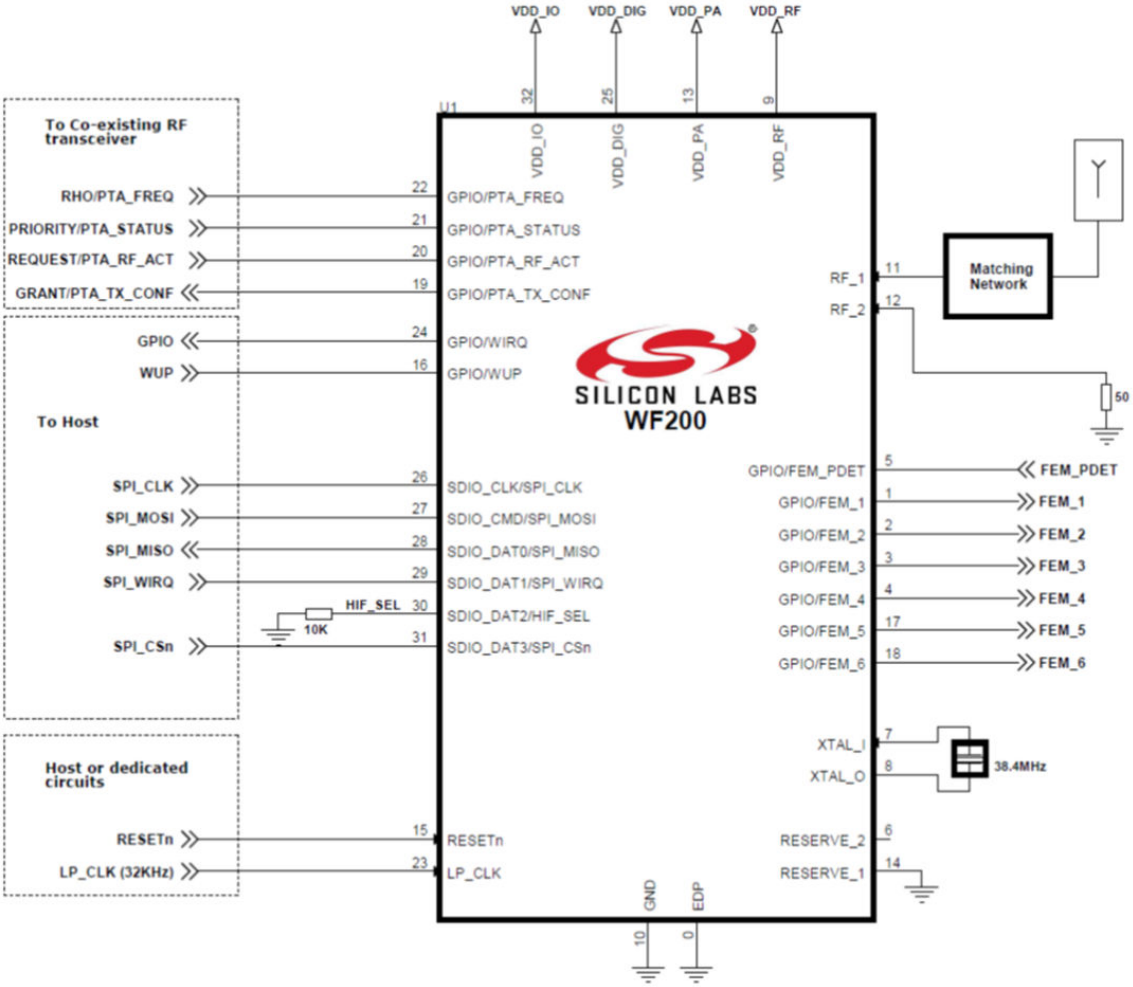


Figure 6.2. Application Using SPI Interface

Figure 6.3.

7. Layout Recommendations

The RF part of the Silicon Labs' development kit board is shown in the figure. Besides the schematic-level matching network and supply filtering considerations, the RF layout routing also has a strong influence on RF performance. Extensive testing has been completed using reference designs provided by Silicon Labs, so it is recommended that designers use the RF section of reference designs "as-is" since they minimize detuning effects caused by additional parasitics or generated by poor component placement and PCB routing. In case of any RF layout modification or change in PCB structure/material compared to development kit board BRD8022A, it is recommended to:

- Check 50 Ω impedance measured at the output of the RF matching network.
- Implement and tune the antenna matching network to get a 50 Ω impedance at the input of the matching network.

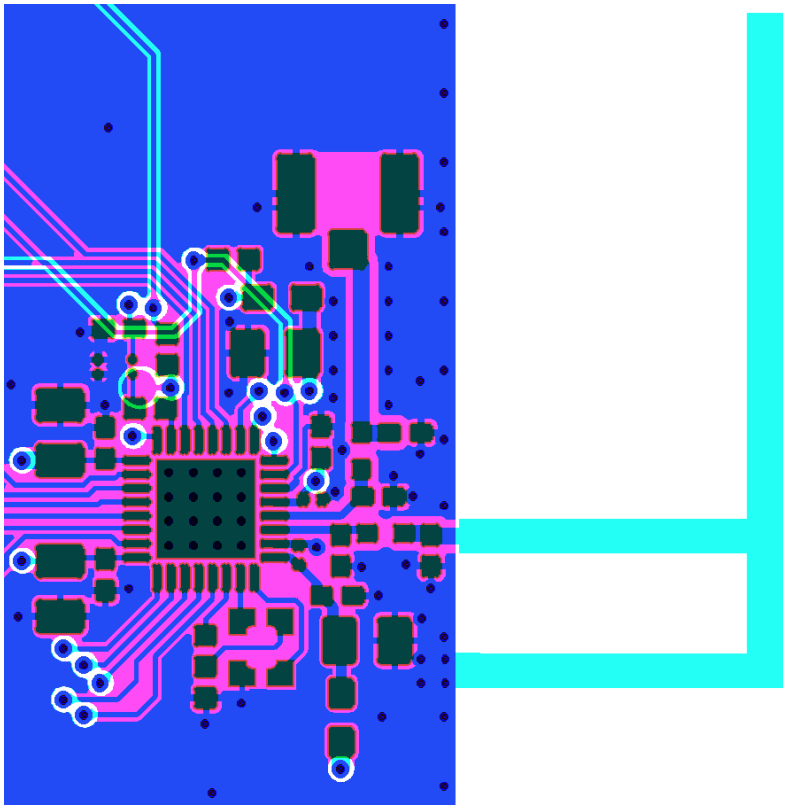


Figure 7.1. RF Section of the Development Kit Board Layout

7.1 Generic RF Layout Considerations

For custom designs, use the same PCB stackup as in the reference design whenever possible. Deviation from the reference PCB stackup can cause different PCB parasitic capacitances, which can detune the matching network from its optimal form. If a design with a different number of layers than the reference design is necessary, make sure that the distance between the top layer and the first inner layer is similar to that found in the reference design, because this distance determines the parasitic capacitance value to ground. Otherwise, detuning of the matching network is possible, and fine tuning of the component values may be required. The Silicon Labs development kit uses a 1.6 mm thick FR4 PCB with the following board stack-up.

Figure 7.2. Reference Design PCB Specification

Use as much continuous and unified ground plane metallization as possible, especially on the top and bottom layers.

Avoid the separation of the ground plane metallization, especially between the ground of the matching network and the WF200 GND pins and exposed pad.

Use as many ground stitching vias, especially near the GND pins, as possible to minimize series parasitic inductance between the ground pours of different layers and between the GND pins.

Use a series of GND stitching vias along the PCB edges and internal GND metal pouring edges. The maximum distance between the vias should be less than lambda/10 of the 10th harmonic (the typical distance between vias on reference radio boards is 2 mm). This distance is required to reduce the PCB radiation at higher harmonics caused by the fringing field of these edges.

The exposed pad footprint for the paddle of the WF200 device should use as many vias as possible to ensure good grounding and heat sink capability. In the reference designs there are 16 vias (4x4 via grid), each with 0.5 mm diameter.

For designs with more than two layers, it is recommended to put as many traces (even the digital traces) as possible in an inner layer and ensure large, continuous GND pours on the top and bottom layers, while keeping the GND pour metallization unbroken beneath the RF areas (between the antenna, matching network and RF chip).

Avoid using long and/or thin transmission lines to connect the RF related components. Otherwise, due to their distributed parasitic inductance, some detuning effects can occur. Also shorten the interconnection lines as much as possible to reduce the parallel parasitic caps to the ground. However, couplings between neighbor discretes may increase in this way.

Route traces (especially the supply and digital lines) on inner layers for boards with more than two layers.

To achieve good RF ground on the layout, it is recommended that one add large, continuous GND metallization on the top layer in the area of the RF section (at a minimum). Better performance may be obtained if this is applied to the entire PCB. To provide a good RF ground, the RF voltage potentials should be equal along the entire GND area as this helps maintain good VDD filtering. Gaps should ideally be filled with GND metal and the resulting sections on the top and bottom layers should be connected with as many vias as possible. The reason for not using vias on the entire GND section is due to the restrictions of the actual radio board design. These restrictions include traces routed on other layers or components on the bottom side.

To reduce the coupling between the nearby discrete inductors, avoid placing them in the same orientation.

Use tapered line between transmission lines with different width (i.e., different impedance) to reduce internal reflections.

Avoid using loops and long wires to obviate their resonances. They also work well as unwanted radiators, especially at the harmonics.

Using silkscreen near the antenna could slightly affect the dielectric environment of the antenna. Although this effect is usually negligible, if possible, try to avoid using silkscreen on the antenna or on the antenna copper pour keep out areas.

Avoid routing GPIO lines close or beneath the RF lines, antenna or crystal, or in parallel with a crystal signal. Use the lowest slew rate possible on GPIO lines to decrease crosstalk to RF or crystal signals.

Use as many parallel grounding vias at the GND metal edges as possible, especially at the edge of the PCB and along the VDD trace, to reduce their harmonic radiation caused by the fringing field.

7.2 RF Matching Network

The RF matching components should be placed as close as possible to the RF pin of the WF200 part to reduce the series parasitic inductance and avoid any detuning effects.

The neighboring matching network components should be placed as close to each other as possible to minimize any PCB parasitic capacitance to the ground and the series parasitic inductances between the components.

Traces near the GND pins of the capacitors should be thickened to improve the grounding effect in the thermal straps. This minimizes series parasitic inductances between the ground pour and the GND pins. Additional vias placed close to the GND pins of capacitors connect them to the inner/bottom layer GND plane and serve to further reduce these effects. To reduce the parasitic inductance of GND vias, these vias will be flooded on the Top layer.

Couplings through the ground can occur between nearby filtering capacitors (especially at high harmonics) and decrease the effectiveness of low-pass filtering, causing higher conducted and radiated harmonics. To avoid possible high harmonic levels, it is recommended that one connect the nearby harmonic filtering capacitors to ground planes on different sides of the transmission line.

The area beneath the RF chip and the matching network (on the first inner layer) should be filled with continuous ground metal as it will show good ground reference for the matching network and will ensure a good, low-impedance return path to the RF chip's ground as well. Board routing and wiring should not be placed in this region to prevent coupling effects with the matching network. It is also recommended that the GND return path between the GND vias of the matching network and the GND vias of the RFIC paddle should not be blocked in any way; the return currents should see a clear, unhindered pathway through the GND plane to the back of the RFIC.

If necessary, a shielding cap can be used to shield the harmonic radiation of the PCB; in that case, the shielding cap should cover all of the RF-related components (excluding the antenna).

To reduce sensitivity to PCB thickness variations, use 50 Ω grounded coplanar lines where possible to connect the antenna or the U.FL connector to the matching network. This also reduces radiation and coupling effects. A general rule is to use 50 Ω transmission lines where the length of the RF trace is longer than λ/16 at the fundamental frequency.

Use many GND vias near the coplanar lines in order to minimize radiation.

The interconnections between elements are not considered transmission lines since their lengths are much shorter than the wavelength, and, thus, their impedances are not critical. As a result, their recommended width is equal to the width of the pad of the applied components. In this way, reflections at pad-trace transitions can be prevented, and parasitic capacitances to ground can be minimized.

7.3 Antenna

To minimize 50 Ω detuning and degradation of the radiation pattern, reduce as much as possible any shielding of the inverted F antenna. The ground plane forms an important part of the antenna as there is significant current running along the ground plane. When using an inverted F antenna, ensure that the PCB size is at least 25.4 mm in width.

For other antenna designs, follow the ground plane size and layout requirements specified by the antenna provider.

To ensure that the main TX requirements, such as Error Vector Magnitude, Out of Band, and Spectral Emissions Mask, are met, optimization of antenna matching network should be performed on the final product as any plastic or casing can alter the antenna impedance.

7.4 Crystals

Place the high-frequency (MHz-ranged) crystal as close to the WF200 part as possible. External crystal load capacitors are not needed since there is an on-chip capacitance bank for this purpose. Thus, it is advisable to select crystals with load capacitance requirements that can be supported by the WF200 part. This way, the crystal can be placed close to the chip pins, and external capacitors are not needed.

Connect the crystal case to the ground using many vias to avoid radiation of the ungrounded parts. Do not leave any metal unconnected and floating that may become an unwanted radiator. Avoid leading supply traces close or beneath the crystal or parallel with a crystal signal or clock trace.

If possible, use an isolating ground metal between the crystal and VDD traces to avoid any detuning effects on the crystal caused by the nearby power supply and to avoid leakage of the crystal/clock signal and its harmonics to the supply lines.

Route traces between crystal and XTALI/XTAL_O pins as differential signals to minimize the area of the trace loop.

7.5 Power Supplies

Always ensure good VDD filtering by using some bypass capacitors (especially at the range of the operating frequency). The series self-resonance of the capacitor should be close to the filtered frequency. The bypass capacitor that filters the highest frequency should be placed closest to the VDD pins of the WF200 (i.e., place the pF-ranged capacitors first and closer to the chip supply pin). In addition to the fundamental frequency, the crystal/clock frequency and its harmonics (up to the third harmonic) should be filtered to avoid up-converted spurs.

To ensure good ground connection, all VDD filtering capacitors should use many vias close to their ground pins. It is also recommended that the GND return path between the GND vias of the VDD filtering capacitors and the GND vias of the RFIC paddle should not be blocked in any way; return currents should have a clear and unhindered pathway through the GND plane to the back of the RFIC.

Bypass capacitors should be placed as close as possible to the WF200 supply pins and should have short connections to ground. In case the power supply trace is coming from another PCB layer, it is recommended that the bypass capacitor be located between the via and the supply pin, i.e., the order of the filtering is: supply pin to bypass capacitors to via and routing.

Use VDD traces that are as short as possible. The VDD trace can be a hidden, unwanted radiator, so it is important to simplify the VDD routing as much as possible and use large, continuous GND pours with many stitching vias. To achieve the simplified VDD routing, try to avoid star topology of the VDD traces (i.e., avoid connecting all VDD traces in one common point).

Avoid placing the supply lines close to the PCB edge.

For designs with more than two layers, use inner the layer to route the power supply. On this inner layer, use wide VDD sub-plane and traces to increase parasitic decoupling capacitance with nearby ground layers.

Place the RF related parts (especially the antenna) far away from the dc-dc converter output and the related dc-dc components, if some is applied on the RF board.

7.6 Host Interface

To reduce radiated coupling of the SDIO/SPI bus, it is recommended that the CLK and DAT traces be surrounded by two GND traces.

7.7 Summary on Routing Suggestions

The ideal layer consistency for PCBs with more than two layers is as follows:

Top layer: Use as much continuous solid GND metallization as possible with many stitching vias.

First inner layer: Use continuous, unified GND metallization beneath the RF part; traces can be routed beneath the non-RF parts if necessary.

Widen, as much as possible, the supply sub-planes and traces.

Surround the SDIO/SPI clock trace with two GND traces and also the entire bus with two GND traces.

All other inner layers: Route as many (supply and digital) traces on these layers as possible. Widen supply sub-planes and traces as much as possible. Surround SDIO/SPI clock trace by two GND traces and also the entire bus with two GND traces.

Bottom layer: This layer should be unified GND metal; route traces on this layer only if necessary.

8. Package Outline

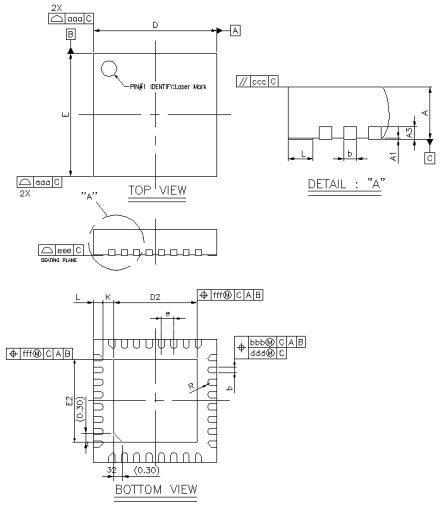


Figure 8.1. WF200 Package Outline

Dimension	Min	Nom	Max
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A3		0.20 REF	
b	0.15	0.20	0.25
D	3.90	4.00	4.10
E	3.90	4.00	4.10
D2	2.60	2.70	2.80
E2	2.60	2.70	2.80
e		0.40 BSC	
L	0.20	0.30	0.40
K	0.20	—	—
R	0.075	—	0.125
aaa		0.10	
bbb		0.07	
ccc		0.10	
ddd		0.05	
eee		0.08	
fff		0.10	

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-220, Variation VKKD-4.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

9. Recommended PCB Land Pattern

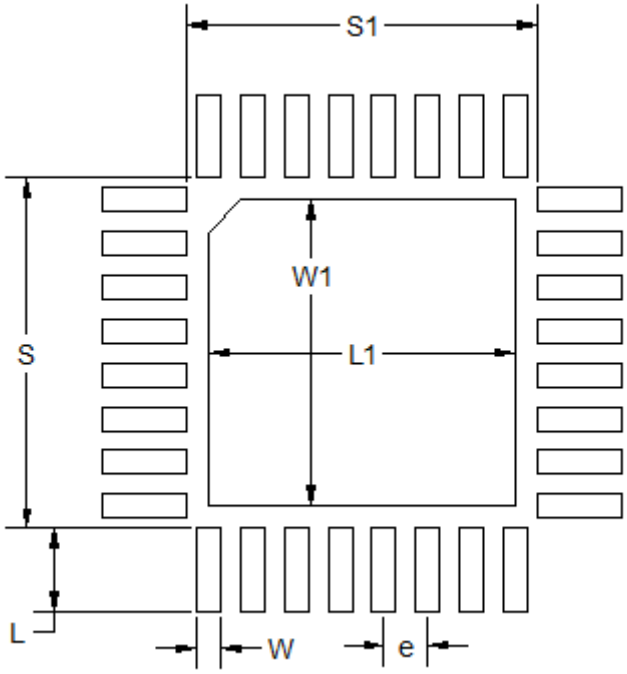
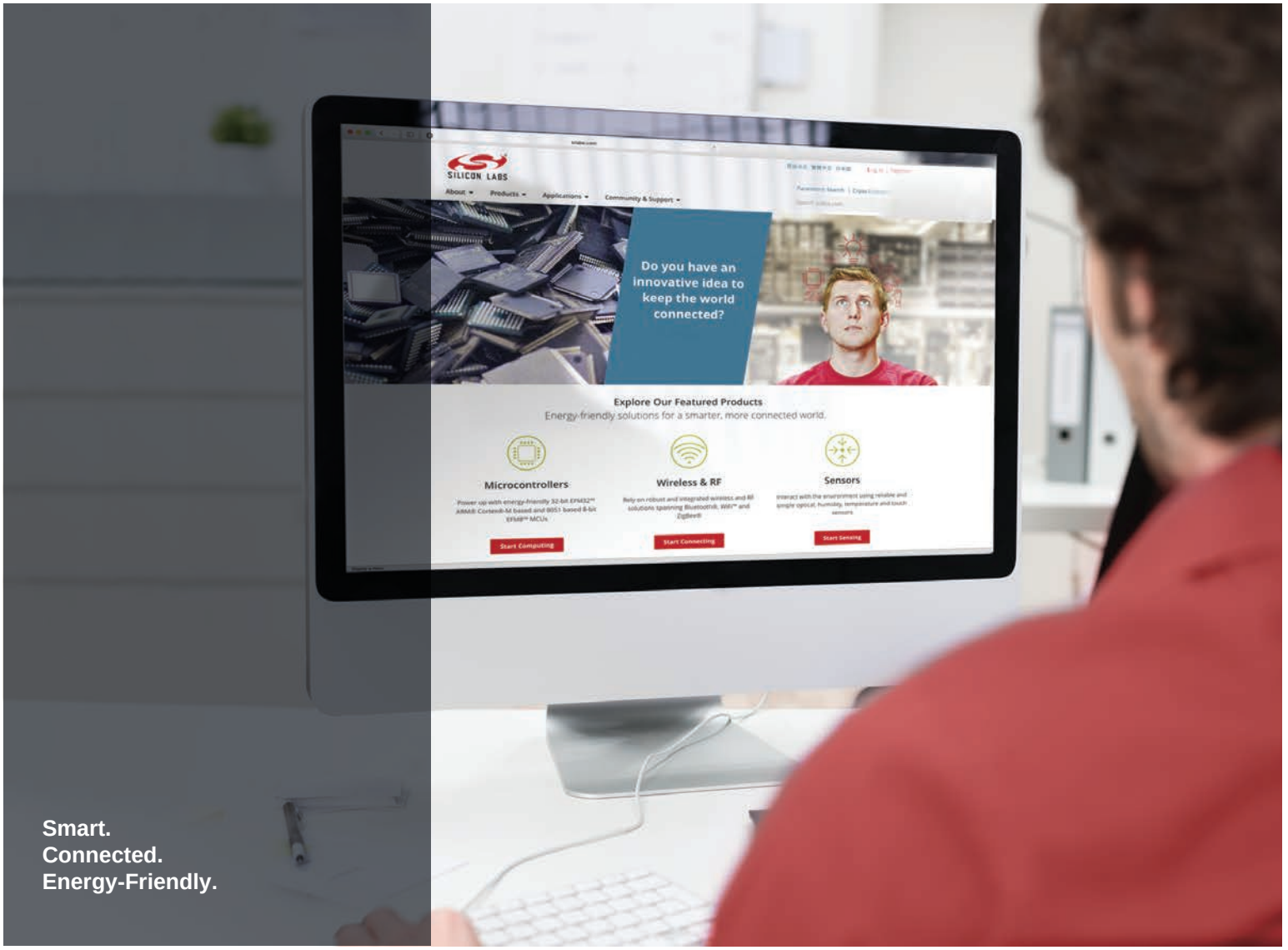


Figure 9.1. Recommended PCB Land Pattern

Dimension	mm
L	0.76
W	0.22
e	0.40
S	3.21
S1	3.21
L1	2.80
W1	2.80



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