## Clock Division with Jitter and Phase Noise Measurements

### Introduction

As clock speeds and communication channels run at ever higher frequencies, accurate jitter and phase noise measurements become more important, even as they become more difficult and expensive to manage. While measuring ultra low-jitter devices and equipment, the engineer is continually required to ask whether the measurement values are the result of the device under test (DUT) or if they are due to the equipment being used. The engineer is also constantly looking for methods of expanding the reach of the equipment at hand. Here are some practical pointers and observations to assist in situations where clock signals have been divided down from higher frequency voltage-controlled oscillators (VCOs).

### Time vs. Frequency Domain

Most modern equipment that measures jitter can be placed into one of two broad categories: time domain and frequency domain. Time domain equipment typically comes in the form of a high-speed digital oscilloscope with high single-shot sampling bandwidth. Frequency domain equipment usually comes in the form of a spectrum analyzer, a spectrum analyzer with phase noise measurement capability or a phase noise analyzer. Each of these two categories of equipment has its own set of advantages and disadvantages. However, it should be remembered that they are measuring the same phenomena, albeit with a different approach. Let's take a closer look at the key differentiating characteristics of these two approaches to measuring jitter:

As shown in Figure 1, peak cycle-to-cycle jitter is the maximum difference between consecutive, adjacent clock periods measured over a fixed number of cycles, typically 1k or 10k. It is used whenever there is a need to limit the size of a sudden jump in frequency. For example, when driving a PLL, it may be desirable to limit the size of an instantaneous change in frequency to ensure that downstream PLLs remain in lock.
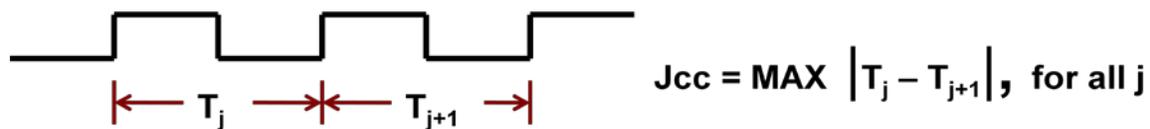


$$Jcc = MAX \left| T_j - T_{j+1} \right|, \text{ for all } j$$

**Figure 1: Cycle-to-Cycle Jitter**

As shown in Figure 2, peak-to-peak period jitter is the difference between the largest clock period and the smallest clock period for all individual clock periods within an observation window (typically 1k or 10k cycles). It is a very useful specification for guaranteeing the setup and hold time of flip flops in digital systems. The term peak-to-peak is defined to be the difference between the smallest and the largest period value sampled during a measurement.

$$Jper = MAX(T_i) - MIN(T_j), \text{ for all } i, j$$
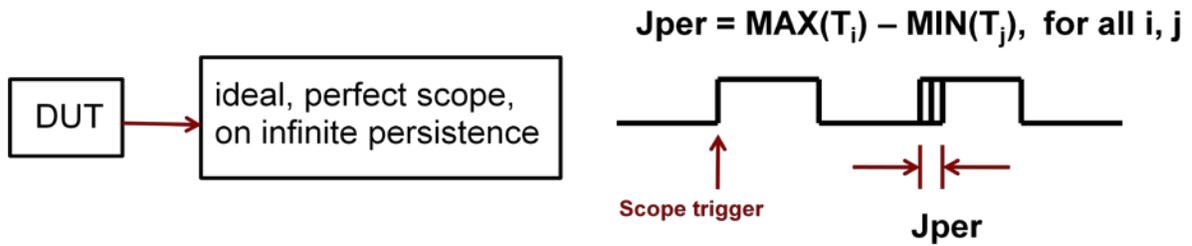
**Figure 2: Period Jitter**

As shown in Figure 3, time interval error (TIE) jitter is also known as accumulated jitter and phase jitter. It is the actual deviation from the ideal clock period over all clock periods. It includes jitter at all jitter modulation frequencies and is commonly used in wide area network timing applications, such as SONET, Synchronous Ethernet and Optical Transport Networking (OTN).
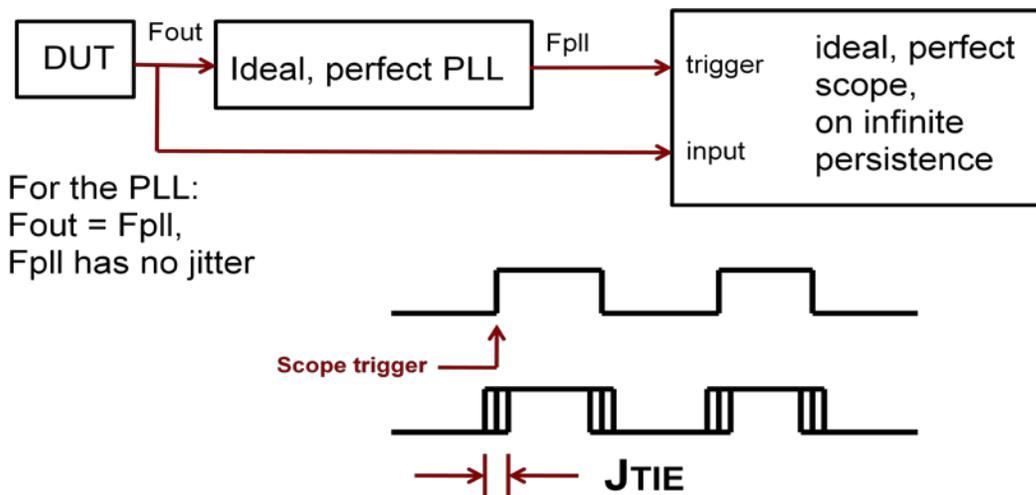


**Figure 3: TIE Jitter**

Note that different statistics can be taken for all types of jitter. That is, root means squared (RMS), peak-to-peak and other statistical values exist for cycle-to-cycle, period and TIE jitter, although some are in more common use than others. Whenever peak-to-peak statistics are used, the number of samples taken needs to be large enough to have confidence in the measurement. Typically, such sample sizes range from 1000 to 10,000.

Time domain equipment has the virtue of being able to directly measure peak-to-peak, cycle-to-cycle, period and TIE jitter. This measurement approach permits the measurement of jitter for very low frequency clock (or carrier) signals. By post-processing the data with techniques such as FFTs and digital filters, it is possible to integrate the phase noise value over a specific band of frequencies to generate RMS phase jitter values. Another key point is that time domain equipment is much better at measuring data-dependent jitter, which makes it very useful for high-speed serial links that use serializer/deserializer (SERDES) technology.

Frequency domain equipment cannot directly measure peak-to-peak, cycle-to-cycle or period jitter, as its native capability is to measure the RMS power of signal in a given frequency band. Frequency domain equipment is also awkward for measuring data dependent jitter. However, the best frequency domain instruments have a lower noise floor than the best time domain instruments. This fact makes frequency domain equipment the instruments of choice for ultra-low phase noise clock signal measurements that are free of data-dependent jitter. Table 1 summarizes the differences between time and frequency domain instruments:

**Table 1: Time vs. Frequency Domain Instrument Differences**

|  | Time Domain | Frequency Domain |
|---|---|---|
| **Native Measurements** | Peak-Peak Jitter | RMS Phase Jitter |
|  | Cycle-to-Cycle Jitter | Phase Noise |
|  | Period Jitter | Jitter Frequency Information |
| **Advantages** | Good with Low-Frequency Clocks | Lower Noise Floor |
|  | Good with Data-Dependent Jitter | Easy Detection of Spurs vs. Random Jitter |

Because we are focusing on the measurement of low-jitter clock signals, there is no need to further discuss  time domain equipment other than to say that various mathematical estimation and translation approaches can be used to go from one type of jitter measurement to another. For example, it is possible to use a crest factor and a desired bit error rate (BER) to go back and forth between peak-to-peak and RMS jitter. Another example is using a Fast Fourier Transform (FFT) of time domain data to provide frequency domain information and filtering. However, it should be remembered that most of these techniques rely on mathematical models that, though they may be good approximations in most situations, have their limitations and should only be utilized with care and thought.

One particular issue that bears further investigation is the effect of clock (or carrier) frequency on the jitter measurement. It is intuitive that a clock signal that is divided down by an ideal divider will have the same clock edge jitter after the divider as before the divider. This is depicted in Figure 4 where the top jittered signal with frequency Fo is divided by two using a perfect divider to produce a clock frequency of Fo/2. Both clock signals have the same jitter, Jo. Note that the jitter energy of the lower clock signal is half that of the higher clock signal because there are half as many edges in a given interval of time.
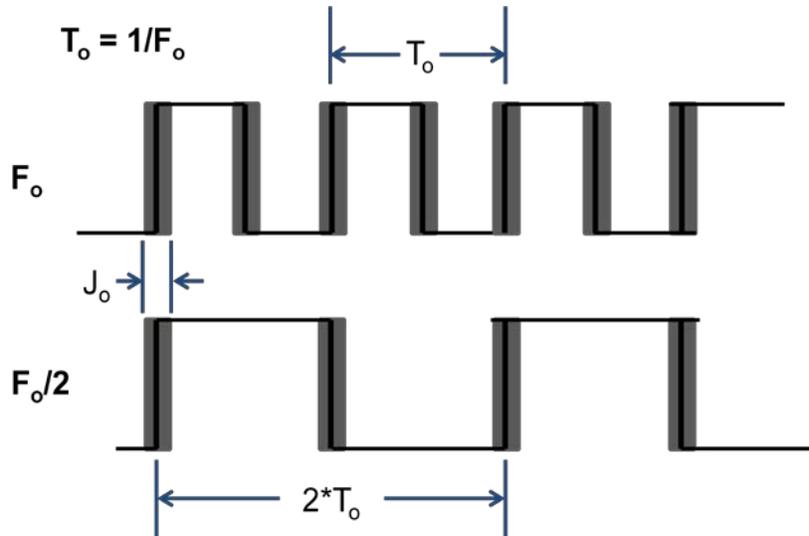
**Figure 4: Division by Two**

The intuition that Jo (as defined in Figure 4) is same for the two clock signals is for the most part true despite the fact that the phase noise of a clock signal that is divided by two will be 6dB lower than the phase noise of the original clock signal. Note for division by two, 6dB = 20*log2 (see Footnote 2.)

The following example illustrates the effect of division by powers of two for both phase noise and jitter. These measurements were performed on a Silicon Labs Si5324 phase locked loop (PLL) device, which has the internal structure described in Figure 5.
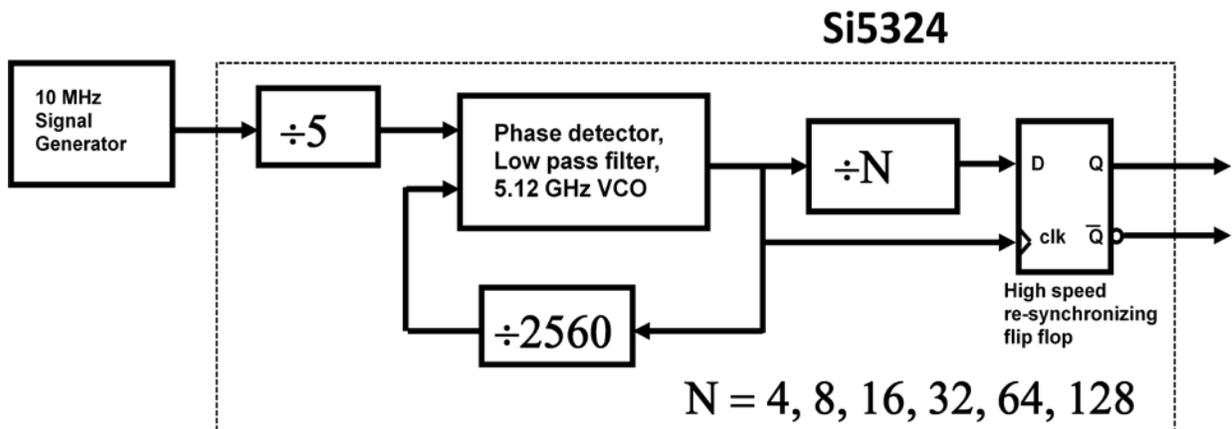


**Figure 5: Si5324 Clock IC Internal Structure**

Note that the output clock is resynchronized by the high-speed VCO, regardless of the final output frequency. This means that the edge shape and placement should be the same for all possible divider values, with the only difference being that there are fewer clock edges during a given time interval.  Though there will be some re-timing noise, it will be the same for all of the different divisor values.
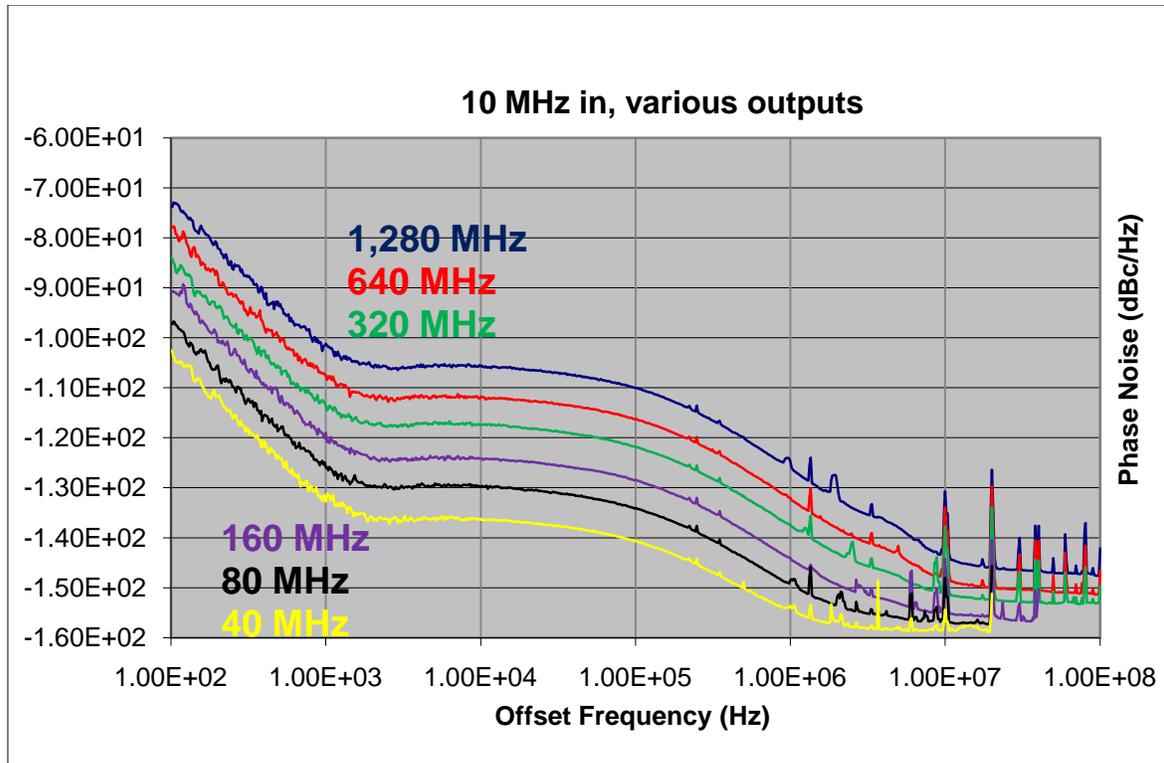
**Figure 6: Phase Noise Plots for Different Divisor Values**

The six curves are essentially the same but with a vertical separation of 6 dBc/Hz. The 6dB separation is relatively constant over all offset frequencies and divisor values with one or two exceptions. On the right-hand edge side of the plot where the offset from the clock (carrier) is at its largest, the relative vertical offsets between the curves are compressed. On the right-hand side of the plot, the compression increases as the clock frequency is reduced. This compression becomes more pronounced as the clock frequency decreases and as the phase noise curve values become lower. The compression occurs because the noise floor of the Agilent model E5052B Signal Source Analyzer is getting close in value to the phase noise (jitter generation) of the Si5324 IC. Note that the noise floor is only an issue because of the combined effect of the ultra-low jitter of the Si5324 and the low carrier frequency.

Table 2 lists the corresponding jitter values for each of the six plots with the jitter integrated from 100 Hz to 20 MHz and all jitter values in femtoseconds RMS.

**Table 2: RMS Jitter Values for Different Values of Division**

| Color | Divisor | Output Frequency (MHz) | Jitter, fsec RMS |
|---|---|---|---|
| Blue | 4 | 1,280 | 441 |
| Red | 8 | 640 | 447 |
| Green | 16 | 320 | 461 |
| Purple | 32 | 160 | 463 |
| Black | 64 | 80 | 477 |
| Yellow | 128 | 40 | 523 |

Starting at the top of Table 2, notice that the jitter increases slightly as the output frequency decreases. This is evidence that the output jitter is relatively constant despite the fact that the phase noise curves are separated from one another by 6 dB. The rate at which the jitter increases becomes more pronounced at the lowest output frequencies. Let's examine the two sources of the increased RMS phase noise values: instrument noise floor and aliasing.
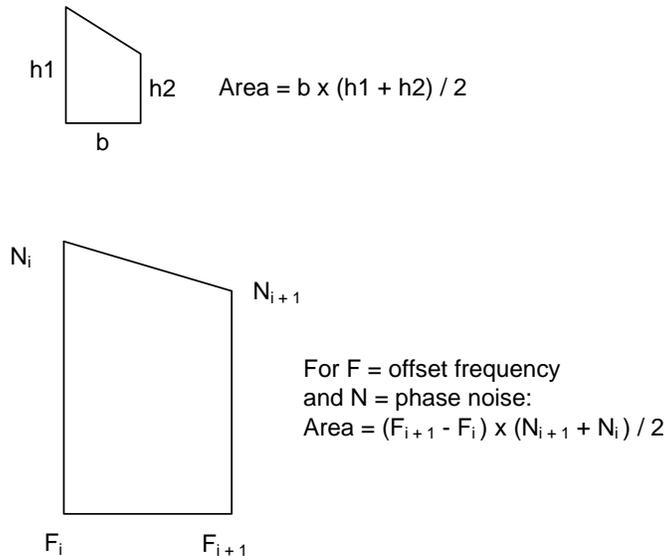
**Instrument Noise Floor and Phase Noise Integration**

As mentioned earlier, when measuring the phase noise of very low-jitter clocks at low clock frequencies, the instrument noise floor can become the limiting factor of a measurement. At some point, you are measuring your equipment, not the device under test. Even though the phase noise curves are all getting monotonically smaller as the clock frequency decreases, the RMS edge jitter remains almost constant because the phase noise integration process uses the clock period to scale the RMS jitter values.

To illustrate how this occurs, let's look at the process of phase noise integration to produce an RMS jitter value. Most modern phase noise equipment produces a file that that has two columns (typically a .CSV file). One of the two columns gives the frequency offset from the clock (or carrier) frequency in Hertz. The other column gives the phase noise values at that offset frequency in dBc/Hz. In this manner, the two columns contain data point pairs that describe the phase noise at a given offset from the clock frequency. The process of integration involves summing up the area under the curve for all of the frequency offset points after converting the dBc/Hz values to linear values in the following manner:

$$\text{Linear Values} = 10^{(\text{dBc/Hz})/10}$$

The formula for the area of a trapezoid shown in Figure 7 is used to find the area described by two adjacent data point pairs:



$$\text{Area} = b \times (h1 + h2) / 2$$

For F = offset frequency
and N = phase noise:
$$\text{Area} = (F_{i+1} - F_i) \times (N_{i+1} + N_i) / 2$$

**Figure 7: Trapezoidal Integration**

The area under the entire curve is then found by summing up the area of all of the trapezoids. The final RMS jitter value is determined by scaling the result by two factors: The value √2 comes from the fact that the data was taken as single side band; however, the RMS jitter is assumed to be dual side band. The assumption that the two side bands of the phase noise are symmetric about the clock frequency is usually a safe one. In this case it is even more justified because the limiting amp shown in Figure 8 will suppress amplitude  modulation (AM) and pass frequency modulation (FM) to ensure symmetric side bands.

The other scaling factor converts the area sum so that it is no longer expressed as a unit interval (UI) but in units of time. This factor keeps the RMS edge jitter values relatively constant while the phase noise values change.

$$\frac{\sqrt{2}}{2\pi F_c} \sum_i \frac{(F_{i+1} - F_i) \times \left( 10^{\frac{(N_i+1)}{10}} + 10^{\frac{N_i}{10}} \right)}{2}$$

Where:

$F_c$ = Clock Frequency

$N_i$ = Phase Noise in dBc/Hz, for the ith entry

$F_i$ = Offset Frequency, for the ith entry

**Aliasing**

The other cause of increasing RMS jitter values with decreasing clock frequency is aliasing. For every division of two, the upper half of a phase noise plot is aliased down into the new lower clock frequency phase plot. Since phase noise is usually higher close to the clock (carrier) frequency and drops off as the offset from the clock frequency increases, the amount of phase noise that is being aliased down is usually relatively small. However, when dividing by large numbers, the effect becomes cumulative and significant. Referring back to Figure 1, the difference between the 1280 MHz and the 640 MHz curves is a constant 6 dB across the entire plot. As a result, one would expect that the increased RMS jitter values for the two curves shown in Table 2 are due entirely to alias and not to the instrument noise floor.

The following spectra and phase noise plots illustrate aliasing. Note that the signals in this example use AM and are not what would be expected in a typical application. Rather, as the block diagram in Figure 8 indicates, they are used here to specifically illustrate this phenomenon.
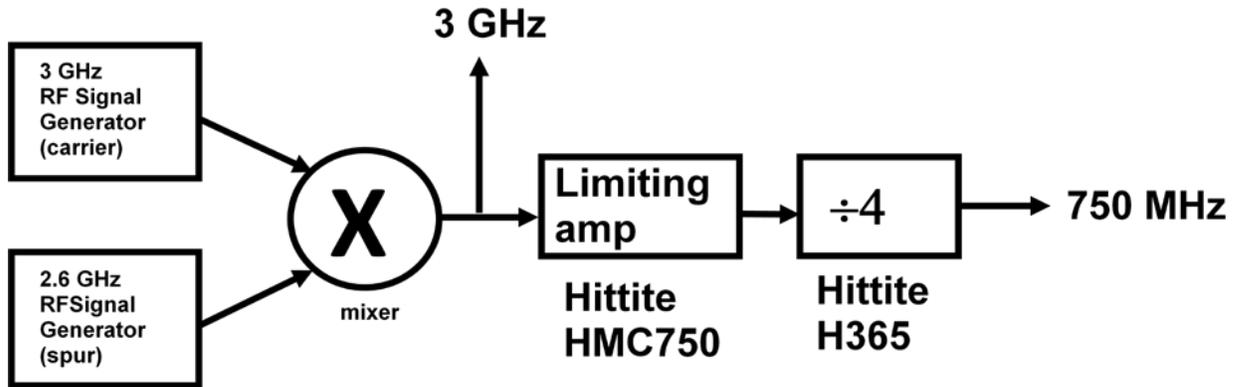
**Figure 8: Aliasing Test Diagram**

The spectra and phase noise plots for the 3 GHz signal are shown Figures 9 and 10:
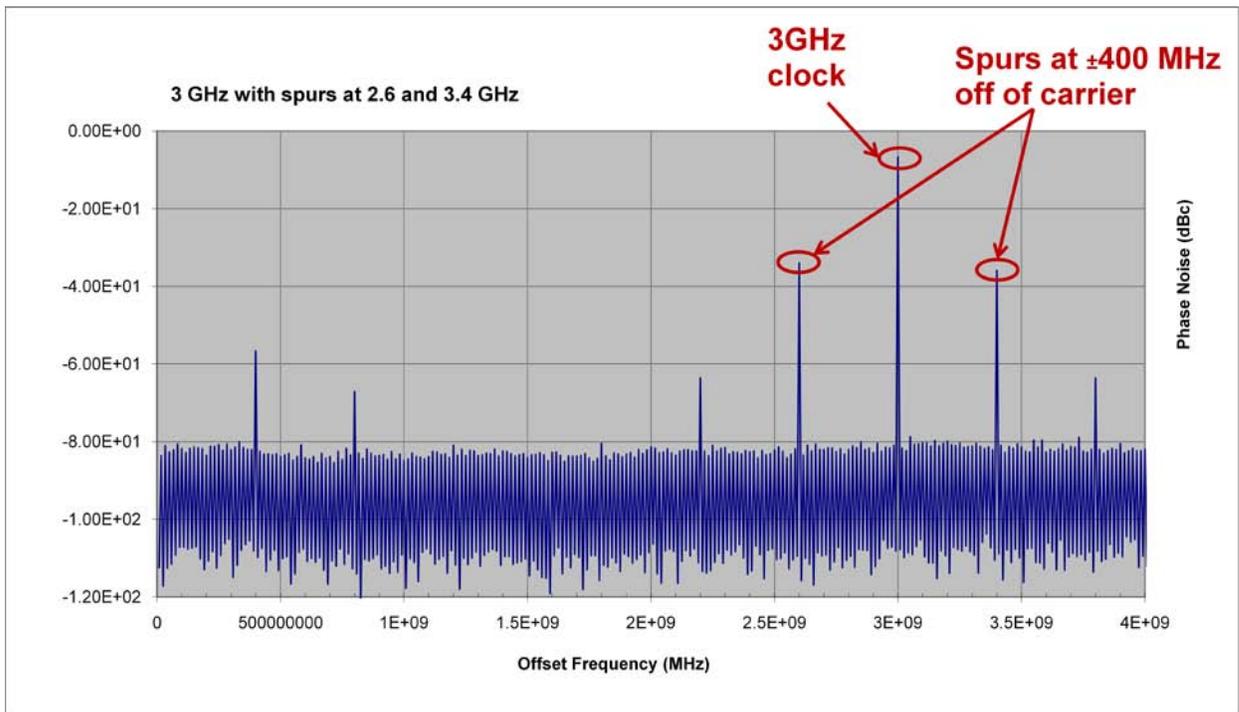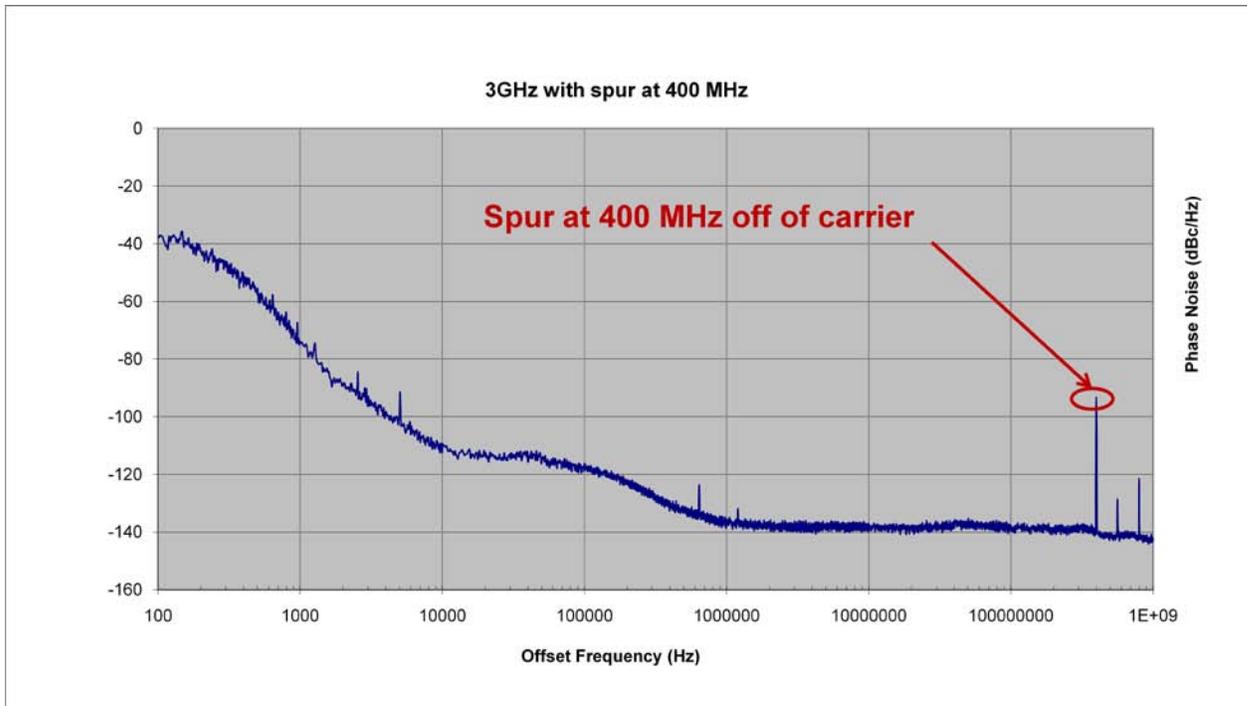


**Figure 9: 3 GHz Spectrum**

**Figure 10: 3 GHz Phase Noise Plot**

The spectrum and phase noise plots of the 3GHz signal show symmetrical spurs at 400 MHz above and below the 3 GHz clock frequency. Note that where the spectrum shows two equal sidebands, the phase noise plot of the same signal combines the effect of these two into a single spur located at 400 MHz off of the 3 GHz carrier. This is an example of the earlier statement about symmetrical sidebands.

The 3 GHz signal is then divided down by a factor of four to produce 750 MHz. The spectrum and phase noise plot of the 750 MHz signal coming out of the divide-by-four circuit are shown in Figures 11 and 12.
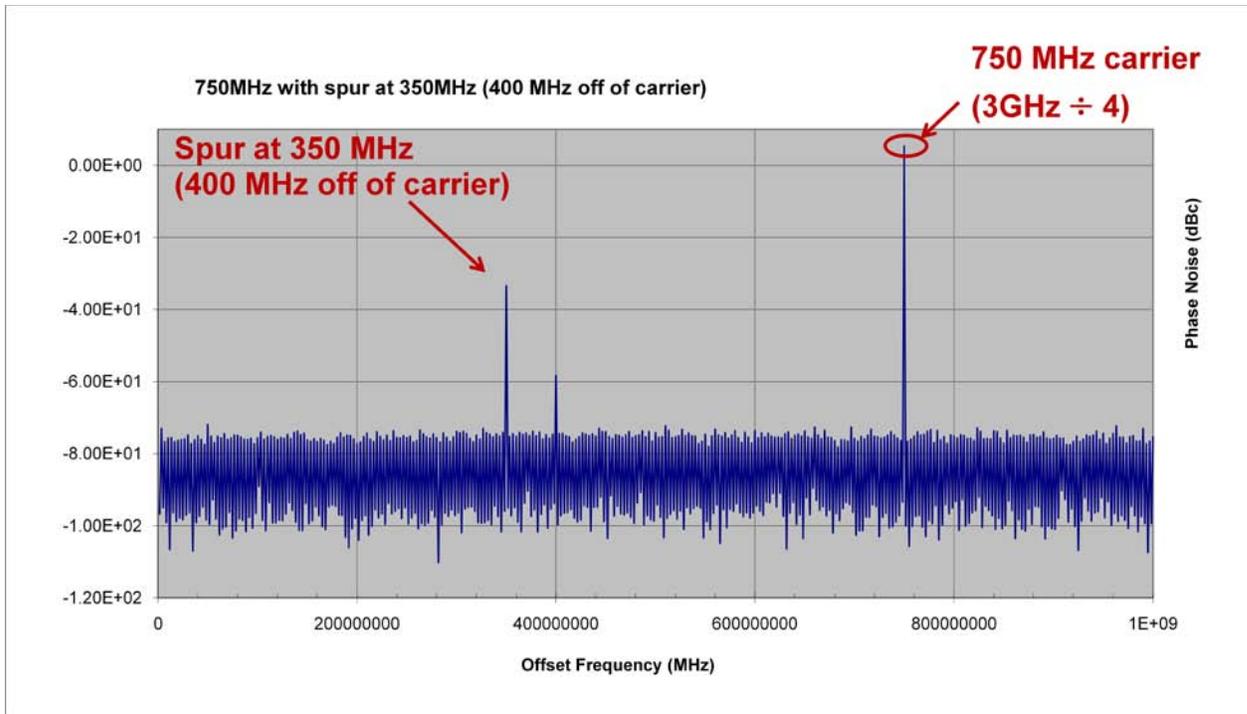
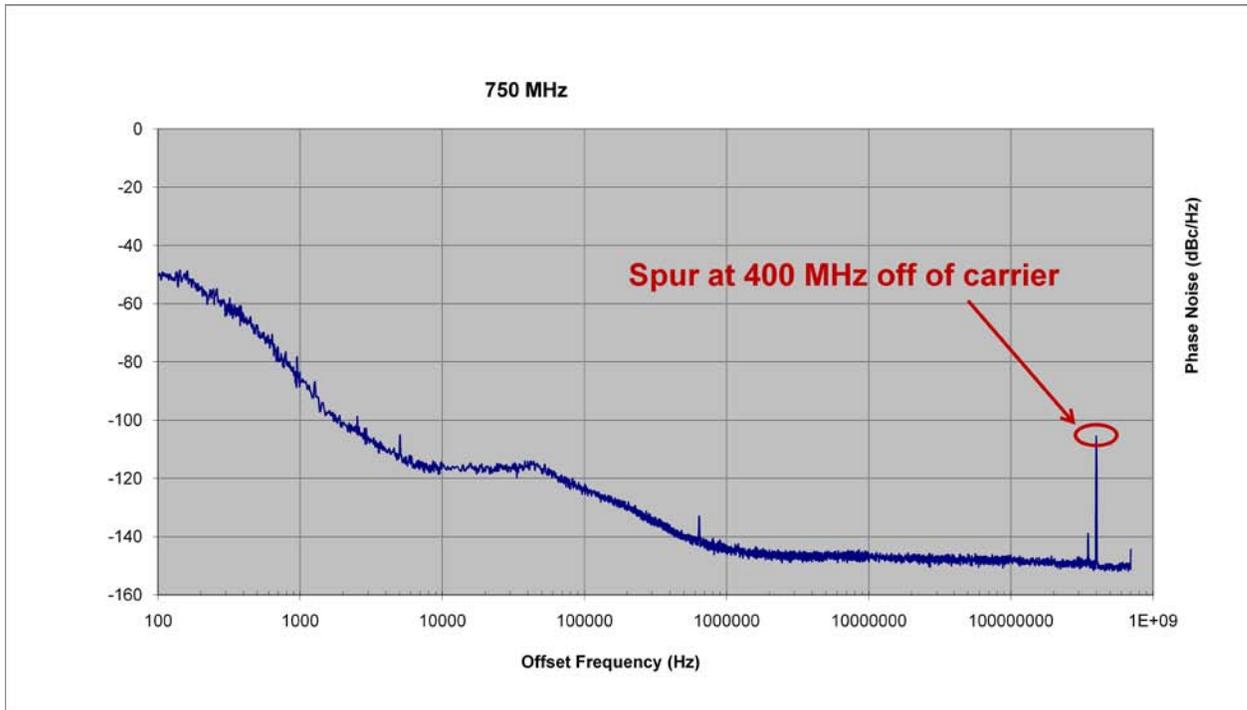**Figure 11: 750 MHz Spectrum**



**Figure 12: 750 MHz Phase Noise Plot**

As a result of the division by four, it can be seen that the spurs at 2.6 GHz and 3.4 GHz are aliased down to a single sideband spur at 350 MHz. Note that 350 MHz is a frequency value that is the same 400 MHz off of the 750 MHz carrier as 2.6 GHz is off of the 3 GHz carrier.

To further illustrate the aliasing, the 750 MHz signal was divided down once more to 375 MHz. The 25 MHz spur in Figure 13 is an alias of the spur at 350 MHz shown in Figure 11. That is, 25 MHz = 375 MHz – 350 MHz, which is another way of saying that 25 MHz is 350 MHz off of 375 MHz.
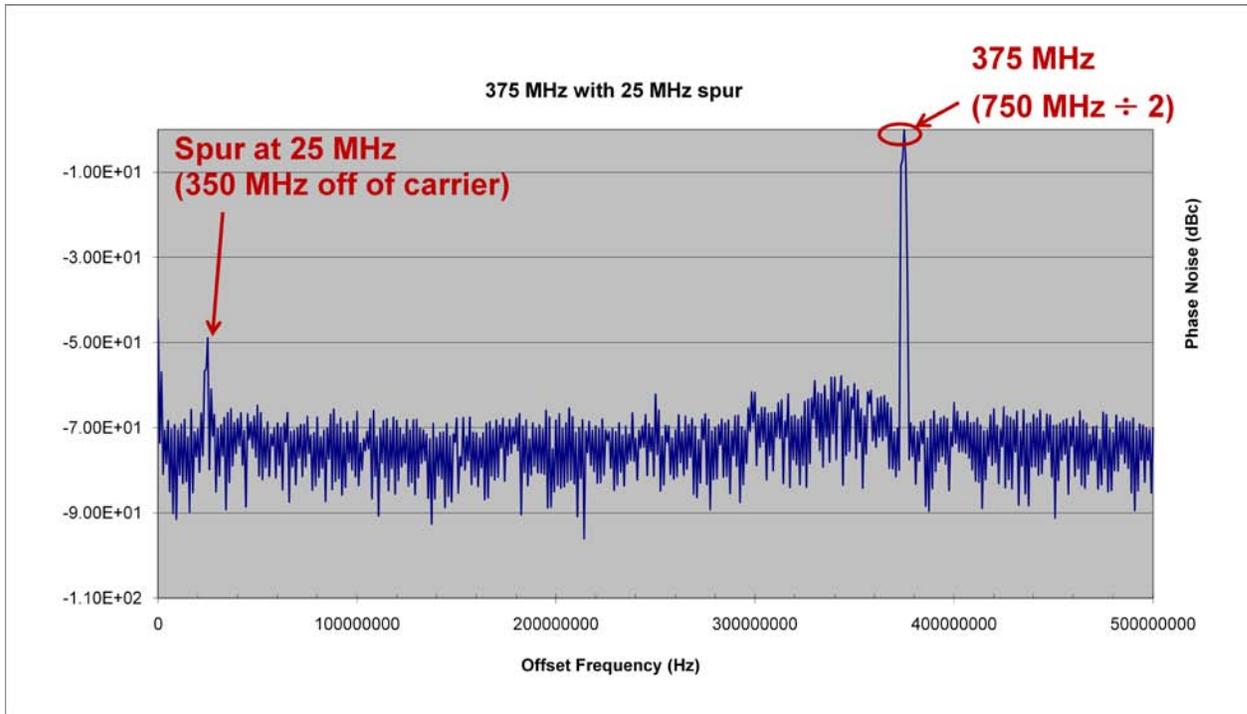


**Figure 13: 375 MHz Spectrum**

**Conclusion**

When measuring very low jitter clocks with low frequency values, the instrumentation noise floor can become a limiting factor. When the clock being measured is divided down from a higher frequency clock, a common technique to avoid this problem is to lower the value of the divider so that the measurement is made at a higher frequency. While this technique is commonly used, it will remove the jitter contribution that will result from higher-frequency jitter components being aliased down by the division. Although the resulting RMS jitter values may be artificially lower, this is an acceptable approach in applications where the far-out phase noise is relatively small.

When measuring low frequency clocks with anything more than very low jitter, the use of time domain equipment is recommended because the measurement can always be made at the actual, desired output frequency, no matter how low the clock frequency may be.

**References**

1. Jitter, Noise and Signal Integrity at High-Speed, Mike Peng Li, Prentice Hall 2008
2. Phase Locked Techniques, Floyd Gardner, section 7.4.1, Phase-Noise Propagation in Auxiliary Devices,  John Wiley and Sons, third edition 2005