How to Design Smart Gas and Water Utility Meters for the Utmost in Power Efficiency

Electronic water and gas meters represent some of the most vexing low-power design challenges for embedded control systems requiring RF connectivity. The nature of these applications requires them to be battery powered (i.e., electricity is rarely provided at the point of service for gas or water utilities). The expected battery life for these systems is often greater than 20 years. This requirement is dictated by the utility provider since a single service call from a technician can often exceed the entire cost of the smart meter. Because of this long-life design requirement, nearly all water and gas meters use a battery chemistry of lithium thionyl chloride ($LiSOCl_2$). This battery chemistry is chosen because of its very low self-discharge behavior and resulting ability to last for up to 20 years in these applications. However, these batteries are very expensive (as much as $1.5/A-hr) resulting in battery bill of material (BOM) costs of up to $10 to $15 per water or gas meter.

Many smart meter providers have determined that they can further differentiate their products by extending their communication range. In their system network topology, a fixed number of meters would communicate usage and billing information to a single repeater mounted on a utility pole through a sub-GHz proprietary network. The repeater would aggregate and transmit the collected information back to the utility provider over a cellular network modem or other backhaul channel. A single repeater could support approximately 1000 meter nodes. However, the cost of the repeater can be anywhere from 10 to 100 times greater than a single meter node. Metering suppliers often face pressure from their customers to reduce the number of repeaters in a given network. This can be most readily achieved by improving the robustness of the transmitter (TX) link.

There are a number of ways to improve the TX link budget. The most obvious solution is to increase the output power of the transmitter using a power amplifier (PA). This is also the most costly approach in terms of battery life. Another strategy is to enhance the protocol to minimize the number of dropped messages and subsequent retransmissions. Although a much lower power approach than simply adding a larger PA, this technique can still increase the new TX power budget by as much as 40 percent over the current power budgets.

Let’s consider three design requirements for one particular smart meter redesign:

- Allocate 40 percent more power budget to TX functions to increase range
- Maintain existing $LiSOCl_2$ battery size (A) and capacity (3650 mA-hr)
- Maintain existing battery service life of 20 years

The strategy is clear: Increase the power within the TX budget while not increasing its total power budget. The reductions would have to be found in other functional areas, namely the RX, active and sleep mode budgets. Figure 1 shows the original power budget and the target budget after redesign.

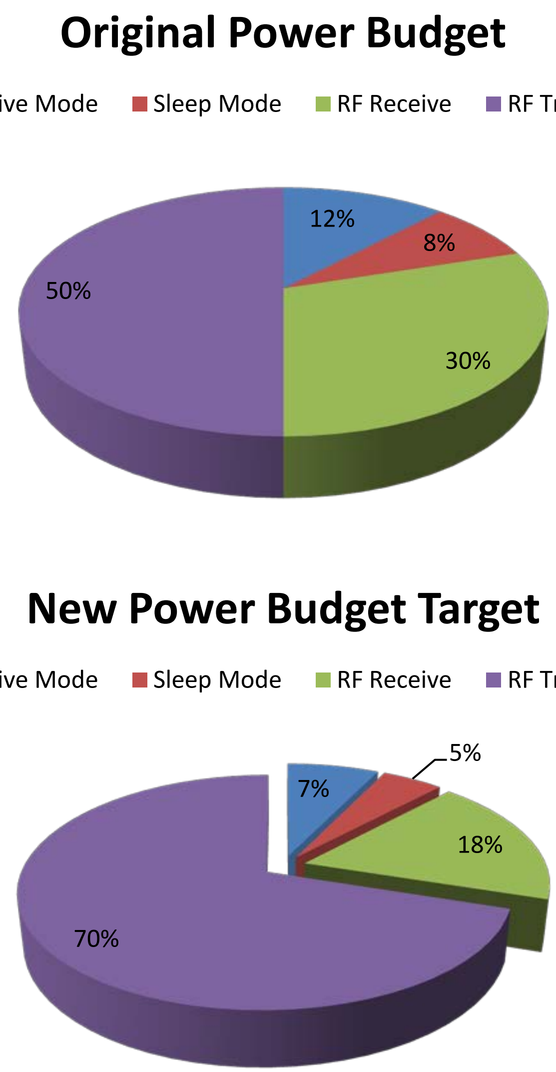

Figure 1. Comparison of Power Budgets for Smart Meter Applications

Higher Efficiency Voltage Conversion

To increase performance and reduce the power requirements of CMOS circuits, chip designers use the smallest practical device geometry to build their integrated circuits. It is common to find embedded processors and RF transceivers designed in 0.18 µm, 0.13 µm and even 90 nm geometries. One of the keys to reducing the power consumed by the device is reducing the internal operating voltage, thus reducing the CVf switching losses.

$$i_{switching\ loss} = C_{gate} \times V_{gate} \times frequency$$

Even though the battery supplying the device may have a terminal voltage of 3.6 volts, the device will operate at a much lower voltage internally.

Nearly every device on the market integrates internal low drop-out regulators (LDO) on-chip. This is the structure that takes a 3.6 V input and regulates the internal voltage of the chip to a lower value, typically 1.8 V or less. In other words, taking a 3.6 V input using a linear regulator with a 1.8 V output has a 50 percent conversion efficiency. Obviously, this gets worse as the output voltage decreases.

More advanced embedded controllers, such as the C8051F960 MCU shown in Figure 2, have integrated switching regulators with much higher efficiency than their LDO counterparts. In many cases, these devices can have switching efficiencies as high as 85 percent. This high efficiency has the effect of reducing the total current sourced from the battery and extends battery life.

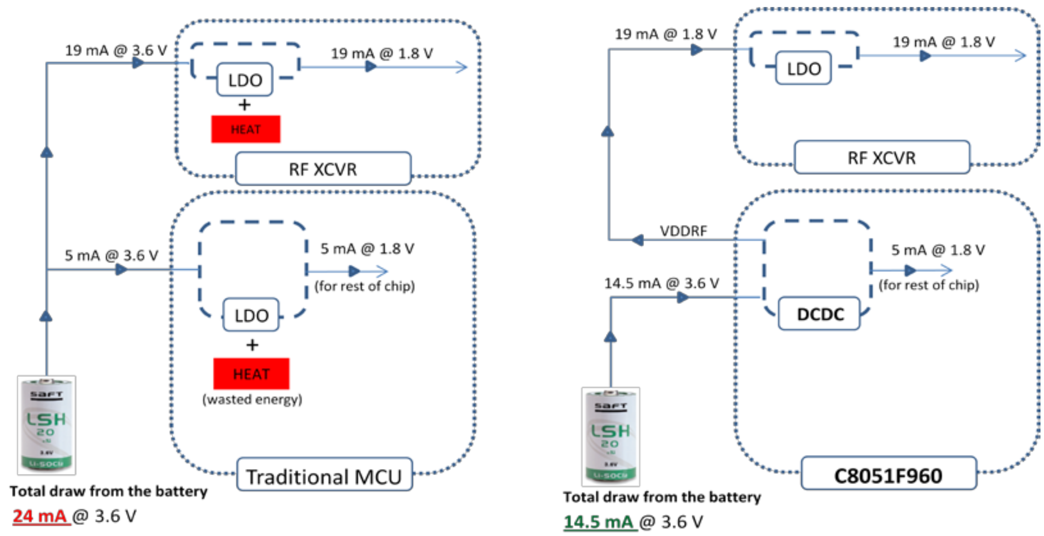

Figure 2. Comparison of Switching Efficiencies between Traditional and Advanced MCUs

Using this approach, we can greatly reduce the existing RX power budget.

$$Idd(battery) = \frac{Idd(xcvr) \times 1.8V}{3.6V \ \times 85\% \, efficiency} \rightarrow Idd(battery) = 62.5\% \; Idd(xcvr)$$

In other words, the current that is sourced by the battery for use by the radio receiver is approximately 62.5 percent of what it would be using the DC-DC buck converter as opposed to just an LDO. This approach has the net effect of reducing the RX current power budget by that amount.

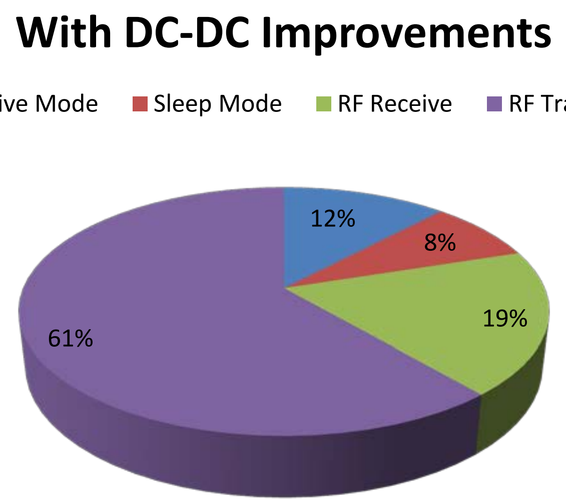

Figure 3. Enhanced RX Power Budget Enabled by DC-DC Switching Improvements

With this change, we have nearly met the new RX power budget (i.e., from 30 percent to 19 percent as shown in Figure 3, although the target is 18 percent). We must continue to optimize the system in other operating modes.

Lower Sleep Mode Power

Battery-powered meters often reside in a low-power sleep mode 99.9 percent of the time. For this reason, it is critical to keep the power consumption of sleep mode circuits as low as possible. Best-in-class devices of just a few years ago could achieve currents on the order of 1 µA using a 32.768 kHz crystal driving a low-power wake-up timer at 3.6 V. Today, further optimizations have yielded devices that can perform the same function at approximately 700 nA at the same voltage. Although the net savings is only 300 nA, this is essentially at 100 percent duty cycle, so this value can be subtracted directly from the power budget.

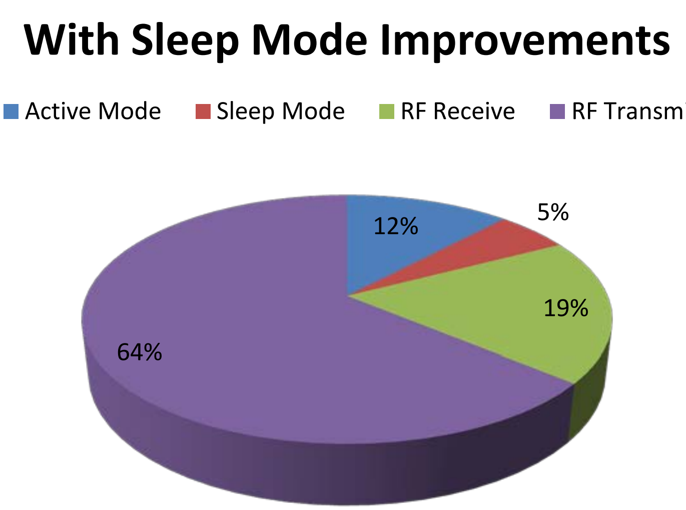

Figure 4. Impact of Sleep Mode Enhancements on Sleep Mode Budget

Using devices with lower power sleep modes, we are able to reduce the sleep mode budget from 8 percent to 5 percent as shown in Figure 4, thus meeting the design target. However, since we only met and did not exceed our goal, additional improvement is still needed to achieve our overall design goal. The last area of focus is reducing active mode power.

Reducing Active Mode Power

It is important to identify the dominant power consumption tasks in the metering application. In our gas or water meter example, there are two primary tasks:

- Check the state of a reed switch 20 times per second to calculate flow.
- Formulate a radio data packet every 15 seconds, and pass that data to the radio transmitter for broadcast.

In many metering applications, a device called a register encoder records the flow of natural gas or water. To the metering system, this can appear electrically as a series of switch closure events or pulses. In a traditional system, the CPU must wake up and sample the state of an I/O pin to determine if the switch is open or closed. If it is a physical reed switch, additional CPU bandwidth is needed to de-bounce the switch as well as manage pull-up resistors to guarantee it is a valid pulse as well as to minimize the current drain through the closed switch. Performing this function in software, even in the most optimized system, can consume well over 1 µA.

A better approach is to use a dedicated input capture timer that can operate autonomously while the device is in sleep mode. This technique has a number of advantages over a software-based approach. Primarily, the switch closures can be accumulated in a hardware register requiring little if any CPU intervention. Additionally, features, such as switch de-bounce, pull-up resistor management and self-calibration, can be integrated directly in the hardware. With two timer inputs, quadrature decode functionality can be supported to determine flow direction. This provides the capability of back-flow detection as well as an anti-tamper provision. A dedicated low-power input capture timer can consume as little as 400 nA at 3.6 V even with a sampling rate as high as 500 Hz. This is a significant improvement over performing this function in software.

When a CPU is running, it typically fetches instructions from non-volatile memory (e.g. flash). It is not uncommon for 40 percent of the active mode current to be attributed to flash access reads. For this reason, any time we are able to move data using dedicated hardware peripherals instead of the CPU, we can save power.

When preparing a message for RF transmission, the data must be manipulated several times. For example, let’s assume you have a 20 byte message payload that needs to be transmitted from the meter to the collector. Initially, these 20 bytes reside in SRAM. However, the data may include private customer information and, therefore, must be encrypted. Afterwards, a cyclic redundancy check (CRC) is computed and appended on the end of the encrypted message. Finally, the entire message will be encoded (e.g., Manchester, 3:6, etc.) before it is serially passed through the serial peripheral interface (SPI) to the radio transceiver. All of these functions can be performed in software using the CPU. However, it is much more efficient to have dedicated hardware, such as a dedicated packet processing engine (DPPE) as shown in Figure 5, perform these tasks.

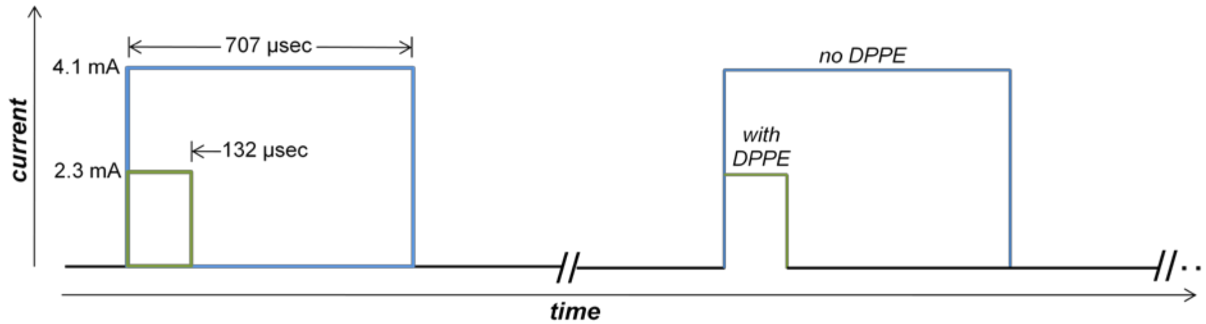

Figure 5. Processing Time and Power Savings Achieved with DPPE Hardware Block

Using a DPPE not only reduces the time needed to perform the functions, but it also reduces the current consumption during that time since flash memory is not being accessed. The net result can be up to a 90 percent power reduction during active mode. With these improvements, we are able to exceed the savings target for active mode, making it only 6 percent of the overall budget as shown in Figure 6.

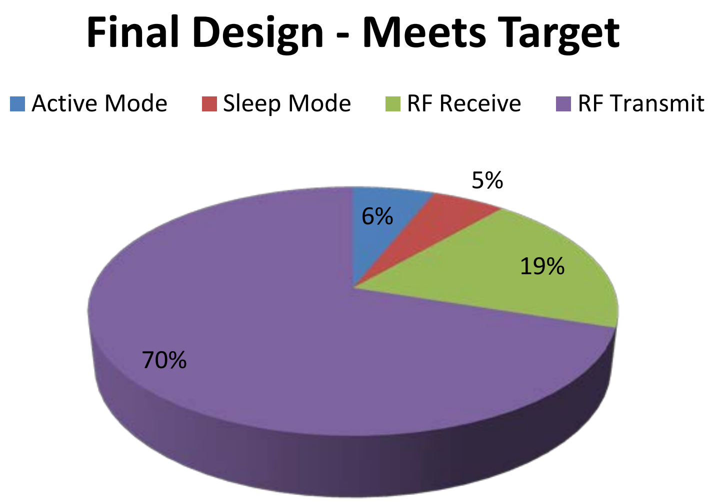

Figure 6. Smart Meter Power Reduction Results Achieved Using DPPE

After applying all three of the power saving techniques, we were able to successfully raise the TX power budget to 70 percent through a complete subsidy of savings from RX, sleep, and active modes. In other words, we met the overall design objectives of increasing the TX reliability without using a larger battery or reducing the original target life.

This example demonstrates how power savings could be applied to redistribute the overall budget in a smart meter application. However, power savings can be valuable in a number of other ways. One obvious example is the ability to use a smaller, lower-cost battery. Another benefit may be to increase the battery's target life using the same battery. A less obvious benefit is greater design margin and reduced warranty liability. Consider a scenario in which a meter manufacturer produces millions of units per year, each with a 20-year service warranty. If meters begin to fail after 15 years because of excessive power consumption, the potential liability to the supplier can involve tens of millions of meters. Ultimately, additional design margin provides peace of mind for engineers and investors alike.