Glitch-Free Frequency Shifting Simplifies Timing Design in Consumer Applications

System designers face significant design challenges in developing solutions to meet increasingly stringent performance and power requirements. The universal challenge is to simplify system design while minimizing power consumption in light of recent green and renewable energy initiatives. As vendors attempt to capitalize on the green market, more products are being labeled green, energy efficient, or environmentally friendly. Clock circuitry plays a valuable role in minimizing power consumption in consumer electronics. Reference clock frequencies can be dynamically reduced during operation to minimize power consumed by different subsystems in the design, providing an effective means of minimizing overall board-level power.

In the audio world, design challenges are no different. Not only is power a concern, but clock generation is becoming increasingly complex as the number of master clock frequencies in audio DAC/CODEC applications grows. Today's audio systems use as many as 24 bits for high-end audio with >110 dB SNR and with <0.003% THD specifications. Because of tightened specifications, audio designers require a wide range of master clocks from as low as 128x with a sampling frequency of 16 kHz for standard audio to as high as 2048x with a sampling frequency of 96 kHz for high-end audio.

Table 1. Audio DAC Frequencies

Standard	Complexity	Sample Frequency (kHz)	Sample Size (bits)	Master Clock (x)	Master Clock Frequency (MHz)
Standard	Low	16	16	128	2.048
		32	16	128	4.096
		44.1	16	128	5.6448
		48	16	128	6.144
		64	16	128	8.192
		88.2	16	128	11.2896
		96	16	128	12.288
Enhanced	Moderate	*	*	*	*
		*	*	*	*
		*	*	*	*
HiFi	High	16	96	2048	32.768
		32	96	2048	65.536
		44.1	96	2048	90.3168
		48	96	2048	98.304
		64	96	2048	131.072
		88.2	96	2048	180.6336
		96	96	2048	196.608

In addition to the complexity of generating a wide range of frequencies, audio applications face challenges in audio popping suppression because the sample clock or sample size differs between standards. To prevent pops from occurring, the audio DAC reference clock needs to glitchlessly switch between frequencies.

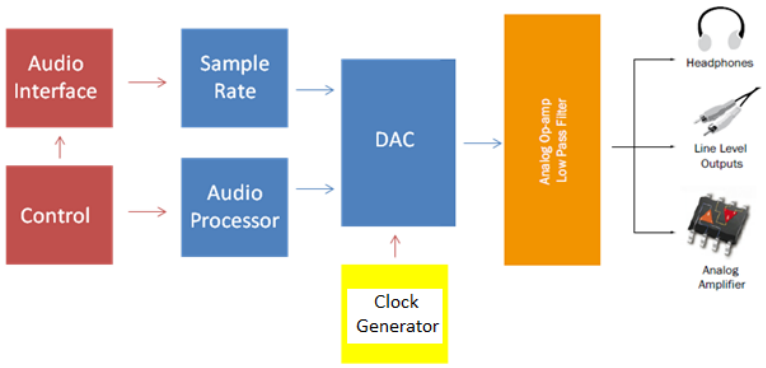

Figure 1. Audio DAC/CODEC Block Diagram

As a result, audio designers have traditionally been forced to design glitch-free frequency switching circuits or add anti-pop algorithms to suppress glitch-induced audio popping that might occur when the master clock shifts frequency.

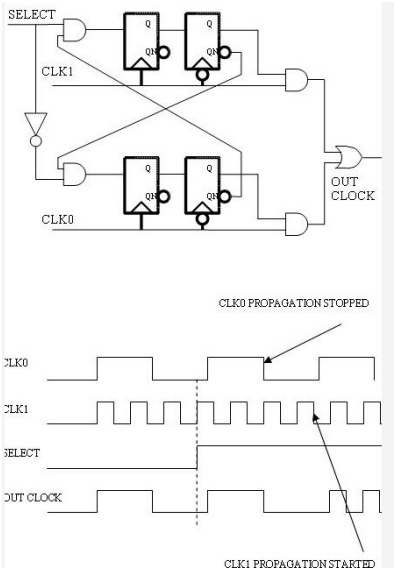

Figure 2. Traditional Glitch-Free Shifting Circuit

Timing and power challenges are also felt in the emerging market of PC computer-based USB applications, which interface PCs to audio systems. Timing considerations include determining a low-power, low-jitter master audio clock and devising the glitch-free shifting circuits essential for high-quality audio reproduction. Jitter generates error, which creates audio artifacts, and glitches induce audio pops, both of which degrade audio quality. Traditional schemes used to improve audio reproduction quality have included the use of Low Noise Phase Locked Loops (PLLs), Voltage Controlled Crystal Oscillators (VCXOs), synthesizers, buffers, external re-timers, etc. In addition to traditional schemes, designers have gone so far as to separate the Digital to Analog converters (DACs) from the USB receiver in the hope of further enhancing audio quality. Other methods of reducing jitter-induced audio artifacts and glitch-induced pops include adaptive approaches in which the master clock is switched less often. Newer asynchronous approaches are being used in which the master audio clock in the DAC is not synchronized to the clock in the computer. The quest for audio quality has not been simple.

PC designers also face challenges similar to those of audio designers in developing overclocking solutions for high-end gaming applications. Desktop PCs and laptops using Intel's Core 2 Quad 6600 and 790i processors and AMD's Phenom II, Athlon II X4 630 and Phenom X4 9950 processors are representative examples. Overclocking is a popular scheme, which increases the CPU clock frequency faster than specified and is used by gamers to maximize CPU computing power. Overclocking is a technique that slowly increments the clock frequency in a glitch-free fashion until the CPU clock has reached

its maximum operating frequency. However, traditional CPU clock generators have often suffered from glitches when the output frequency is shifted.

Glitchless Frequency Shifting Simplifies Design

Silicon Labs' newest clock generator family, the Si5350/51 Any-Frequency CMOS clock generator + VCXO, addresses these design challenges. The Si5350/51 is the industry's most frequency-flexible CMOS clock generator and supports the generation of any frequency up to 160 MHz on each of its eight clock outputs, providing greater frequency flexibility than traditional 4-PLL solutions. Most combinations of frequencies can be generated with 0 ppm error*, enabling the device to replace standalone clock ICs, XOs and VCXOs. The Si5350/51 timing ICs can simultaneously generate free-running clocks synchronized to a crystal input and clocks synchronized to a reference clock or analog control voltage input, allowing multiple board-level timing domains to be clocked from a single device. The Si5350/51 supports an innovative glitch-free frequency switching feature that eliminates glitches and runt pulses during output clock frequency transition.

* A very small combination of frequencies are generated with worst case 0.125 ppm synthesis error.

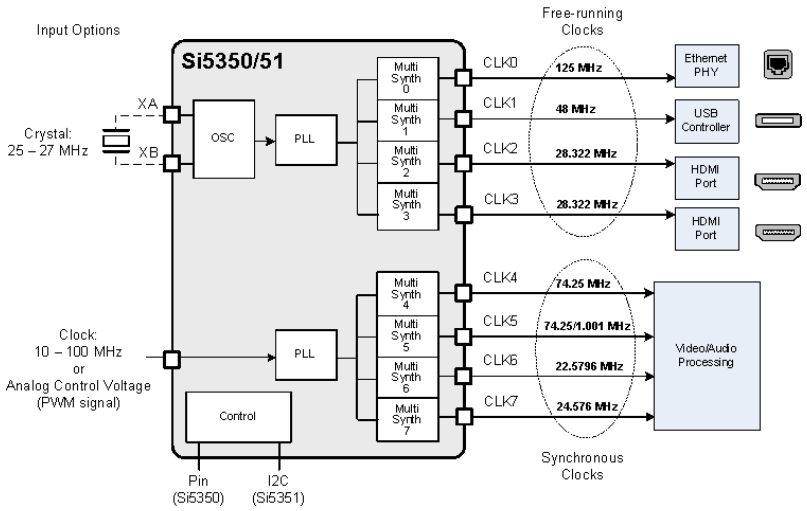

Figure 3. Si5350/51 Generates Timing for Multiple Clock Domains

Given its clock synthesis flexibility and the ability to dynamically switch between different frequencies glitchlessly, the Si5350/51 dramatically simplifies timing architectures while reducing the size and power requirements required by traditional solutions.

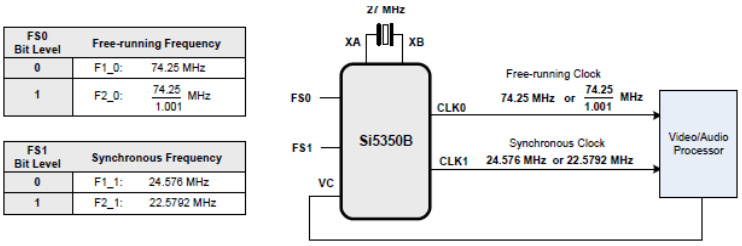

Figure 4. Si5350/51 Simultaneously Generates Audio and Video Clocks

The Si5350/51 simplifies system-level design by providing glitchless frequency shifting between multiple rates, as shown in Figure 4. This frequency shifting technique simplifies clock synthesis in power-sensitive designs, audio, audio USB, PC overclocking, video applications, and any application that requires a combination of frequencies. The Si5351 is an I^2C programmable clock generator. The frequency of each output can be dynamically changed without affecting the other device outputs by simply reprogramming a MultiSynth output divider value for the appropriate output clock*. The Si5350 is a factory- or field-programmable clock generator, which supports one or two Frequency Select pins that can be used to switch between two frequencies as illustrated below.

* Glitchless frequency shifting applies to frequencies less than or equal to 112.5 MHz.

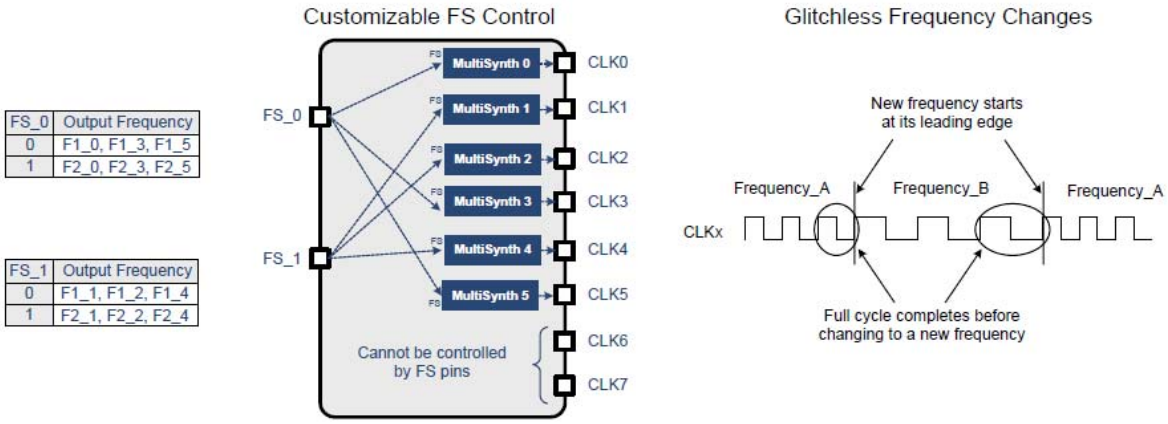

Figure 5. Custom Control Pins and Glitchless Frequency Change

Custom Samples and ClockBuilder™

Custom factory-programmed, pin-controlled versions of the Si5350 clock generator are available using Silicon Labs' Web-based ClockBuilder™ utility. The ClockBuilder™ configuration utility provides turnkey application-specific clocks, eliminating the need for field programming hardware and software. Since the Si5350/51 does not require metal mask changes to customized clock frequencies like traditional clock ICs, lead times for custom clocks are reduced from six weeks to less than two weeks. Silicon Labs also offers a field programming kit to enable rapid prototyping for when faster cycle times are required.

Summary

The Si5350/51 is the industry's most flexible CMOS clock generator capable of supporting any-frequency synthesis on eight independent output clocks as well as supporting glitch-free, on-the-fly frequency switching. By providing this level of frequency flexibility, the Si5350/51 eliminates the need for fixed-frequency clock generators and discrete crystal oscillators. The device provides outstanding jitter performance, enabling a single device to provide critical reference timing for cost-sensitive consumer, enterprise and communications applications including audio, video, computing or any application that requires multiple frequencies. Clock frequency shifting is greatly simplified, and the need for additional glitch-reducing circuitry and software is eliminated. The best-in-class flexibility and integration provided by the Si5350/51 greatly simplifies timing architectures.