Clock Generator Considerations for the Rapidly Growing PCIe Market

Introduction

The PCI Express (PCIe) interconnect has grown very popular over the past five years and is now widely used in many different markets and applications. Originally developed for use in the personal computing (PC) and server markets, the PCIe standard has become a de-facto data bus used in communications, storage, industrial and consumer electronics products. Although the performance requirements for PCIe reference clocks are standard within any application, numerous clock generator and clock buffer products optimized for PCIe are available to help systems designers address the unique requirements of consumer, server/storage and communications applications.

History of the PCIe Interconnect

A PCIe data link consists of one or more lanes encompassing a transmit (Tx) and receive (Rx) differential pair. A PCIe slot may contain up to 32 lanes, providing excellent bandwidth scalability. The first-generation PCIe specification was introduced by the PCI-Special Interest Group (SIG) in 2003, with a maximum data throughput of 16 GBytes per second (GB/s) in a 32-lane configuration. At the time, this specification was a major improvement over the previously used PCI and PCI-X bus architectures. Four years later, the PCIe 2.0 spec was released, which doubled the transfer rate to 32GB/s in a 32-lane configuration. This effectively meant designers could get the same amount of data transfer bandwidth in half the lanes of a Gen1 based design. The PCI-SIG introduced the third-generation specification in November 2011, again doubling the transfer rate to 64 GB/s.

	Nominal Bit Rate	Data Throughput Per Lane	Max Data Throughput (32 Lanes)	Year Released
PCIe 1.1	2.5 Gbits/s	500 MBytes/s	16 GBytes/s	2003
PCIe 2.1	5.0 Gbits/s	1.0 GBytes/s	32 GBytes/s	2007
PCIe 3.0	8.0 Gbits/s	2.0 GBytes/s	64 GBytes/s	2010

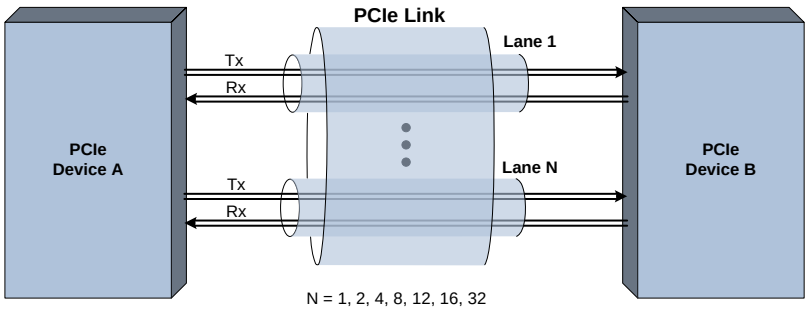

Figure 1. The PCI Express Link

Market Trends Fueling PCIe Adoption

In 2007, PCIe Gen2 had become widely used in most server/storage and communications infrastructure applications. At the same time, PCIe Gen1 had started gaining traction in the embedded, instrumentation and customer premises equipment (CPE) markets. The need for higher data throughput, an attractive cost point, scalability, and growing availability of PCIe ports in SoCs, ASICs, microprocessors and FPGAs were all contributing factors in PCIe Gen1 proliferation into these markets. Multi-function printers, network switches, routers, wireless access points and high-end consumer electronics were all starting to adopt PCIe as larger amounts of digital data were being both created and consumed by consumers.

Although the consumer electronics market had not yet adopted the PCIe interconnect, it was fueling the requirement for PCIe to continue scaling towards higher data rates and larger bandwidth capability. By early 2008, smartphone adoption and social media were both rapidly growing in popularity, enabling end users to not only create, store and share new digital media content such as pictures and video but also to request access to that content anywhere and anytime via the Internet and cellular devices. At the same time, cloud computing and audio/video streaming services were becoming popular with consumers.

Furthermore, Internet-based high-definition music and video services were becoming mainstream, increasing demand for higher bandwidth capability from server and datacenter infrastructure. Consumer thirst for high-resolution media content was requiring more bandwidth at faster speeds.

The culmination of these market trends has led to the adoption of the PCIe Gen3 interconnect standard, which has been predominantly used in server, storage, and datacenter end markets to date. New technology advancements in solid state drive (SSD) devices have further enabled datacenter and cloud computing to keep up with consumer demand for digital content. Enterprise SSDs use PCIe Gen3 as the main interconnect between the host motherboard and SSD controllers, enabling incredibly fast access to content stored in datacenters and in the cloud.

By using PCIe Gen3, networking and enterprise equipment manufacturers have been able to scale bandwidth and data rates without rebuilding the entire infrastructure. As with the previous generation shift from PCIe Gen1 to PCIe Gen2 in the 2007 timeframe, PCIe Gen2 is now becoming widely adopted in the embedded, communications and CPE markets. PCIe Gen2 ports are now commonly found in general-purpose microprocessors, FPGAs, SoCs and ASICs.

As higher resolution digital media is being created, stored, streamed and displayed, consumer electronics devices are also adopting PCIe. Today's high-end digital televisions, DSLR cameras and home gateways are all taking advantage of the high data rate capabilities that the PCIe interconnect has to offer.

Jitter Performance

As the data rates and bandwidths have scaled upwards, so to have the performance requirements of reference clocks. Table 1 provides a snapshot of the maximum jitter requirements corresponding to each of the three PCIe generation specifications.

Table 1. PCIe Clocking Architectures

	Description	Symbol	Limit	Units
Common Refclk Architecture				
PCIe 1.1	Random Jitter	Rj	4.7	ps pk-pk
	Deterministic Jitter	Dj	41.9	ps pk-pk
	Total Jitter Where Tj = Dj + 14.069 x Rj (for BER 10^{-12})	Tj	108	ps pk-pk
PCIe 2.1	High Frequency RMS Jitter Measured from 1.5 MHz to Nyquist (or $f_{REFCLK/2}$)	J_{RMS-HF}	3.1	ps RMS
	Low Frequency RMS Jitter Measured from 10 kHz to 1.5 MHz	J_{RMS-LF}	3.0	ps RMS
PCIe 3.0	Random Jitter	J_{RMS}	1.0	ps RMS
Data Clocked Refclk Architecture				
PCIe 1.1	Not defined in PCIe standards			
PCIe 2.1	High Frequency RMS Jitter Measured from 1.5 MHz to Nyquist (or $f_{REFCLK/2}$)	J_{RMS-HF}	4.0	ps RMS
	Low Frequency RMS Jitter Measured from 10 kHz to 1.5 MHz	J_{RMS-LF}	7.5	ps RMS
PCIe 3.0	Random Jitter	J_{RMS}	1.0	ps RMS
Separate Refclk Architecture				
PCIe 1.1	Device dependent. Not defined in PCIe standards.			
PCIe 2.1				
PCIe 3.0				

System designers should consider their total clock jitter budget and not just the jitter of a single clock generator of buffer. Ideally, designers should specify clock generators and buffers that offer jitter performance well within the maximum specifications set by the PCI-SIG. Optimal PCIe timing solutions should offer more than a 50 percent margin.

Power Consumption

Energy consumption and associated costs have become a paramount issue for data center operators and owners. Data centers are large consumers of servers and storage systems. Most PCIe clock generator and buffer solutions in the market use constant current mode HCSL output buffer technology, first developed in the early 2000s for the PC market. As the name suggests, each output consumes a constant current, so clock outputs are continuously burning power. Optimal clock generator and buffer solutions use low-power push-pull output buffer technology, which conversely provides a constant voltage source. These output buffers provide an output signal fully compatible to HCSL for PCIe applications, with the added benefit of 66 percent power consumption reduction over the constant current mode solutions.

Edge Rate / Skew Tuning

Best-in-class clock generators and buffers optimized for PCIe applications feature I^2C programmable edge rate and skew features. With these PCIe clocks, each output can be individually tuned to the PCB environment, reducing electromagnetic interference (EMI). Mismatch in the edge rate and skew will create common mode energy that radiates EMI as well as an unstable cross point that causes data loss. Clock outputs commonly drive multiple buses with the outputs. Therefore, any clock misalignments will add up to a large amount of common mode energy. Having the capability to quickly tune the skew or edge rates of a particular output could potentially prevent board re-spins.

Board Space and BOM

Board space and bill-of-materials (BOM) cost are always critical considerations in consumer and embedded applications. In addition to power consumption savings, another advantage of using low-power push-pull output buffers is that all terminating resistor are integrated. This saves up to four resistors per clock output, reducing BOM cost as well as total PCB area needed for the PCIe clocks. Addressing these

consumer electronics market needs, Silicon Labs' offers the Si52111-xx, Si52112-xx and Si53102 PCIe clock ICs in small-form-factor 3 mm x 3 mm 10-pin TDFN and 1.4 mm x 1.6 mm 8-pin TDFN packages.

Summary

PCIe has become the high-speed interconnect of choice in the server/storage, embedded, communications and consumer markets. Technology trends have contributed to the proliferation of PCIe from generation to generation, with the server/storage markets adopting the newer standards first. As the data rate and bandwidth capabilities have scaled from Gen1 to Gen2 to Gen3, clock generator performance has become increasingly important as well. Jitter performance, power consumption, signal integrity, EMI, BOM cost and total PCB area are also critical factors that designers must take into consideration.

Silicon Labs offers a wide array of clock generator and clock buffer solutions that meet the PCIe Gen1.1, 2.1 and 3.0 specifications, with a multitude of feature sets and power savings benefits available to match a broad range of application requirements. For more information about Silicon Labs' PCIe timing solutions, visit www.silabs.com/pcie.

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