Using Direct Memory Access for Data Transfers without CPU Intervention Can Reduce Power and Extend System Battery Life

The implementation of direct memory access (DMA) in 32-bit microcontrollers (MCUs) based on ARM® cores has limitations. Specifically, DMA does not support chaining (connecting a string of peripherals using DMA) or sequencing (executing specific steps in the chain of peripherals multiple times), and it requires CPU intervention. Silicon Labs’ SiM3L1xx low-power 32-bit microcontroller devices include an on-chip Data Transfer Manager (DTM) that addresses both of these limitations without requiring CPU intervention. The DTM allows a string of DMA transfers to occur autonomously, thus off-loading the CPU and saving power. For applications requiring radio communications, the SiM3L1xx MCU is able to autonomously construct and receive radio packets using the DTM. In the following example, the DTM is constructing a radio packet and sending it via the serial peripheral interface (SPI) to a connected radio. Chaining is used between the peripherals, and sequencing enables multiple iterations of AES encryption to occur before data is sent to the CRC peripheral.

In addition to off-loading the CPU in active mode, the DTM avoids executing code from flash, providing a 30-40 percent power savings and extending application battery life. Although primarily intended for the construction and reception of radio packets, the DTM has the flexibility to adapt to a wide range of applications that require a chain of DMA operations.

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