

PCI-EXPRESS 1 代、2 代和 3 代四输出时钟发生器及 25 MHz 参考时钟

特点

- PCI-Express 1 代、2 代和 3 和 Gen 4 通用时钟兼容
- 第 3 代 SRNS 兼容
- 低功耗，差分输出
- 无需终端电阻
- 各时钟专用输出使能硬件引脚
- 差分时钟上有扩频使能引脚
- 四个 PCI-Express 时钟
- 25 MHz 参考时钟
- 25 MHz 晶体输入或时钟输入
- 信号完整性调整
- 支持 I²C，带回读功能
- 使用三角扩频改善图最大程度地减少电磁干扰 (EMI)
- 扩展温度范围
-40 至 85 °C
- 3.3 V 电源
- 24 引脚 QFN 封装

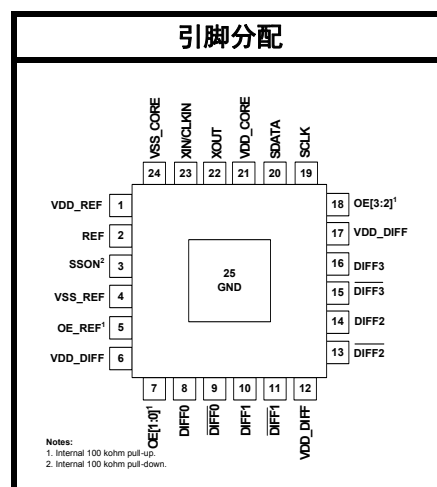


应用

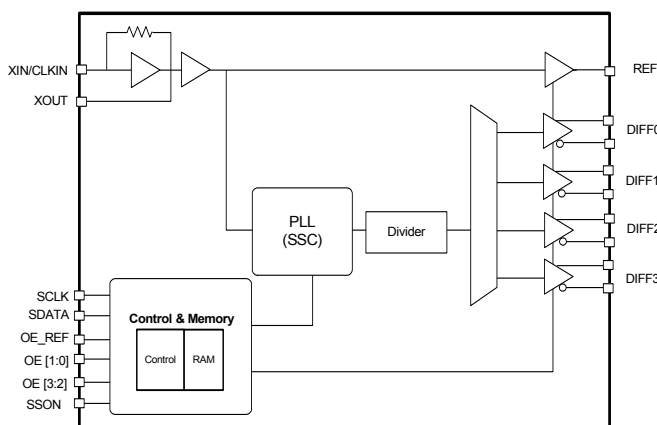
- 网络附加存储
- 无线接入点
- 多功能打印机
- 路由器

描述

Si52143 是扩频时钟使能 PCIe 时钟发生器，可作为四个 PCIe 时钟和一个 25 MHz 参考时钟的时钟源。设备有三个用于启用输出（打开电源时即动态生成）的硬件输出使能引脚，和一个控制 PCIe 时钟输出上的扩频的硬件引脚。除硬件控制引脚外，I²C 编程功能还可用于动态控制 PCIe 时钟输出上的真、补偿或两种差分信号上的偏移、边缘频率和振幅。这种控制功能可在 PCIe 时钟输出上实现最佳信号完整性和最佳 EMI 签名。关于信号完整性调整和可配置性的信息请参考 AN636。使用 Silicon Labs PCIe 时钟抖动工具可快速轻松地测量 PCIe 时钟抖动。免费下载 www.silabs.com/pcie-learningcenter。



功能模块示意图



专利申请中

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1. Electrical Specifications

Table 1. DC Electrical Specifications

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--------------------------------------------------|----------------------|----------------------------------------------------------------------------|-----------------------|-----|-----------------------|------|
| 3.3 V Operating Voltage | VDD core | 3.3 ± 5% | 3.135 | 3.3 | 3.465 | V |
| 3.3 V Input High Voltage | V _{IH} | Control input pins | 2.0 | — | V _{DD} + 0.3 | V |
| 3.3 V Input Low Voltage | V _{IL} | Control input pins | V _{SS} - 0.3 | — | 0.8 | V |
| Input High Voltage | V _{IHI2C} | SDATA, SCLK | 2.2 | — | — | V |
| Input Low Voltage | V _{ILI2C} | SDATA, SCLK | — | — | 1.0 | V |
| Input High Leakage Current | I _{IH} | Except internal pull-down resistors, 0 < V _{IN} < V _{DD} | — | — | 5 | μA |
| Input Low Leakage Current | I _{IL} | Except internal pull-up resistors, 0 < V _{IN} < V _{DD} | -5 | — | — | μA |
| 3.3 V Output High Voltage (Single-Ended Outputs) | V _{OH} | I _{OH} = -1 mA | 2.4 | — | — | V |
| 3.3 V Output High Voltage (Single-Ended Outputs) | V _{OL} | I _{OL} = 1 mA | - | — | 0.4 | V |
| High-impedance Output Current | I _{OZ} | | -10 | — | 10 | μA |
| Input Pin Capacitance | C _{IN} | | 1.5 | — | 5 | pF |
| Output Pin Capacitance | C _{OUT} | | — | — | 6 | pF |
| Pin Inductance | L _{IN} | | — | — | 7 | nH |
| Dynamic Supply Current | I _{DD_3.3V} | All outputs enabled. Differential clocks with 5" traces and 2 pF load. | — | — | 55 | mA |

Table 2. AC Electrical Specification

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|-------------------------------------------------------------|--------------------|--------------------------------------------------------------|------|------|---------|------|
| Crystal | | | | | | |
| Long-term Accuracy | L_{ACC} | Measured at VDD/2 differential | — | — | 250 | ppm |
| Clock Input | | | | | | |
| Duty Cycle | T_{DC} | Measured at VDD/2 | 45 | — | 55 | % |
| CLKIN Rising and Falling Slew Rate | T_R/T_F | Measured between 0.2 V _{DD} and 0.8 V _{DD} | 0.5 | — | 4.0 | V/ns |
| Cycle to Cycle Jitter | T_{CCJ} | Measured at VDD/2 | — | — | 250 | ps |
| Long Term Jitter | T_{LTJ} | Measured at VDD/2 | — | — | 350 | ps |
| Input High Voltage | V_{IH} | XIN/CLKIN pin | 2 | — | VDD+0.3 | V |
| Input Low Voltage | V_{IL} | XIN/CLKIN pin | — | — | 0.8 | V |
| Input High Current | I_{IH} | XIN/CLKIN pin, VIN = VDD | — | — | 35 | μA |
| Input Low Current | I_{IL} | XIN/CLKIN pin, 0 < VIN < 0.8 | -35 | — | — | μA |
| DIFF at 0.7 V | | | | | | |
| Duty Cycle | T_{DC} | Measured at 0 V differential | 45 | — | 55 | % |
| Output-to-Output Skew | T_{SKEW} | Measured at 0 V differential | — | — | 50 | ps |
| Cycle to Cycle Jitter | T_{CCJ} | Measured at 0 V differential | — | 35 | 50 | ps |
| PCIe Gen 1 Pk-Pk Jitter, Common Clock | Pk-Pk | PCIe Gen 1 | 0 | 40 | 50 | ps |
| PCIe Gen 2 Phase Jitter, Common Clock | RMS_{GEN2} | 10 kHz < F < 1.5 MHz | 0 | 2 | 2.6 | ps |
| | | 1.5 MHz < F < Nyquist Rate | 0 | 2 | 2.6 | ps |
| PCIe Gen 3 Phase Jitter, Common Clock | RMS_{GEN3} | PLL BW of 2–4 or 2–5 MHz, CDR = 10 MHz | 0 | 0.5 | 0.9 | ps |
| PCIe Gen 3 Phase Jitter, Separate Reference No Spread, SRNS | RMS_{GEN3_SRNS} | PLL BW of 2–4 or 2–5 MHz, CDR = 10 MHz | — | 0.35 | 0.64 | ps |
| PCIe Gen 4 Phase Jitter, Common Clock | RMS_{GEN4} | PLL BW of 2–4 or 2–5 MHz, CDR = 10 MHz | — | 0.5 | 0.9 | ps |
| Long Term Accuracy | L_{ACC} | Measured at 0 V differential | — | — | 100 | ppm |
| Rising/Falling Slew Rate | T_R / T_F | Measured differentially from ±150 mV | 1 | — | 8 | V/ns |
| Voltage High | V_{HIGH} | | — | — | 1.15 | V |
| Voltage Low | V_{LOW} | | -0.3 | — | — | V |
| Crossing Point Voltage at 0.7 V Swing | V_{OX} | | 300 | — | 550 | mV |

Notes:

1. Visit www.pcisig.com for complete PCIe specifications.
2. Gen 4 specifications based on the PCI-Express Base Specification 4.0 rev. 0.5.
3. Download the Silicon Labs PCIe Clock Jitter Tool at www.silabs.com/pcie-learningcenter.

Table 2. AC Electrical Specification (Continued)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------|------------------------------------------------------------------------|------|------|-----|------|
| Spread Range | SPR-2 | Down spread | — | -0.5 | — | % |
| Modulation Frequency | F _{MOD} | | 30 | 31.5 | 33 | kHz |
| REF(25 MHz) at 3.3 V | | | | | | |
| Duty Cycle | T _{DC} | Measurement at 1.5 V | 45 | — | 55 | % |
| Rising and Falling Edge Rate | T _R / T _F | Measured between 0.8 and 2.0 V | 1.0 | — | 4.0 | V/ns |
| Cycle to Cycle Jitter | T _{CCJ} | Measurement at 1.5 V | — | — | 300 | ps |
| Long Term Accuracy | L _{ACC} | Measured at 1.5 V | — | — | 100 | ppm |
| Enable/Disable and Set-Up | | | | | | |
| Clock Stabilization from Power-up | T _{STABLE} | Measured from the point both V _{DD} and clock input are valid | — | — | 1.8 | ms |
| Stopclock Set-up Time | T _{SS} | | 10.0 | — | — | ns |
| Notes: | | | | | | |
| <ol style="list-style-type: none"> 1. Visit www.pcisig.com for complete PCIe specifications. 2. Gen 4 specifications based on the PCI-Express Base Specification 4.0 rev. 0.5. 3. Download the Silicon Labs PCIe Clock Jitter Tool at www.silabs.com/pcie-learningcenter. | | | | | | |

Table 3. Absolute Maximum Conditions

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|-----------------------------|------|-----|-----|-----------------|
| Main Supply Voltage | V _{DD_3.3V} | Functional | — | — | 4.6 | V |
| Input Voltage | V _{IN} | Relative to V _{SS} | -0.5 | — | 4.6 | V _{DC} |
| Temperature, Storage | T _S | Non-functional | -65 | — | 150 | °C |
| Temperature, Operating Ambient | T _A | Functional | -40 | — | 85 | °C |
| Temperature, Junction | T _J | Functional | — | — | 150 | °C |
| Dissipation, Junction to Case | Ø _{JC} | JEDEC (JESD 51) | — | — | 25 | °C/W |
| Dissipation, Junction to Ambient | Ø _{JA} | JEDEC (JESD 51) | — | — | 37 | °C/W |
| ESD Protection (Human Body Model) | ESD _{HBM} | JEDEC (JESD 22-A114) | 2000 | — | — | V |
| Flammability Rating | UL-94 | UL (Class) | V-0 | | | |
| Note: While using multiple power supplies, the voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is not required. | | | | | | |

2. Functional Description

2.1. Crystal Recommendations

If using crystal input, the device requires a parallel resonance 25 MHz crystal.

Table 4. Crystal Recommendations

| Frequency (Fund) | Cut | Loading | Load Cap | Shunt Cap (max) | Motional (max) | Tolerance (max) | Stability (max) | Aging (max) |
|------------------|-----|----------|----------|-----------------|----------------|-----------------|-----------------|-------------|
| 25 MHz | AT | Parallel | 12–15 pF | 5 pF | 0.016 pF | 35 ppm | 30 ppm | 5 ppm |

2.1.1. Crystal Loading

Crystal loading is critical for ppm accuracy. In order to achieve low/zero ppm error, use the calculations below in section 2.1.2 to estimate the appropriate capacitive loading (CL).

Figure 1 shows a typical crystal configuration using two trim capacitors. It is important that the trim capacitors are in series with the crystal.

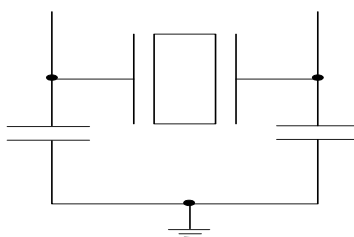


Figure 1. Crystal Capacitive Clarification

2.1.2. Calculating Load Capacitors

In addition to the standard external trim capacitors, consider the trace capacitance and pin capacitance to calculate the crystal loading correctly. The capacitance on each side is in series with the crystal. The total capacitance on both sides is twice the specified crystal load capacitance (CL). Trim capacitors are calculated to provide equal capacitive loading on both sides.

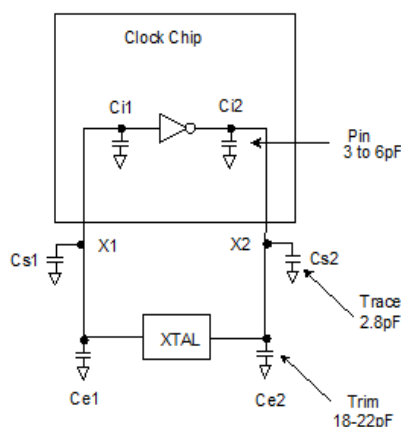


Figure 2. Crystal Loading Example

Use the following formulas to calculate the trim capacitor values for Ce1 and Ce2.

Load Capacitance (each side)

$$C_e = 2 \times CL - (C_s + C_i)$$

Total Capacitance (as seen by the crystal)

$$CL_e = \frac{1}{\left(\frac{1}{C_{e1} + C_{s1} + C_{i1}} + \frac{1}{C_{e2} + C_{s2} + C_{i2}} \right)}$$

- CL: Crystal load capacitance
- CL_e: Actual loading seen by crystal using standard value trim capacitors
- C_e: External trim capacitors
- C_s: Stray capacitance (terraced)
- C_i: Internal capacitance (lead frame, bond wires, etc.)

2.2. OE Pin Definition

The OE pins are active high inputs used to enable and disable the output clocks. To enable the output clock, the OE pin needs to be logic high and the I²C output enable bit needs to be logic high. There are two methods to disable the output clocks: the OE is pulled to a logic low, or the I²C enable bit is set to a logic low. The OE pins is required to be driven at all time and even though it has an internally 100 kΩ resistor.

2.3. OE Assertion

The OE signals are active high input used for synchronous stopping and starting the output clocks respectively while the rest of the clock generator continues to function. The assertion of the OE signal by making it logic high causes stopped respective output clocks to resume normal operation. No short or stretched clock pulses are produced when the clock resumes. The maximum latency from the assertion to active outputs is no more than two to six output clock cycles.

2.4. OE Deassertion

When the OE pin is deasserted by making its logic low, the corresponding output clocks are stopped cleanly, and the final output state is driven low.

2.5. SSON Pin Definition

SSON is an active input used to enable –0.5% spread on all DIFF outputs. When sampled high, –0.5% spread is enabled on all DIFF outputs. When sampled low, the DIFF output frequencies are non-spread.

3. Test and Measurement Setup

Figure 3 shows the test load configuration for HCSL clock outputs.

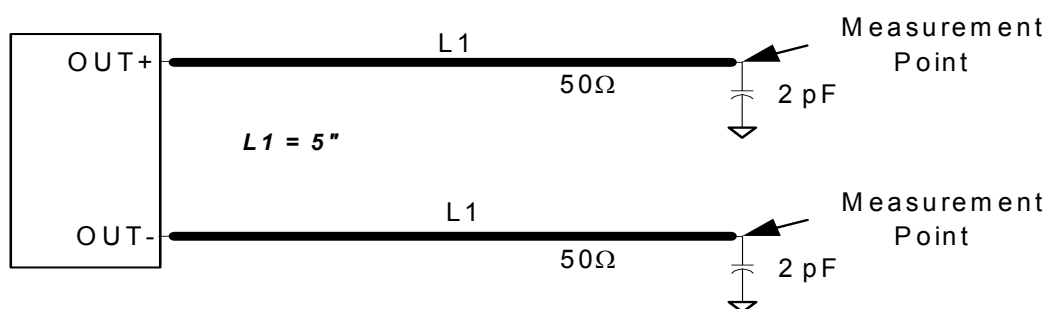
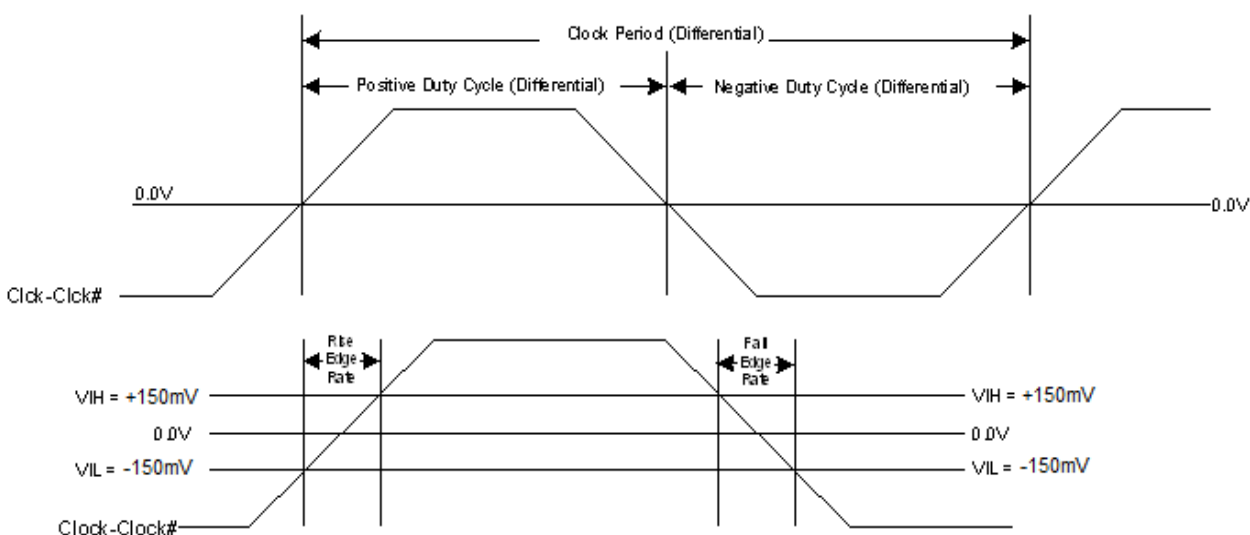


Figure 3. 0.7 V Differential Load Configuration

Please reference application note AN781 recommendations on how to terminate the differential outputs for LVDS, LVPECL, or CML signalling levels.



**Figure 4. Differential Output Measurement for Differential Signals
(for AC Parameters Measurement)**

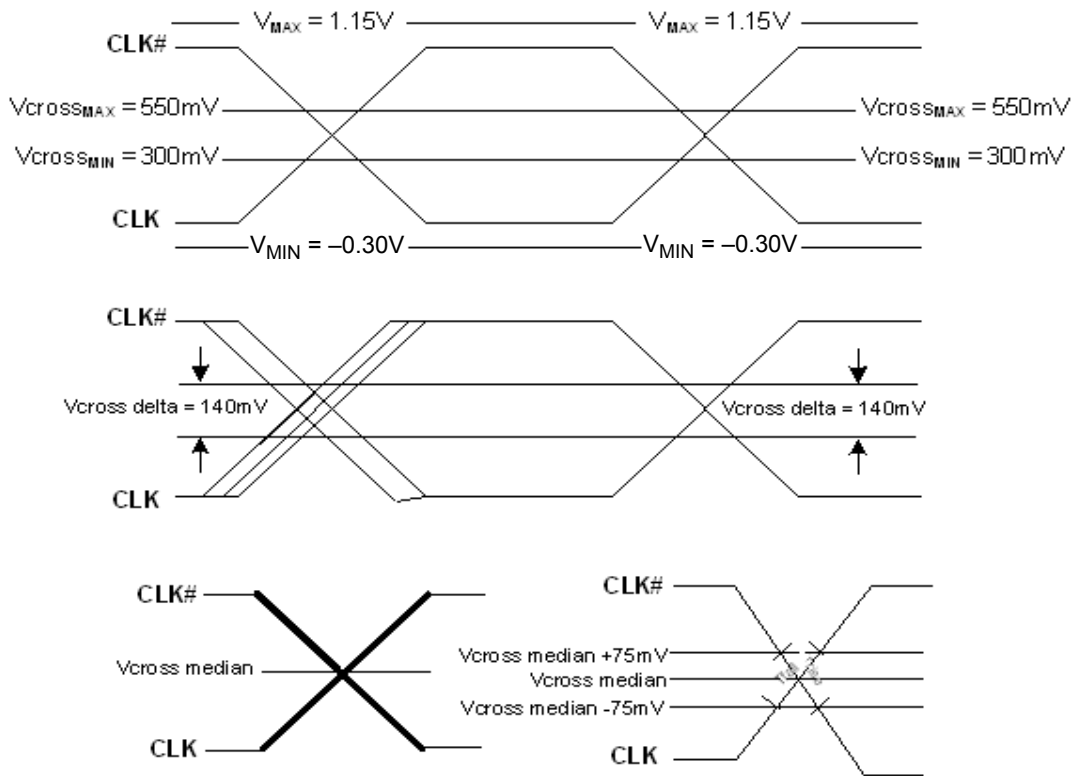


Figure 5. Single-ended Measurement for Differential Output Signals (for AC Parameters Measurement)

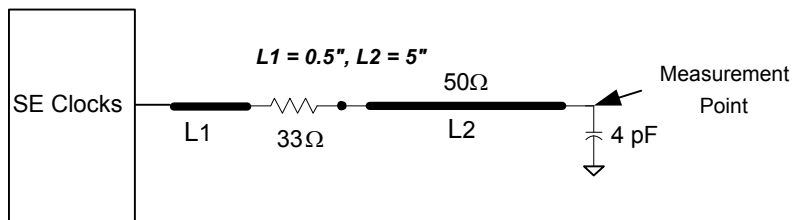


Figure 6. Single-Ended Clocks with Single Load Configuration

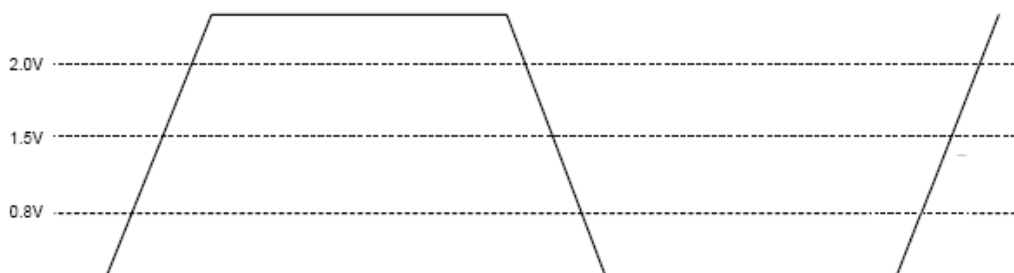


Figure 7. Single-Ended Output Signal (for AC Parameter Measurement)

4. Control Registers

4.1. I²C Interface

To enhance the flexibility and function of the clock synthesizer, an I²C interface is provided. Through the I²C Interface, various device functions are available, such as individual clock enablement. The registers associated with the I²C Interface initialize to their default setting at power-up. The use of this interface is optional. Clock device register changes are normally made at system initialization, if any are required. Power management functions can only be programmed in program mode and not in normal operation modes.

4.2. Data Protocol

The clock driver I²C protocol accepts byte write, byte read, block write, and block read operations from the controller. For block write/read operation, access the bytes in sequential order from lowest to highest (most significant bit first) with the ability to stop after any complete byte is transferred. For byte write and byte read operations, the system controller can access individually indexed bytes.

The block write and block read protocol is outlined in Table 5 while Table 6 outlines byte write and byte read protocol. The slave receiver address is 11010110 (D6h).

Table 5. Block Read and Block Write Protocol

| Block Write Protocol | | Block Read Protocol | |
|----------------------|-------------------------------|---------------------|-----------------------------------|
| Bit | Description | Bit | Description |
| 1 | Start | 1 | Start |
| 8:2 | Slave address—7 bits | 8:2 | Slave address—7 bits |
| 9 | Write | 9 | Write |
| 10 | Acknowledge from slave | 10 | Acknowledge from slave |
| 18:11 | Command Code—8 bits | 18:11 | Command Code—8 bits |
| 19 | Acknowledge from slave | 19 | Acknowledge from slave |
| 27:20 | Byte Count—8 bits | 20 | Repeat start |
| 28 | Acknowledge from slave | 27:21 | Slave address—7 bits |
| 36:29 | Data byte 1—8 bits | 28 | Read = 1 |
| 37 | Acknowledge from slave | 29 | Acknowledge from slave |
| 45:38 | Data byte 2—8 bits | 37:30 | Byte Count from slave—8 bits |
| 46 | Acknowledge from slave | 38 | Acknowledge |
| | Data Byte /Slave Acknowledges | 46:39 | Data byte 1 from slave—8 bits |
| | Data Byte N—8 bits | 47 | Acknowledge |
| | Acknowledge from slave | 55:48 | Data byte 2 from slave—8 bits |
| | Stop | 56 | Acknowledge |
| | | | Data bytes from slave/Acknowledge |
| | | | Data Byte N from slave—8 bits |
| | | | NOT Acknowledge |
| | | | Stop |

Table 6. Byte Read and Byte Write Protocol

| Byte Write Protocol | | Byte Read Protocol | |
|---------------------|------------------------|--------------------|------------------------|
| Bit | Description | Bit | Description |
| 1 | Start | 1 | Start |
| 8:2 | Slave address–7 bits | 8:2 | Slave address–7 bits |
| 9 | Write | 9 | Write |
| 10 | Acknowledge from slave | 10 | Acknowledge from slave |
| 18:11 | Command Code–8 bits | 18:11 | Command Code–8 bits |
| 19 | Acknowledge from slave | 19 | Acknowledge from slave |
| 27:20 | Data byte–8 bits | 20 | Repeated start |
| 28 | Acknowledge from slave | 27:21 | Slave address–7 bits |
| 29 | Stop | 28 | Read |
| | | 29 | Acknowledge from slave |
| | | 37:30 | Data from slave–8 bits |
| | | 38 | NOT Acknowledge |
| | | 39 | Stop |

Control Register 0. Byte 0

| Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|-----|-----|-----|-----|-----|--------|-----|-----|
| Name | | | | | | REF_OE | | |
| Type | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

Reset settings = 00000100

| Bit | Name | Function |
|-----|----------|----------------------------------------------------------------------------|
| 7:3 | Reserved | |
| 2 | REF_OE | Output Enable for REF. 0: Output disabled. 1: Output enabled. |
| 1:0 | Reserved | |

Control Register 1. Byte 1

| Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|-----|-----|-----|-----|-----|----------|-----|----------|
| Name | | | | | | DIFF0_OE | | DIFF1_OE |
| Type | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

Reset settings = 00000101

| Bit | Name | Function |
|-----|----------|------------------------------------------------------------------------------|
| 7:3 | Reserved | |
| 2 | DIFF0_OE | Output Enable for DIFF0. 0: Output disabled. 1: Output enabled. |
| 1 | Reserved | |
| 0 | DIFF1_OE | Output Enable for DIFF1. 0: Output disabled. 1: Output enabled. |

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Control Register 2. Byte 2

| Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|----------|----------|-----|-----|-----|-----|-----|-----|
| Name | DIFF2_OE | DIFF3_OE | | | | | | |
| Type | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

Reset settings = 11000000

| Bit | Name | Function |
|-----|----------|------------------------------------------------------------------------------|
| 7 | DIFF2_OE | Output Enable for DIFF2. 0: Output disabled. 1: Output enabled. |
| 6 | DIFF3_OE | Output Enable for DIFF3. 0: Output disabled. 1: Output enabled. |
| 5:0 | Reserved | |

Control Register 3. Byte 3

| Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|---------------|-----|-----|-----|----------------|-----|-----|-----|
| Name | Rev Code[3:0] | | | | Vendor ID[3:0] | | | |
| Type | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

Reset settings = 00001000

| Bit | Name | Function |
|-----|----------------|------------------------------------|
| 7:4 | Rev Code[3:0] | Program Revision Code. |
| 3:0 | Vendor ID[3:0] | Vendor Identification Code. |

Control Register 4. Byte 4

| Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|---------|-----|-----|-----|-----|-----|-----|-----|
| Name | BC[7:0] | | | | | | | |
| Type | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

Reset settings = 00000110

| Bit | Name | Function |
|-----|---------|-----------------------------|
| 7:0 | BC[7:0] | Byte Count Register. |

Control Register 5. Byte 5

| Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|--------------|------------------|------------------|------------------|-----|-----|-----|-----|
| Name | DIFF_Amp_Sel | DIFF_Amp_Cntl[2] | DIFF_Amp_Cntl[1] | DIFF_Amp_Cntl[0] | | | | |
| Type | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

Reset settings = 11011000

| Bit | Name | Function |
|-----|------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7 | DIFF_Amp_Sel | Amplitude Control for DIFF Differential Outputs. 0: Differential outputs with Default amplitude. 1: Differential outputs amplitude is set by Byte 5[6:4]. |
| 6 | DIFF_Amp_Cntl[2] | DIFF Differential Outputs Amplitude Adjustment. 000: 300 mV 001: 400 mV 010: 500 mV 011: 600 mV 100: 700 mV 101: 800 mV 110: 900 mV 111: 1000 mV |
| 5 | DIFF_Amp_Cntl[1] | |
| 4 | DIFF_Amp_Cntl[0] | |
| 3:0 | Reserved | |

5. Pin Descriptions: 24-Pin QFN

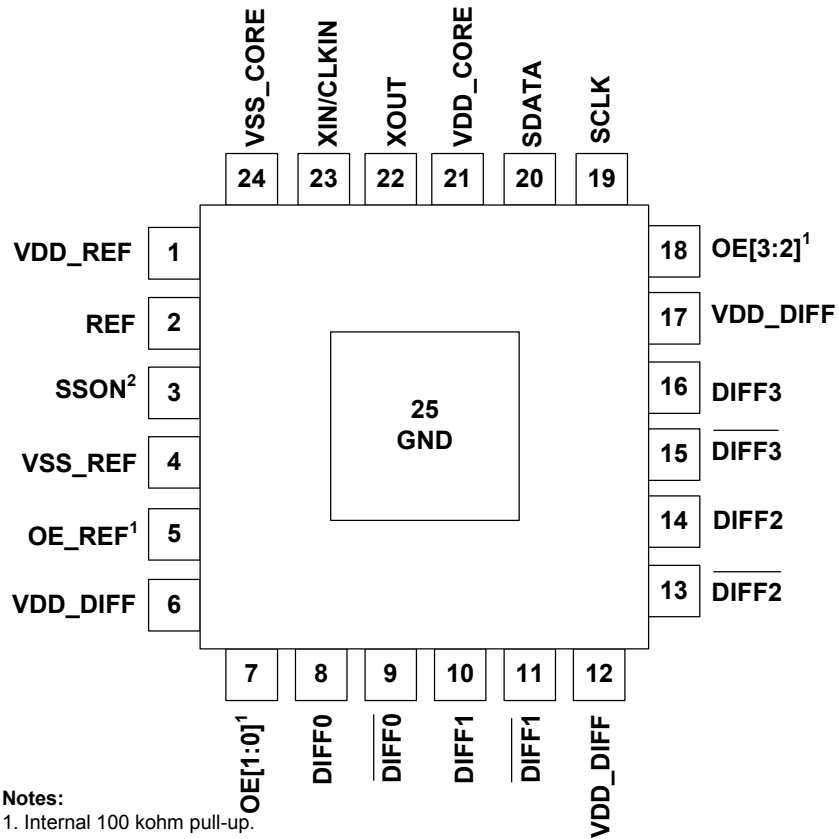


Table 7. Si52143 24-Pin QFN Descriptions

| Pin # | Name | Type | Description |
|-------|---------------------------|--------|-----------------------------------------------------------------------------------------|
| 1 | VDD_REF | PWR | 3.3 V power supply. |
| 2 | REF | O, SE | 3.3 V, 25 MHz crystal reference clock output. |
| 3 | SSON | I,PD | Active high input pin enables –0.5% spread on DIFF outputs (internal 100 kΩ pull-down). |
| 4 | VSS_REF | GND | Ground |
| 5 | OE_REF | I,PU | Active high input to enable or disable REF clock. |
| 6 | VDD_DIFF | PWR | 3.3 V power supply. |
| 7 | OE[1:0] | I,PU | Active high input to enable or disable DIFF0 and DIFF1 clocks. |
| 8 | DIFF0 | O, DIF | 0.7 V, 100 MHz differential clock output. |
| 9 | $\overline{\text{DIFF0}}$ | O, DIF | 0.7 V, 100 MHz differential clock output. |
| 10 | DIFF1 | O, DIF | 0.7 V, 100 MHz differential clock output. |

Table 7. Si52143 24-Pin QFN Descriptions (Continued)

| Pin # | Name | Type | Description |
|-------|---------------------------|--------|-------------------------------------------------------------------------|
| 11 | $\overline{\text{DIFF1}}$ | O, DIF | 0.7 V, 100 MHz differential clock output. |
| 12 | VDD_DIFF | PWR | 3.3 V power supply. |
| 13 | $\overline{\text{DIFF2}}$ | O, DIF | 0.7 V, 100 MHz differential clock output. |
| 14 | DIFF2 | O, DIF | 0.7 V, 100 MHz differential clock output. |
| 15 | $\overline{\text{DIFF3}}$ | O, DIF | 0.7 V, 100 MHz differential clock output. |
| 16 | DIFF3 | O, DIF | 0.7 V, 100 MHz differential clock output. |
| 17 | VDD_DIFF | PWR | 3.3 V power supply. |
| 18 | OE[3:2] | I,PU | Active high input to enable or disable DIFF2 and DIFF3 clocks. |
| 19 | SCLK | I | I ² C SCLOCK. |
| 20 | SDATA | I/O | I ² C SDATA. |
| 21 | VDD_CORE | PWR | 3.3 V power supply. |
| 22 | XOUT | O | 25.00 MHz crystal output, Float XOUT if using only CLKIN (Clock input). |
| 23 | XIN/CLKIN | I | 25.00 MHz crystal input or 3.3 V, 25 MHz Clock Input. |
| 24 | VSS_CORE | GND | Ground. |
| 25 | GND | GND | Ground for bottom pad of the IC. |

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6. Ordering Guide

| Part Number | Package Type | Temperature |
|------------------|--------------------------|--------------------------|
| Lead-free | | |
| Si52143-A01AGM | 24-pin QFN | Industrial, -40 to 85 °C |
| Si52143-A01AGMR | 24-pin QFN—Tape and Reel | Industrial, -40 to 85 °C |

7. Package Outline

Figure 8 illustrates the package details for the Si52143. Table 8 lists the values for the dimensions shown in the illustration.

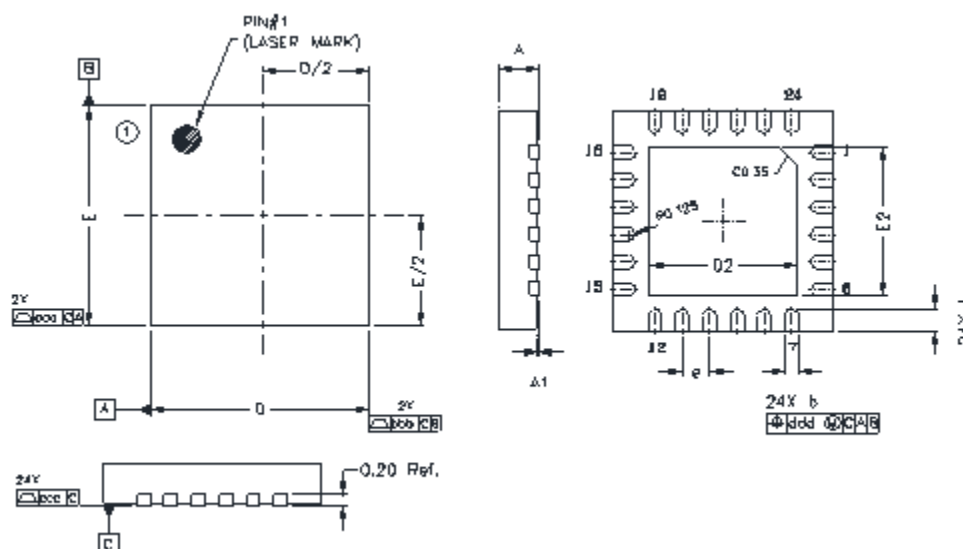


Figure 8. 24-Pin Quad Flat No Lead (QFN) Package

Table 8. Package Diagram Dimensions

| Symbol | Millimeters | | |
|------------------------------------------------------------------------------------------------------------|-------------|-------|------|
| | Min | Nom | Max |
| A | 0.70 | 0.75 | 0.80 |
| A1 | 0.00 | 0.025 | 0.05 |
| b | 0.20 | 0.25 | 0.30 |
| D | 4.00 BSC | | |
| D2 | 2.60 | 2.70 | 2.80 |
| e | 0.50 BSC | | |
| E | 4.00 BSC | | |
| E2 | 2.60 | 2.70 | 2.80 |
| L | 0.30 | 0.40 | 0.50 |
| aaa | 0.10 | | |
| bbb | 0.10 | | |
| ccc | 0.08 | | |
| ddd | 0.07 | | |
| Notes: | | | |
| 1. All dimensions shown are in millimeters (mm) unless otherwise noted. | | | |
| 2. Dimensioning and Tolerancing per ANSI Y14.5M-1994. | | | |
| 3. This drawing conforms to JEDEC outline MO-220, variation VGGD-8. | | | |
| 4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components. | | | |

8. Land Pattern

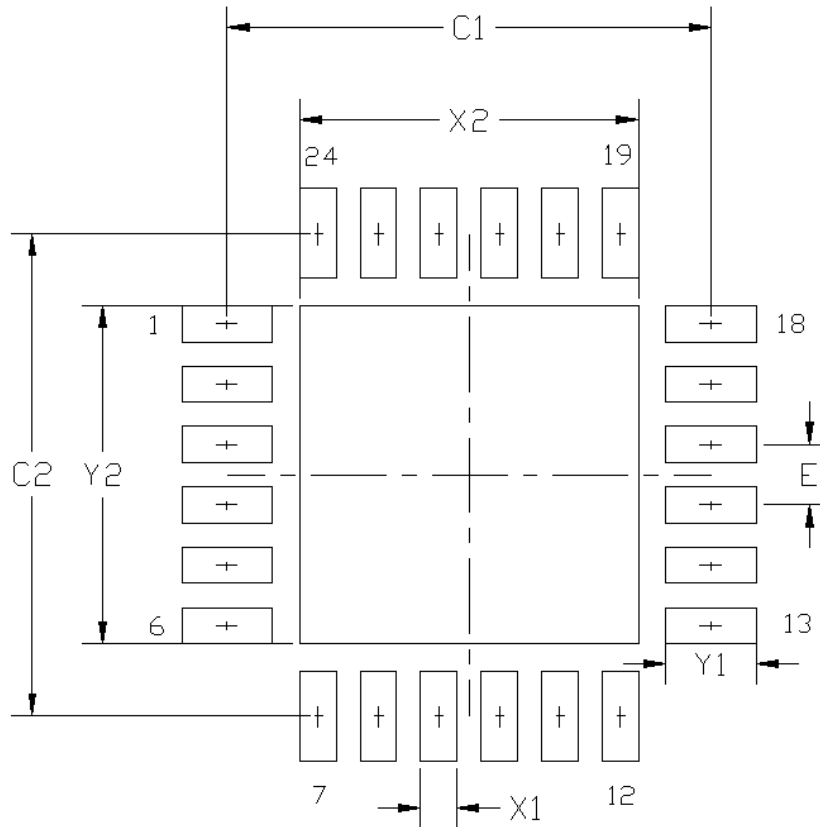


Figure 9. QFN Land Pattern

Table 9. Land Pattern Dimensions

| Dimension | Unit mm |
|-----------|----------|
| C1 | 4.0 |
| C2 | 4.0 |
| E | 0.50 BSC |
| X1 | 0.30 |
| X2 | 2.70 |
| Y1 | 0.80 |

Table 9. Land Pattern Dimensions (Continued)

| Y2 | 2.70 |
|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|
| <p>Notes:</p> <p>General</p> <ol style="list-style-type: none"> 1. All dimensions shown are in millimeters (mm) unless otherwise noted. 2. This land pattern design is based on the IPC-7351 guidelines. <p>Solder Mask Design</p> <ol style="list-style-type: none"> 3. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 μm minimum, all the way around the pad. <p>Stencil Design</p> <ol style="list-style-type: none"> 4. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release. 5. The stencil thickness should be 0.125 mm (5 mils). 6. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter 7. pads. 8. A 2x2 array of 1.10 mm x 1.10 mm openings on 1.30mm pitch should be used for the center ground pad. <p>Card Assembly</p> <ol style="list-style-type: none"> 9. A No-Clean, Type-3 solder paste is recommended. 10. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components. | |

DOCUMENT CHANGE LIST

Revision 0.1 to Revision 1.0

- Updated Features on page 1.
- Updated Description on page 1.
- Updated Table 1 on page 4.
- Updated Table 2 on page 5.
- Updated Section 2.1 on page 7.
- Updated Section 2.1.1 on page 7.
- Updated Section 4.1 on page 11.
- Updated Section 4.2 on page 11.
- Updated Pin Descriptions on page 16.

Revision 1.0 to Revision 1.1

- Removed Moisture Sensitivity Level specification from Table 3.

Revision 1.1 to Revision 1.2

- Updated Table 2.
- Updated Section 3.

Revision 1.2 to Revision 1.3

- Updated Features on page 1.
- Updated Description on page 1.
- Updated Table 2, “AC Electrical Specification,” on page 5.

Revision 1.3 to Revision 1.4

- Added test condition to Tstable in Table 2.



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