Innovative DSPLL® and MultiSynth Clock Architecture Enables High-Density 10/40/100G Line Card Designs

Introduction

The insatiable demand for bandwidth to support applications such as video streaming and cloud computing is driving telecom service providers to continuously increase network capacity and migrate to higher speed Internet infrastructure equipment.

To minimize the capital investment required to expand network capacity, operators are increasingly seeking networking equipment solutions that support faster data transmission and significantly higher optical port density. These trends are now accelerating as metro and core networks transition from 10/40G to 100G/400G and as Carrier Ethernet networks migrate to higher port count and higher switching density 10/40 Gigabit Ethernet (GbE) edge routers.

To complicate matters, there is intense pressure on manufacturers to significantly reduce the cost-per-bit of optical transmission equipment. As a result, telecom equipment providers are designing the next generation of metro packet-optical and mobile backhaul equipment that accelerates network convergence and effectively lowers the cost-per-bit.

These platforms combine high-speed data transmission with greater port density and functional integration. For example, many of these new systems support OTN switching and IP/MPLS in a single converged services platform optimized for software-defined networking (SDN) applications.

These industry trends and the overall market pressure to reduce optical transmission and switching cost-per-bit significantly increase the need for highly integrated, high-performance, frequency-flexible clocks that are easily reconfigurable across a broad range of applications. Table 1 (see page 1) lists common communications protocols and their associated reference frequencies that must be supported by next-generation OTN equipment.

Protocol	Network	Protocol Description	Data Rates (Gbps)	Frequencies (MHz)
GbE	WAN, LAN	Gigabit Ethernet	1	125
10GbE		10 Gigabit Ethernet WAN	10	156.25
		10 Gigabit Ethernet LAN		161.1328125
100GbE		100 Gigabit Ethernet	100	644.53125
OTU-1	Metro and Core Optical	Transports SONET OC-48 or synchronous digital hierarchy (SDH) STM-16 signal	2.66	166.6285714
OTU-2		Transports an OC-192, STM-64 or wide area network (WAN) physical layer (PHY) for 10 Gigabit Ethernet	10.7	167.3316456
OTU-4		Transport for 100 Gigabit Ethernet	112	698.8123348
3G-SDI	Broadcast Video	Third-Generation Serial Digital Interface for video	2.97	148.3516484, 148.5
CPRI	Wireless Base Stations	Common Public Radio Interface for wireless base stations	3.072	153.6
			6.144	307.2
OC-12/STM-4	Metro and Core Optical	Synchronous Optical Networking (SONET) protocols for fiber optic networks	0.622	77.76
OC-48/STM-16			2.488	155.52
OC-192/STM-64			9.95	622.08
FC-200 (2GFC)	Storage	Fibre Channel Storage Networks	0.4	132.8125
FC-400 (4GFC)			0.8	132.8125
FC-800 (8GFC)			1.6	132.8125
FC-1200 (10GFC)			2.4	164.3554688
Infiniband	Data centers	Switched fabric for high-performance computing and enterprise data centers	10	156.25

Table 1. Common Protocols Supported by OTN Equipment

Simplified Clock Generation in OTN and 10/40/100G Ethernet

Figure 1 shows a high-level block diagram of a packet optical transport switch (P-OTS) or packet transport network (PTN) platform. Silicon Labs has developed a new portfolio of clock generators and jitter attenuators optimized for high-speed, frequency-flexible, ultra-low-jitter clock synthesis. These clock devices enable system designers to design “any-port, any-protocol” line cards with industry-leading jitter performance of < 100 fs RMS typical (12 kHz to 20 MHz). The devices also support “on-the-fly” frequency reconfiguration. This feature dramatically simplifies system design, enabling significantly lower cost and more flexible service provisioning in SDN environments. Service provisioning allows network operators to respond to users’ rapidly-changing demands for diverse voice, video and data services, such as cloud storage, video streaming and mobile services.

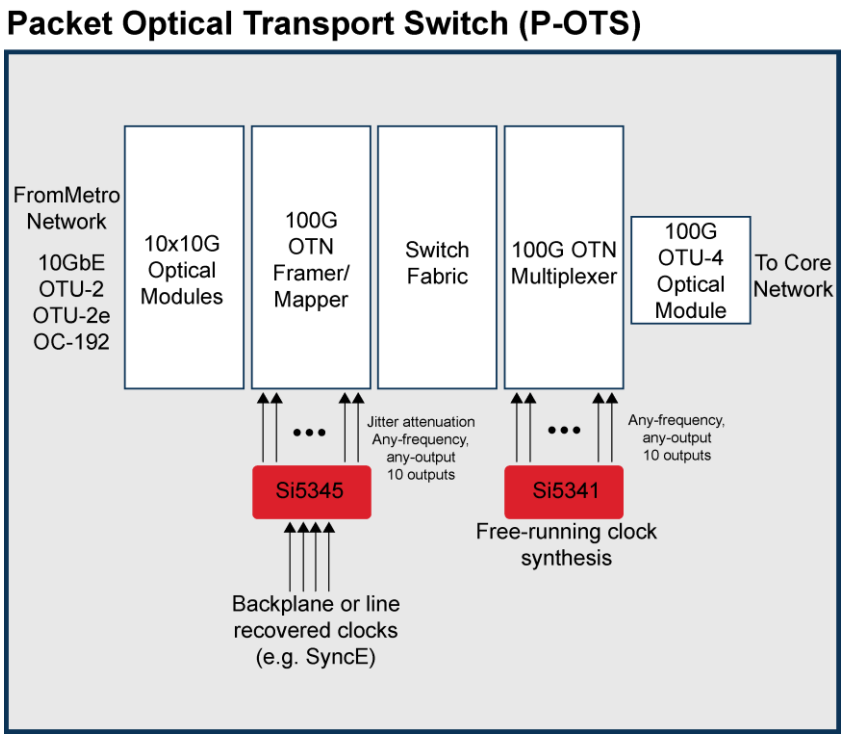

Figure 1. Packet Optical Transport Switch Block Diagram

Function	Device	# PLLs	# MultiSynth Fractional Dividers	Clock Inputs	Clock Outputs	Jitter, RMS typ (12 kHz to 20 MHz)	Loop Bandwidth	Key Features
Clock Generation	Si5340	1	4	3	4	< 100 fs* < 150 fs**	1 MHz	In-circuit programmable configurable output drivers, glitchless on-the-fly frequency changes, LOS/LOL monitors, built-in power supply filtering, I2C/SPI control, any-frequency synthesis with 0 ppm error
	Si5341	1	5	3	10		1 MHz	
Jitter Attenuation	Si5342	1	2	4	2	< 100 fs* < 150 fs**	0.1 Hz to 4 kHz	Same features as Si5340/41 plus jitter attenuation, hitless switching, holdover, fast-lock, DCO mode, any-frequency synthesis with 0 ppm error
	Si5344	1	4	4	4			
	Si5345	1	5	4	10			
	Si5346	2	-	4	4			
	Si5347	4	-	4	8			

Table 2. Si534x Clock Generators and Jitter-Attenuating Clocks

Fourth-Generation DSPLL vs. Traditional High Performance Clock Architectures

The Si5345/44/42 jitter attenuators leverage a unique, proprietary architecture that delivers greater frequency flexibility, lower jitter, lower phase noise and improved spurious performance compared to traditional clock architectures. These new devices have been designed using the most advanced process technology for any standalone clock device (55 nm CMOS), making it possible to deliver unparalleled performance and frequency synthesis flexibility in a single, unified architecture. Figure 2 shows a simplified view comparing Silicon Labs' Si5345 clocks and traditional approaches.

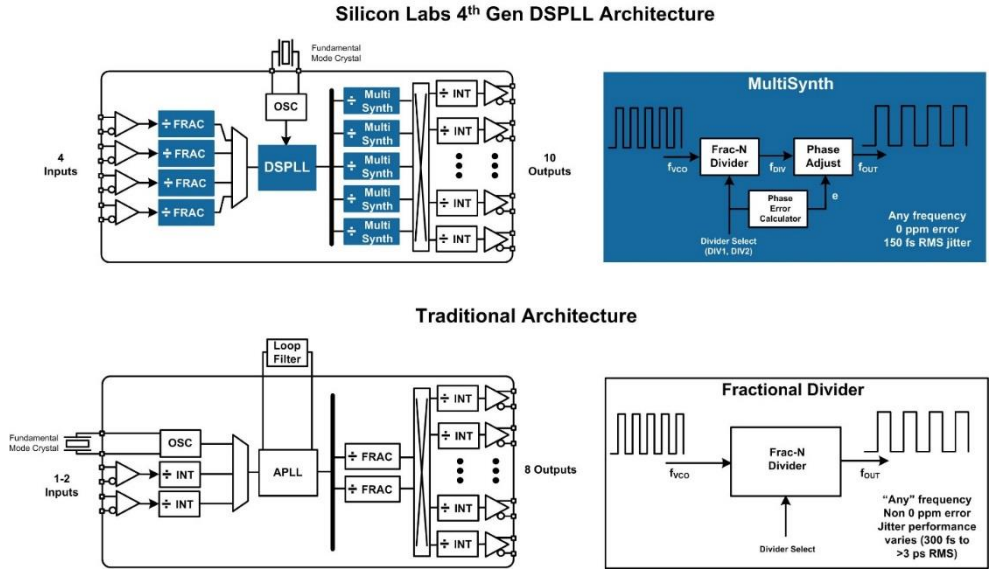

Figure 2. Silicon Labs' Fourth-Generation DSPLL Architecture vs. Traditional Approach

The Si5345 supports a flexible input stage with independent fractional dividers for each clock input. This integration simplifies interfacing the device to a wide range of clocks from different sources (e.g. BITS, SyncE, SONET/SDH, PDH, ASIC, FPGA). The DSPLL provides jitter attenuation, any-frequency translation, hitless switching and holdover. The DSPLL combines an analog LC-VCO with a DSP-based digital loop filter and digital phase detector. This hybrid mixed-signal approach offers the best of both worlds: low phase noise and low-jitter clock synthesis in a highly-integrated, digitally-programmable architecture. The loop filter function is integrated on-chip, eliminating discrete filter components and simplifying PCB layout.

The Si5345 device supports an integrated fast-lock feature that enables extremely fast PLL acquisition regardless of loop bandwidth settings (<100 msec). In addition to eliminating noise coupling associated with external filter components, the DSPLL bandwidth is user-programmable across the 0.1 Hz to 4 kHz range, enabling application-dependent loop bandwidth selection while minimizing jitter transfer. In contrast, most traditional APLL solutions require discrete loop filters, which are sensitive to board-level noise, impact jitter generation and increase PCB layout complexity.

The DSPLL drives five independent MultiSynth fractional dividers, which are connected via a non-blocking cross point switch to an array of 10 clock outputs. In the first stage of the MultiSynth architecture, Silicon Labs' MultiSynth high-speed fractional-N divider seamlessly switches between the two closest integer divider values to produce an exact output clock frequency with 0 ppm frequency synthesis error. To eliminate phase error generated by this process, MultiSynth calculates the relative phase difference between the clock produced by the fractional-N divider and the desired output clock and dynamically adjusts the phase to match the ideal clock waveform.

This novel approach makes it possible to generate any-output clock frequencies from 1 kHz to 800 MHz with 0 ppm error while achieving better than 100 fs RMS phase jitter performance (12 kHz to 20 MHz) in integer mode and less than 150 fs in its synthesis mode which simultaneously generates both fractional and integer related clocks. In contrast, traditional architectures rely on conventional fractional dividers that do not perform phase error cancellation, resulting in significantly higher output jitter when the device is configured to generate fractional output clocks.

Si5345/44/42 Jitter Performance

The jitter measurements in Table 3 show typical jitter performance when the Si5345/44/42 is configured for a typical 10/40/100G OTN application. The Si534x provides highly-consistent, repeatable ultra-low-jitter performance across process, voltage and temperature.

Input Clock	Output Clocks	Phase Jitter (12 kHz to 20 MHz)
38.88 MHz	155.52 MHz	137 fs RMS
	156.25 MHz	120 fs RMS
	164.36 MHz	143 fs RMS
	167.33 MHz	133 fs RMS
	173.37 MHz	101 fs RMS

Fourth-Generation DSPLL Enables High Port Density Line Cards

Next-generation 10/40/100G OTN switching and transmission equipment is transitioning to higher port densities to further scale network capacity. This is increasing the market need for more highly integrated physical-layer timing devices that provide multiple independent PLLs in a single IC, minimizing the PCB footprint in tightly packed, high-density line cards.

The fourth-generation DSPLL architecture is compact and scalable, making it possible to build monolithic, single-chip multi-PLL jitter attenuating clocks that are significantly smaller and lower jitter than competing solutions. Figure 3 contrasts the Si5347 quad-DSPLL jitter attenuating clock with a conventional digital + analog phase-locked loop (DPLL + APLL) approach. Conventional solutions use a DPLL for jitter attenuation and an APLL for frequency translation. This architecture is not optimized for space, power or performance. Because each APLL uses a discrete VCO, the traditional architecture is highly-susceptible to crosstalk when the VCOs are operating in close frequency proximity.

In contrast, Silicon Labs' DSPLL architecture replaces both the DPLL and APLL. The DSPLL leverages a highly-digital, low-noise architecture to deliver a solution that is highly optimized for space and power. Each DSPLL is isolated using an extensive number of on-chip regulators, providing noise isolation while minimizing susceptibility to crosstalk. As a result, the Si5347 device delivers any-frequency clock synthesis with greater than 60 percent lower jitter and a 50 percent smaller footprint than comparable multi-PLL solutions. With this approach, the Si5347 provides the highest level of PLL integration and performance in the industry.

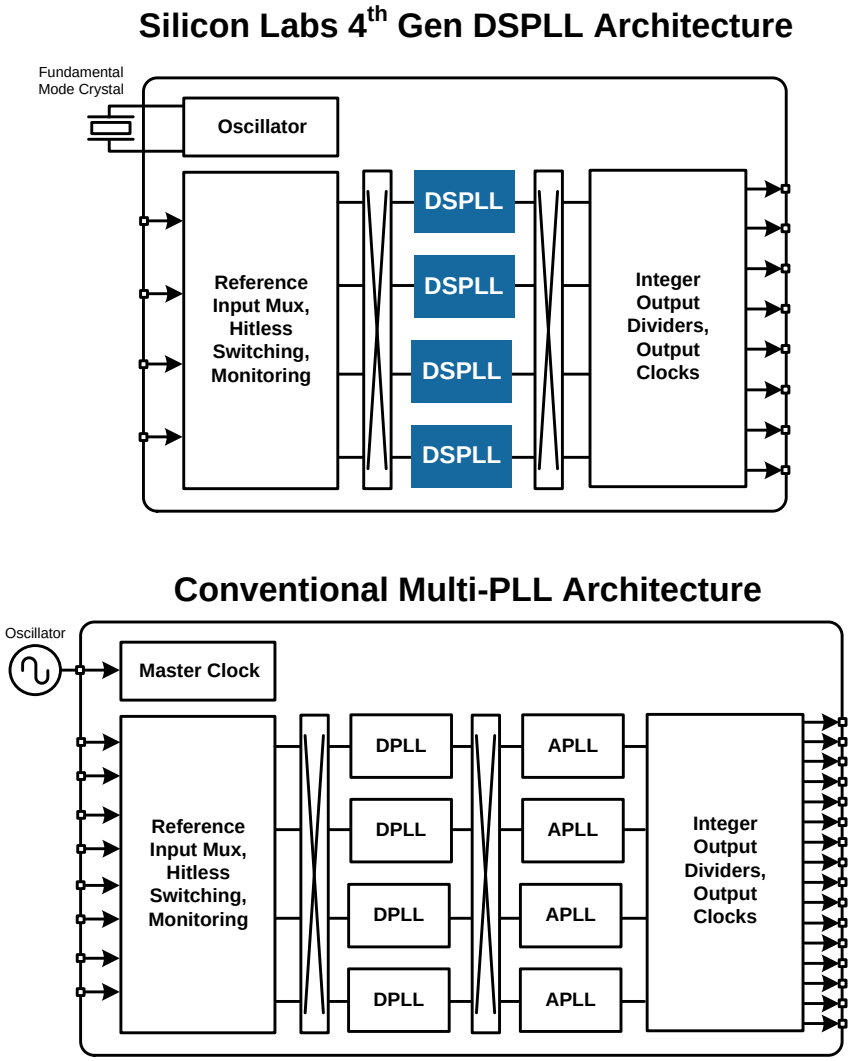

Figure 3. Quad-DSPLL Jitter Attenuating Clock vs. Conventional Multi-PLL Architecture

Si534x Power Supply Noise Rejection

The Si534x clocks provide extensive on-chip regulation to minimize the impact of board-level noise on clock output jitter. For the data summarized in Table 4, 100 mVpp sinusoidal noise was applied to the

device power pins, and jitter was measured at the clock outputs. A 1.0 uF bypass cap was used on every VDD pin; otherwise, no power supply filtering components were used.

Noise Frequency	100 kHz	200 kHz	300 kHz	400 kHz	500 kHz
Si534x Jitter (RMS)	138 fs	142 fs	144 fs	142 fs	144 fs

Table 4. Si534x Jitter Generation When Subjected to 100mVpp Sinusoidal Noise on Device Power Supply
(f_{IN} = 25 MHz, f_{OUT} = 156.25 MHz)

Summary

Silicon Labs' fourth-generation DSPLL clocks leverage cutting-edge, mixed-signal analog design and 55 nm CMOS technology to deliver any-frequency, any-output clock synthesis with industry-leading PLL integration and jitter performance. Hardware designers can leverage these new products to minimize the timing component BOM count and complexity required to build any-protocol, any-port, high-density 10/40/100G OTN and Ethernet line cards.

Learn more about Silicon Labs' timing solutions at www.silabs.com/timing

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